BECKHOFF

CB3053

Manual

rev. 1.3

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Contents

0 Document History

Version	Changes
0.1	first pre-release
1.0	added dimensional drawings
1.1	added maximum current on 2x3 connector, no more TTL option for COM, updated block diagram (ALC885 EOL), minor changes
1.2	improved output quality of dimensional drawings, minor changes
1.3	corrected LAN pinout

NOTE

1 Introduction

1.1 Notes on the Documentation

This description is only intended for the use of trained specialists in control and automation engineering who are familiar with the applicable national standards. It is essential that the following notes and explanations are followed when installing and commissioning these components.

1.1.1 Liability Conditions

The responsible staff must ensure that the application or use of the products described satisfy all the requirements for safety, including all the relevant laws, regulations, guidelines and standards.
The documentation has been prepared with care. The products described are, however, constantly under development. For that reason the documentation is not in every case checked for consistency with performance data, standards or other characteristics. None of the statements of this manual represents a guarantee (Garantie) in the meaning of § 443 BGB of the German Civil Code or a statement about the contractually expected fitness for a particular purpose in the meaning of § 434 par. 1 sentence 1 BGB. In the event that it contains technical or editorial errors, we retain the right to make alterations at any time and without warning. No claims for the modification of products that have already been supplied may be made on the basis of the data, diagrams and descriptions in this documentation.

1.1.2 Copyright

1.2 Safety Instructions

Please consider the following safety instructions and descriptions. Product specific safety instructions are to be found on the following pages or in the areas mounting, wiring, commissioning etc.

1.2.1 Disclaimer

All the components are supplied in particular hardware and software configurations appropriate for the application. Modifications to hardware or software configurations other than those described in the documentation are not permitted, and nullify the liability of Beckhoff Automation GmbH.

1.2.2 Description of Safety Symbols

The following safety symbols are used in this documentation. They are intended to alert the reader to the associated safety instructions.

ACUTE RISK OF INJURY!

If you do not adhere to the safety advise next to this symbol, there is immediate danger to life and health of individuals!

RISK OF INJURY!

If you do not adhere to the safety advise next to this symbol, there is danger to life and health of individuals!

HAZARD TO INDIVIDUALS, ENVIRONMENT, DEVICES, OR DATA!

If you do not adhere to the safety advise next to this symbol, there is obvious hazard to individuals, to environment, to materials, or to data.

NOTE OR POINTER

This symbol indicates information that contributes to better understanding.

1.3 Essential Safety Measures

1.3.1 Operator's Obligation to Exercise Diligence

The operator must ensure that

- the product is only used for its intended purpose
- the product is only operated in sound condition and in working order
- the instruction manual is in good condition and complete, and always available for reference at the location where the products are used
- the product is only used by suitably qualified and authorised personnel
- the personnel is instructed regularly about relevant occupational safety and environmental protection aspects
- the operating personnel is familiar with the operating manual and in particular the safety notes contained herein

1.3.2 National Regulations Depending on the Machine Type

Depending on the type of machine and plant in which the product is used, national regulations governing the controllers of such machines will apply, and must be observed by the operator. These regulations cover, amongst other things, the intervals between inspections of the controller. The operator must initiate such inspections in good time.

1.3.3 Operator Requirements

- Read the operating instructions

All users of the product must have read the operating instructions for the system they work with.

- System know-how

All users must be familiar with all accessible functions of the product.

1.4 Functional Range

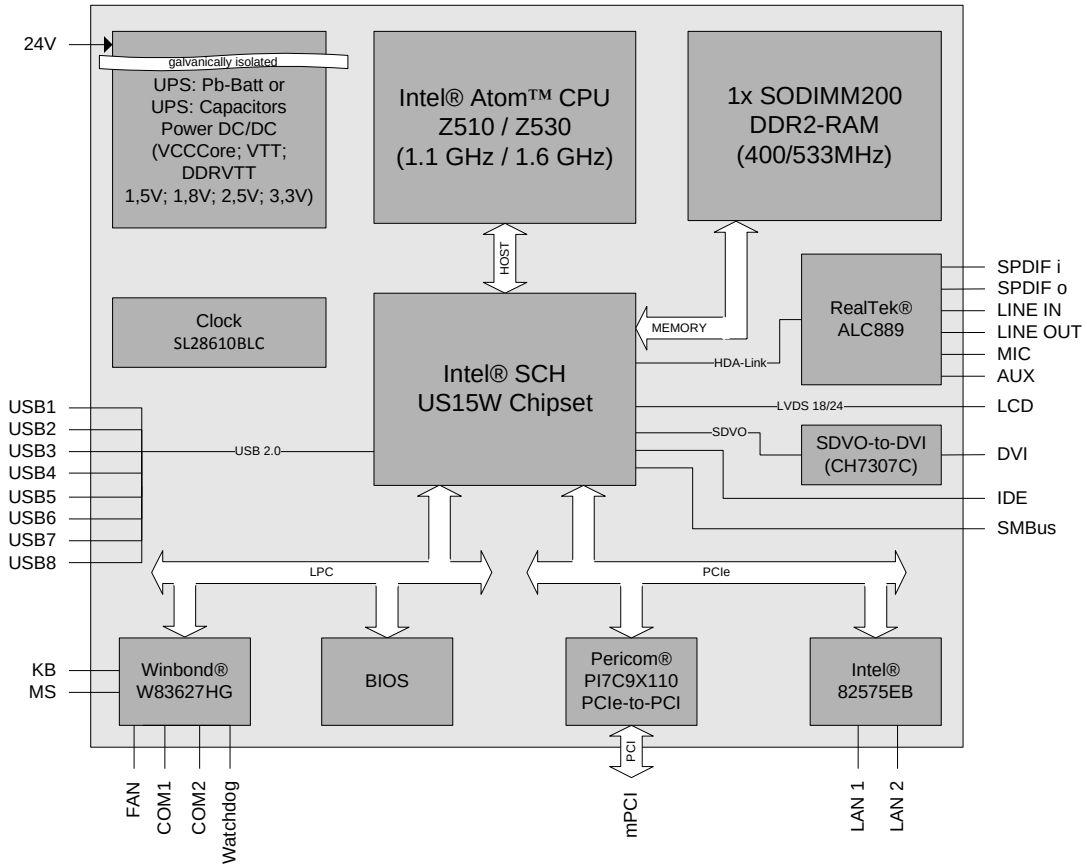
NOTE

The descriptions contained in the present documentation represent a detailed and extensive product description. As far as the described motherboard was acquired as an integral component of an Industrial PC from Beckhoff Automation GmbH, this product description shall be applied only in limited scope. Only the contractually agreed specifications of the corresponding Industrial PC from Beckhoff Automation GmbH shall be relevant. Due to several models of Industrial PCs, variations in the component placement of the motherboards are possible. Support and service benefits for the built-in motherboard will be rendered by Beckhoff Automation GmbH exclusively as specified in the product description (inclusive operation system) of the particular Industrial PC.

2 Overview

2.1 Features

The CB3053 is a highly complex 3,5-inch board which incorporates complete motherboard functionality. Equipped with an Intel® Atom™ processor (Z510 or Z530), it can accommodate up to 2 GByte of RAM (DDR2-533) via SO-DIMM200. It also provides a PCI bus (via mPCI connector) and additional peripheral devices such as two serial interfaces, two Gigabit Ethernet interfaces (LAN), an IDE interface, an audio interface (HDA 5.1), eight USB channels, DVI and LVDS/TFT support, and a touchscreen connector. The board is based on Intel®'s Menlow® platform which is optimized for low power consumption. Relieving system designers of the burden that the need for active cooling normally presents, Menlow® offers attractive new possibilities in the embedded and mobile markets. As a special feature, the board provides either an internal (capacitor-based) or an external (Pb-battery) UPS device.



- Processor Intel® Atom™ (single core, 512KB L2-cache, up to 1.6 GHz clock speed)
- Chipset Intel® SCH US15W with integrated graphics adapter
- SO-DIMM200 socket for one DDR2-533 module of up to 2 GByte
- Two serial interfaces COM1 and COM2
- Two LAN interfaces Ethernet 10/100/1000 (Base-T)
- IDE interface
- PS2 keyboard / mouse interface
- Eight USB 2.0 interfaces
- AWARD BIOS 6.10
- DVI connection
- LCD connection via LVDS 18/24Bit

- AC97/HDA compatible sound controller with SPDIF in and out
- RTC with external CMOS battery
- 24V supply voltage (tolerates 20V-30V)
- PCI bus via mPCI connector
- UPS: capacitor-based or Pb-battery
- sizet: 102 mm x 147 mm

2.2 Specifications and Documents

In making this manual and for further reading of technical documentation, the following documents, specifications and web-pages were used and are recommended.

- PCI Specification
  Version 2.3 resp. 3.0
  www.pcisig.com
- ACPI Specification
  Version 3.0
  www.acpi.info
- ATA/ATAPI Specification
  Version 7 Rev. 1
  www.t13.org
- USB Specifications
  www.usb.org
- SM-Bus Specification
  Version 2.0
  www.smbus.org
- Intel® Chipset Documentation
  SCH Datasheet
  www.intel.com
- Intel® Chip Documentation
  Atom Datasheet
  www.intel.com
- Winbond® Chip Documentation
  W83627HG
  www.winbond-usa.com oder www.winbond.com.tw
- Intel® Chip Documentation
  82575EB Datasheet
  www.intel.com

3 Detailed Description

3.1 Power Supply / UPS

The CB3053 needs an external power supply of 24V (will tolerate 20V-30V). This input is galvanically isolated from the board's internal circuitry. It is also used for charging any UPS device that may be present. This UPS device is either capacitor-based or connected externally as a Pb-battery pack. With a UPS installed and charged, the module can stay operational even when a power failure occurs. A capacitor-based UPS can keep the board alive only for a few seconds while a Pb-battery typically allows for several minutes of continued operation. The exact amount of time is hard to predict as it also depends on factors such as the UPS' charge level at the time of the power failure, CPU/chipset power consumption etc. Generally, a Pb-battery needs a much longer time to reach full charge level compared to a capacitor-based UPS.

3.2 CPU

The motherboard employs an Intel® Atom™ processor either with 1.1GHz or with 1.6GHz clock speed (Z510/Z530). These are single core CPUs which are optimized for low power consumption while at the same time providing state-of-the-art computing performance.
The processors include a second level cache of 512 KByte. They also offer many features known from the desktop range such as MMX2, serial number, loadable microcode etc.
The Atom™ CPU is combined with the SCH US15W chipset. The power consumption of these two components never exceeds 5 watts combined. Therefore, passive cooling solutions will be sufficient for many system configurations.

3.3 Memory

There is one conventional SO-DIMM200 socket available to equip the board with memory. For technical and mechanical reasons it is possible that particular memory modules cannot be employed. Please ask your sales representative for recommended memory modules.
With currently available SO-DIMM200 modules a memory extension up to 2 GByte is possible (DDR2-533).

4 Connectors

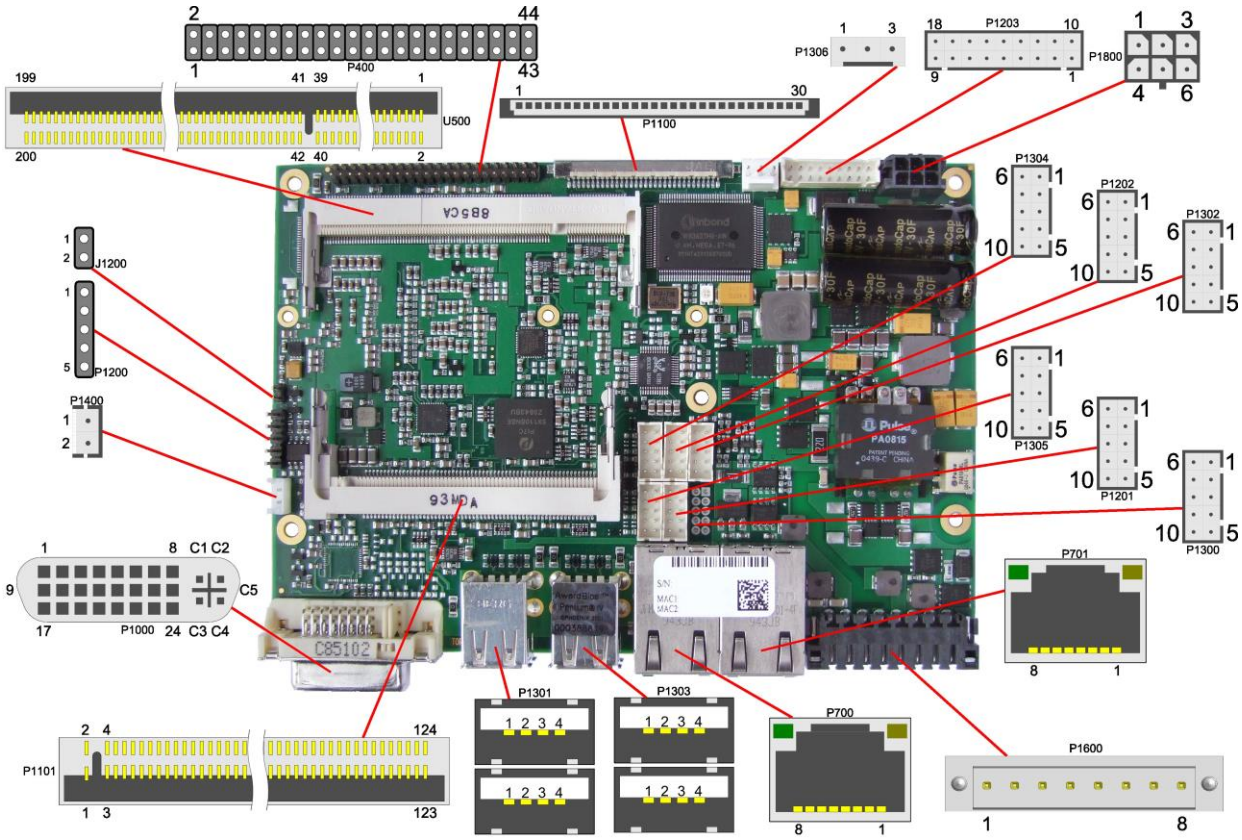
This section describes all the connectors found on the CB3053.

CAUTION

For most interfaces, the cables must meet certain requirements. For instance, USB 2.0 requires twisted and shielded cables to reliably maintain full speed data rates. Restrictions on maximum cable length are also in place for many high speed interfaces and for power supply. Please refer to the respective specifications and use suitable cables at all times.

4.1 Connector Map

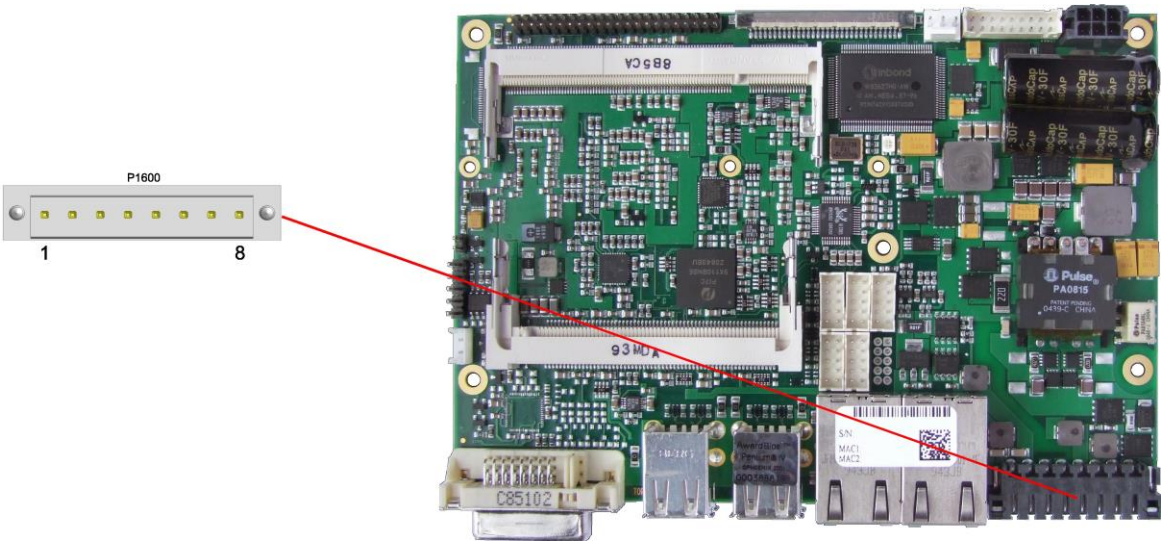
Please use the connector map below for quick reference. Only connectors on the component side are shown. For more information on each connector refer to the table below.



Ref-No.	Function	Page
P400	"IDE Interface"	p. 33
U500	"Memory"	p. 22
P700/1	"LAN"	p. 31
P1000	"DVI"	p. 25
P1100	"LVDS"	p. 26
P1101	"Mini-PCI"	p. 36
P1200	"Touch Screen"	p. 28
J1200	"Touch Screen"	p. 28
P1201	"SMB/I2C"	p. 35
P1202	"Audio"	p. 32
P1203	"System"	p. 20
P1300/2	"Serial Interfaces COM1 and COM2"	p. 34
P1301/3	"USB 1-4"	p. 29
P1304/5	"USB 5-8"	p. 30
P1306	"Fan Connector"	p. 38
P1400	"External CMOS Battery"	p. 21
P1600	"Power Supply"	p. 18
P1800	"Power Connector"	p. 19

4.2 Power Supply

The power supply of the hardware module is realized via an 8pin connector (Weidmüller 180537-0000). The main 24V power lines are assigned to pins 5 and 6. An external Pb-battery can be connected to pins 1 and 2 to provide UPS functionality. Contact your sales person to discuss suitable battery packs.
Pin 3 (UPS_OUT) is a 24V output (max. 2A), which is supported by the UPS (Pb-accu or capacitors) in the event of a power failure. One possible application would be to use this output to supply a display device which would then be able to display information about the power failure and the imminent system shutdown.
If a UPS is present you need to have a possibility to shut down the board in a regular way without activating the UPS, thereby preventing premature aging of UPS components. That's what pin 7 (PC_ON#) is for. When pulled high (24V) a regular shutdown without UPS activity is triggered. As a part of this regular shutdown pins 3 (UPS_OUT) and 8 (Power Status) are pulled from 24V to 0V. Any devices connected to UPS_OUT will thus also be switched off without discharging the UPS.

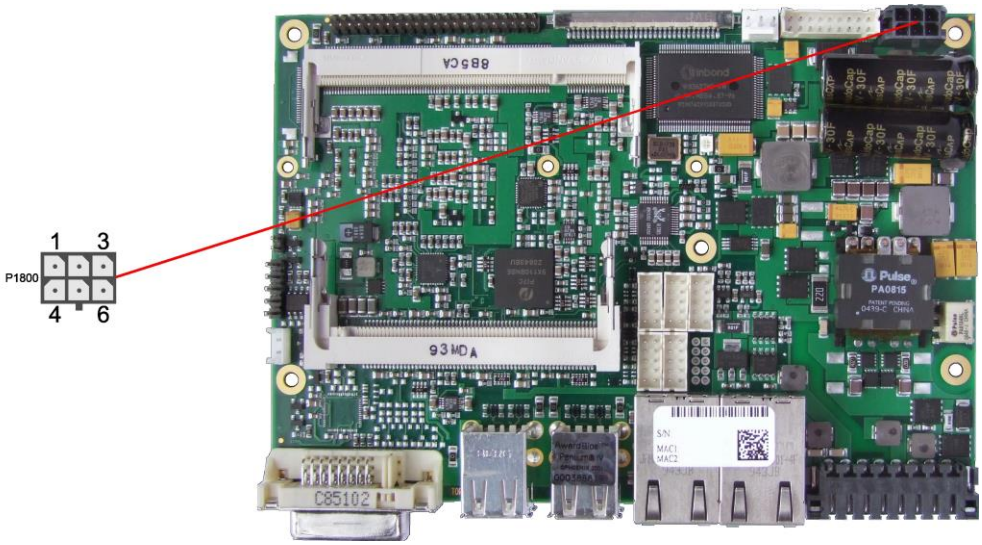


Pinout power connector:

Pin	Name	Description
1	BATT24V#	Pb-accu 24V -
2	BATT24V	Pb-accu 24V +
3	UPS_OUT	UPS outgoing supply 24V
4	GND	ground
5	24V#	power supply 24V -
6	24V	power supply 24V +
7	PC_ON#	power on
8	PWRSTAT	power status

4.3 Power Connector

The board is equipped with a 2x3pin Molex connector offering standard 5V and 12V power supplies for additional peripheral devices. Maximum current is 2 amperes for VCC/SVCC combined, and also 2 amperes for 12V. In the case of a power failure theses supplies are supported by the UPS circuit, but only if the UPS is a Pb-battery. They are not supported if the UPS is capacitor-based.

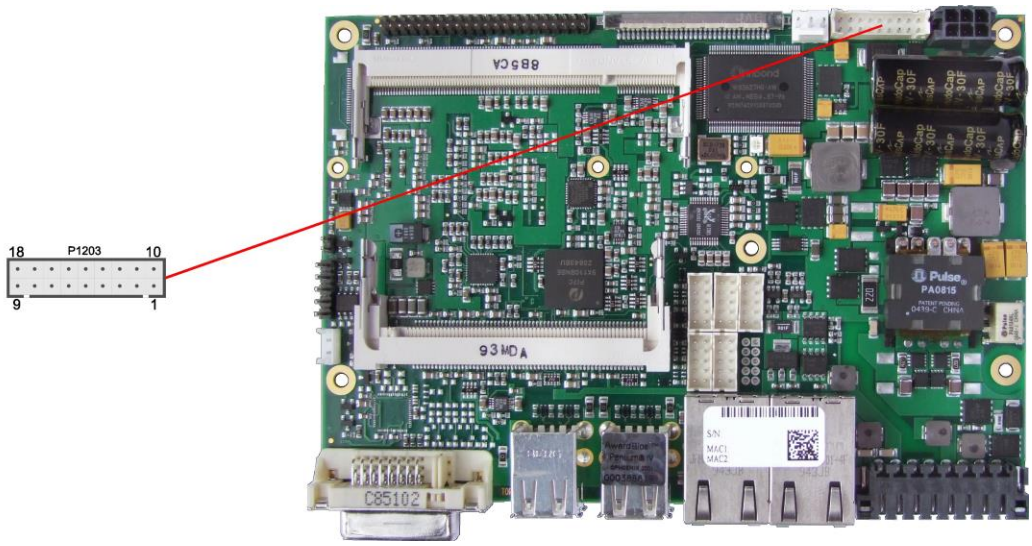


Pinout power connector Molex 2x3:

Description	Name	Pin		Name	Description
ground	GND	1	4	VCC	power supply 5V
reserved	RES	2	5	SVCC	standby supply 5V
reserved	RES	3	6	12V	power supply 12V

4.4 System

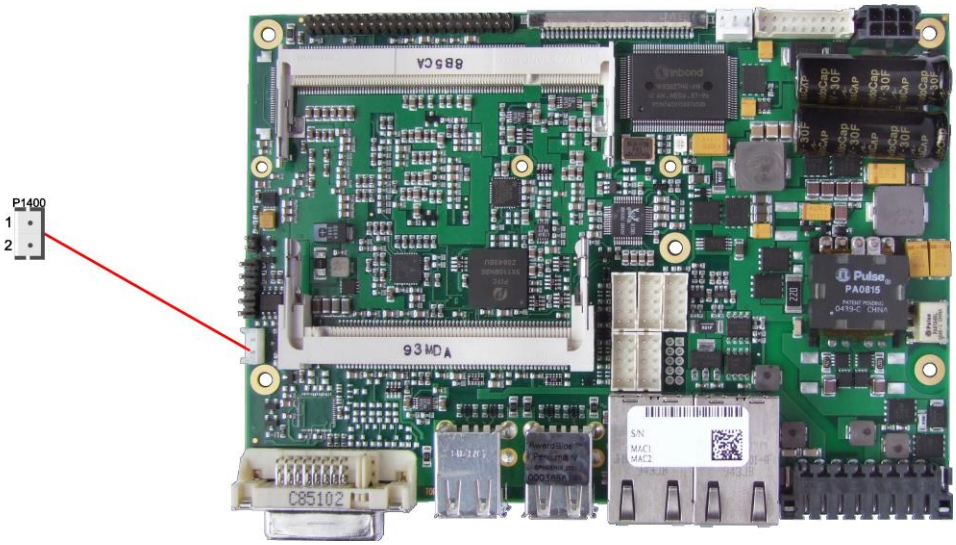
Some typical signals for system control are provided through a 2x9 pin connector (JST B18B-PHDSS, mating connector: PHDR-18VS). This connector combines signals for power button, reset, keyboard, speaker, and several LEDs such as harddisk LED, touch screen LED, suspend LED, and three additional LEDs which are driven by GPIOs. Of these three GPIO-LEDs, LED1 and LED2 are already provided with a series resistor. As can be seen from the pinout table below, corresponding signals are often placed vis-à-vis or at least near to each other.



Description	Name	Pin		Name	Description
ground	GND	1	10	PWRBTN#	on/suspend button
ground	GND	2	11	RESET#	reset to ground
LED touch screen	TOUCHLED	3	12	3.3V	3.3 volt supply
LED suspend / ACPI	S-LED	4	13	S3.3V	standby supply 3.3 volt
LED harddisk	HDLED	5	14	3.3V	3.3 volt supply
LED GPIO device	LED1	6	15	3.3V	3.3 volt supply
LED GPIO device	LED2	7	16	LED3	LED GPIO device
speaker to 5 volt	SPEAKER	8	17	KDAT	keyboard data
standby supply 5 volt	(S)VCC	9	18	KCLK	keyboard clock

4.5 External CMOS Battery

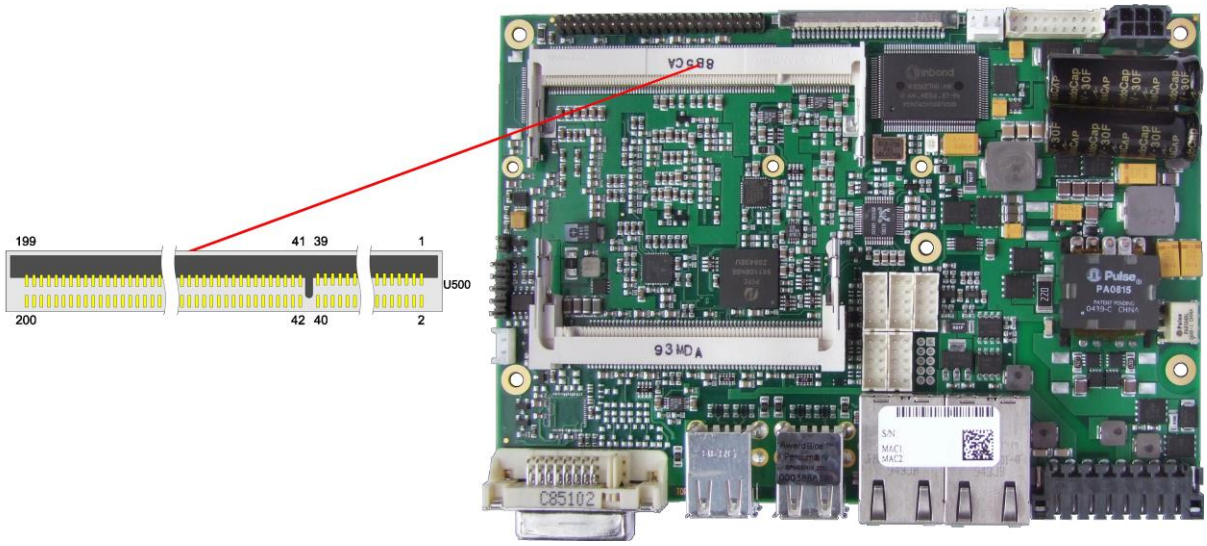
For keeping the internal clock alive even if the rest of the board is switched off, an external battery can be attached via a 2 pin connector (JST B2B-EH-A, mating connector: EHR-2).



Pin	Name	Description
1	BATT	battery 3.3 volt
2	GND	ground

4.6 Memory

Conventional SO-DIMM200 memory modules, as familiar from notebook computers, are used to equip the board with memory. For technical and mechanical reasons it is possible that particular memory modules cannot be employed. Please ask your distributor for recommended memory modules.
With currently available SO-DIMM200 modules a memory extension up to 2 GByte is possible (DDR2-533). All timing parameters for different memory modules are automatically set by BIOS.



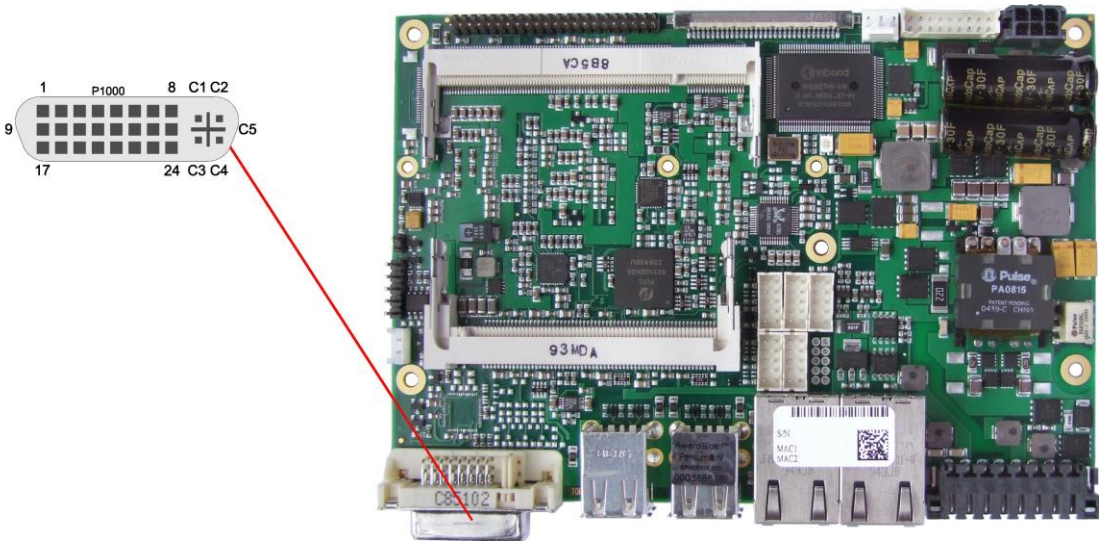
Description	Name	Pin		Name	Description
memory reference current	REF	1	2	GND	ground
ground	GND	3	4	DQ4	data 4
data 0	DQ0	5	6	DQ5	data 5
data 1	DQ1	7	8	GND	ground
ground	GND	9	10	DQM0	data mask 0
data strobe 0 -	DQS0#	11	12	GND	ground
data strobe 0 +	DQS0	13	14	DQ6	data 6
ground	GND	15	16	DQ7	data 7
data 2	DQ2	17	18	GND	ground
data 3	DQ3	19	20	DQ12	data 12
ground	GND	21	22	DQ13	data 13
data 8	DQ8	23	24	GND	ground
data 9	DQ9	25	26	DQM1	data mask 1
ground	GND	27	28	GND	ground
data strobe 1 -	DQS1#	29	30	CK0	clock 0 +
data strobe 1 +	DQS1	31	32	CK0#	clock 0 -
ground	GND	33	34	GND	ground
data 10	DQ10	35	36	DQ14	data 14
data 11	DQ11	37	38	DQ15	data 15
ground	GND	39	40	GND	ground
ground	GND	41	42	GND	ground
data 16	DQ16	43	44	DQ20	data 20
data 17	DQ17	45	46	DQ21	data 21
ground	GND	47	48	GND	ground
data strobe 2 -	DQS2#	49	50	N/C	reserved
data strobe 2 +	DQS2	51	52	DQM2	data mask 2

Description	Name	Pin		Name	Description
ground	GND	53	54	GND	ground
data 18	DQ18	55	56	DQ22	data 22
data 19	DQ19	57	58	DQ23	data 23
ground	GND	59	60	GND	ground
data 24	DQ24	61	62	DQ28	data 28
data 25	DQ25	63	64	DQ29	data 29
ground	GND	65	66	GND	ground
data mask 3	DQM3	67	68	DQS3#	data strobe 3 -
reserved	N/C	69	70	DQS3	data strobe 3 +
ground	GND	71	72	GND	ground
data 26	DQ26	73	74	DQ30	data 30
data 27	DQ27	75	76	DQ31	data 31
ground	GND	77	78	GND	ground
clock enables 0	CKE0	79	80	CKE1	clock enables 1
1.8 volt supply	1.8V	81	82	1.8V	1.8 volt supply
reserved	N/C	83	84	N/C	reserved
SDRAM bank 2	BA2	85	86	N/C	reserved
1.8 volt supply	1.8V	87	88	1.8V	1.8 volt supply
address 12	A12	89	90	A11	address 11
address 9	A9	91	92	A7	address 7
address 8	A8	93	94	A6	address 6
1.8 volt supply	1.8V	95	96	1.8V	1.8 volt supply
address 5	A5	97	98	A4	address 4
address 3	A3	99	100	A12	address 2
address 1	A1	101	102	A0	address 0
1.8 volt supply	1.8V	103	104	1.8V	1.8 volt supply
address 10	A10	105	106	BA1	SDRAM bank 1
SDRAM bank 0	BA0	107	108	RAS#	row address strobe
write enable	WE#	109	110	S0#	chip select 0
1.8 volt supply	1.8V	111	112	1.8V	1.8 volt supply
column address strobe	CAS#	113	114	ODT0	on die termination 0
chip select 1	S1#	115	116	A13	address 13
1.8 volt supply	1.8V	117	118	1.8V	1.8 volt supply
on die termination 1	ODT1	119	120	N/C	reserved
ground	GND	121	122	GND	ground
data 32	DQ32	123	124	DQ36	data 36
data 33	DQ33	125	126	DQ37	data 37
ground	GND	127	128	GND	ground
data strobe 4 -	DQS4#	129	130	DQM4	data mask 4
data strobe 4 +	DQS4	131	132	GND	ground
ground	GND	133	134	DQ38	data 38
data 34	DQ34	135	136	DQ39	data 39
data 35	DQ35	137	138	GND	ground
ground	GND	139	140	DQ44	data 44
data 40	DQ40	141	142	DQ45	data 45
data 41	DQ41	143	144	GND	ground
ground	GND	145	146	DQS5#	data strobe 5 -
data mask 5	DQM5	147	148	DQS5	data strobe 5 +
ground	GND	149	150	GND	ground
data 42	DQ42	151	152	DQ46	data 46
data 43	DQ43	153	154	DQ47	data 47
ground	GND	155	156	GND	ground
data 48	DQ48	157	158	DQ52	data 52
data 49	DQ49	159	160	DQ53	data 53
ground	GND	161	162	GND	ground

Description	Name	Pin		Name	Description
test	TEST	163	164	CK1	clock 1 +
ground	GND	165	166	CK1#	clock 1 -
data strobe 6 -	DQS6#	167	168	GND	ground
data strobe 6	DQS6	169	170	DQM6	data mask 6
ground	GND	171	172	GND	ground
data 50	DQ50	173	174	DQ54	data 54
data 51	DQ51	175	176	DQ55	data 55
ground	GND	177	178	GND	ground
data 56	DQ56	179	180	DQ60	data 60
data 57	DQ57	181	182	DQ61	data 61
ground	GND	183	184	GND	ground
data mask 7	DQM7	185	186	DQS7#	data strobe 7 -
ground	GND	187	188	DQS7	data strobe 7 +
data 58	DQ58	189	190	GND	ground
data 59	DQ59	191	192	DQ62	data 62
ground	GND	193	194	DQ63	data 63
SMBus data	SDA	195	196	GND	ground
SMBus clock	SCL	197	198	SA0	SPD address
3.3 volt supply	3.3V	199	200	SA1	SPD address

4.7 DVI

The CB3053 is connected to an external display via a DVI-D connector. Only digital displays are supported. RGB-pins (C1-C4 and pin 8) are not connected.

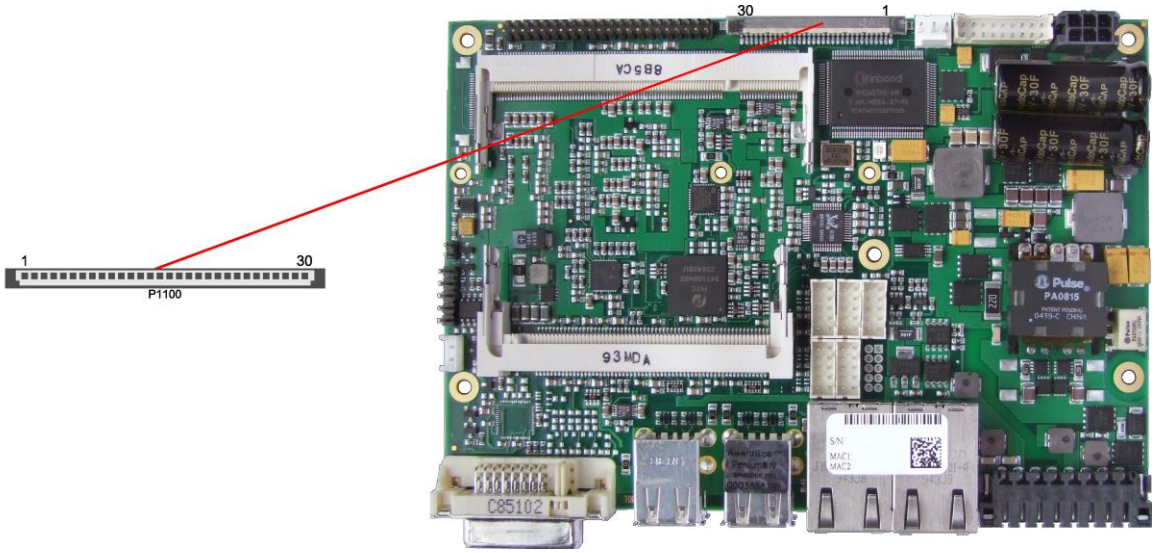


Pinout DVI-D:

Pin	Name	Description
1	TMDSDAT2#	DVI data 2 -
2	TMDSDAT2	DVI data 2 +
3	GND	ground
4	N/C	reserved
5	N/C	reserved
6	DDC CLK	DDC clock (DVI/VGA)
7	DDC DAT	DDC data (DVI/VGA)
8	N/C	reserved
9	TMDSDAT1#	DVI data 1 -
10	TMDSDAT1	DVI data 1 +
11	GND	ground
12	N/C	reserved
13	N/C	reserved
14	VCC	5 volt supply
15	GND	ground
16	HP_DETECT	hot plug detect
17	TMDSDAT0#	DVI data 0 -
18	TMDSDAT0	DVI data 0 +
19	GND	ground
20	N/C	reserved
21	N/C	reserved
22	GND	ground
23	TMDS CLK	DVI clock +
24	TMDS CLK#	DVI clock -
C1	N/C	reserved
C2	N/C	reserved
C3	N/C	reserved
C4	N/C	reserved
C5	GND	ground

4.8 LVDS

The board also offers the possibility to use displays with LVDS interface. These can be connected via a 30 pin flat-cable plug (JAE FI-X30S-HF-NPB, mating connector: FI-X30C(2)-NPB). Only shielded and twisted cables may be used. The display type is to be chosen over the BIOS setup. The connector has two additional shield pins S1 and S2 which are omitted in the pinout table below.



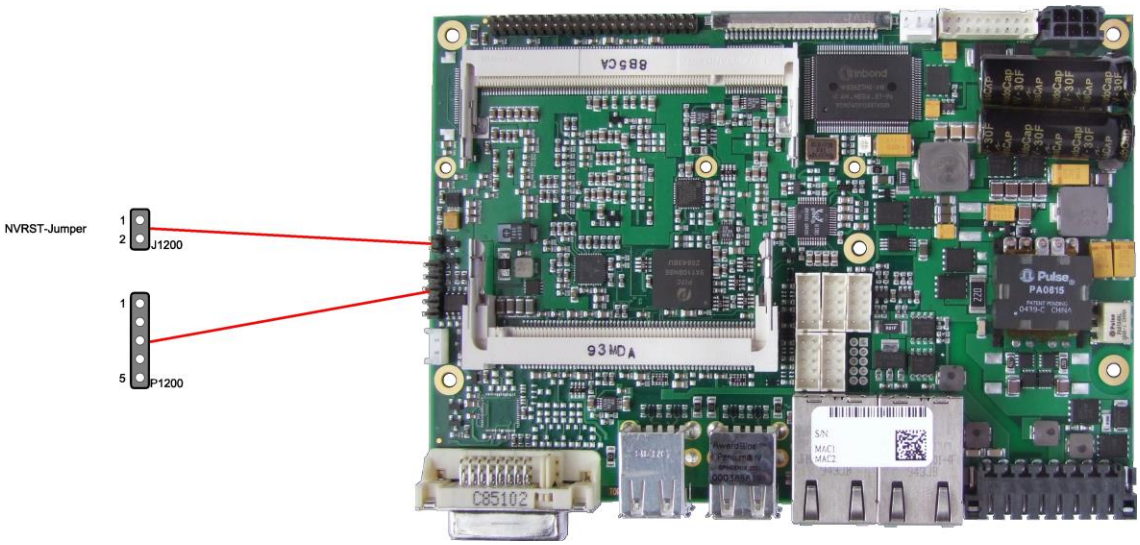
Pinout LVDS connector:

Pin	Name	Description
1	TXO00#	LVDS even data 0 -
2	TXO00	LVDS even data 0 +
3	TXO01#	LVDS even data 1 -
4	TXO01	LVDS even data 1 +
5	TXO02#	LVDS even data 2 -
6	TXO02	LVDS even data 2 +
7	GND	ground
8	TXO0C#	LVDS even clock -
9	TXO0C	LVDS even clock +
10	TXO03#	LVDS even data 3 -
11	TXO03	LVDS even data 3 +
12	N/C	reserved
13	N/C	reserved
14	GND	ground
15	N/C	reserved
16	N/C	reserved
17	GND	ground
18	N/C	reserved
19	N/C	reserved
20	N/C	reserved
21	N/C	reserved
22	N/C	reserved
23	N/C	reserved
24	GND	ground
25	3.3V	3.3 volt supply
26	DDC_CLK	EDID clock for LCD

Pin	Name	Description
27	DDC_DAT	EDID data for LCD
28	FP_3.3V	switched 3.3 volt for display
29	FP_BL	switched 5 volt for backlight
30	VCC	5 volt supply

4.9 Touch Screen

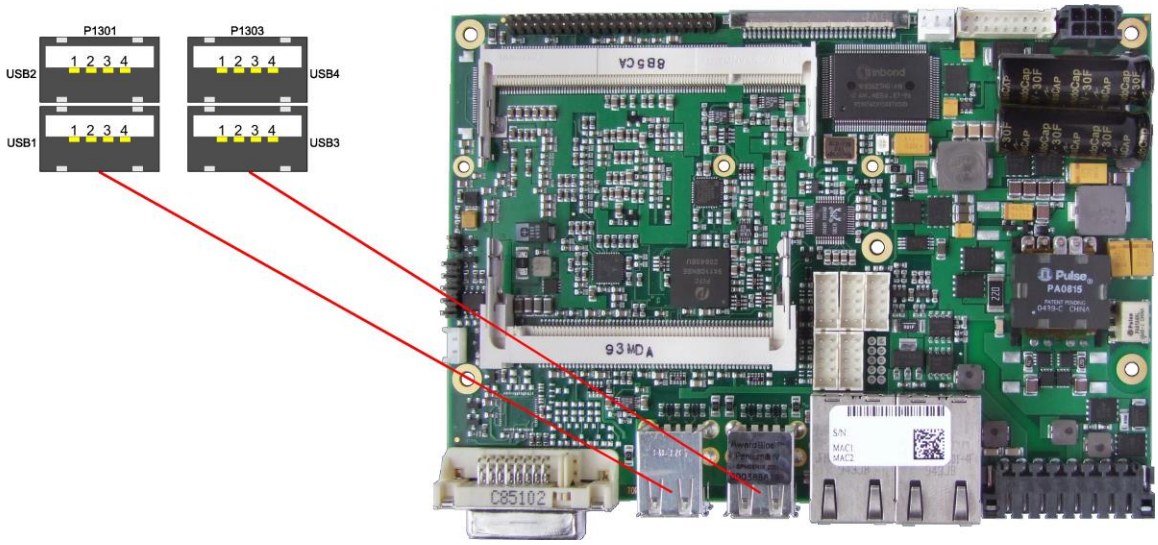
A key feature of the CB3053 is the possibility to connect a touch screen. Both 4-wire and 5-wire resistive touch screens are supported. For receiving the relevant signals a 5 pin standard IDC socket connector with a spacing of 2.54 mm is provided. If the connected touch screen is 4-wire then pin 1 will not be used. There is an accompanying jumper which, if shorted at boot time, triggers the NVRST-signal in the controller, thereby resetting all parameters of NVRAM to default values.
Conversion to the respective connector of the touch screen must be provided externally. Please consult the manufacturer's documentation to figure out the relevant technical details.
Note: In the pinout table below H, X, S, Y, and L are the signal names in the case of 5-wire, XL, XR, YT, and YB are the names in the case of 4-wire.



Pin	Name	Description
1	H-DRV	H driver control
2	X/XL-DRV	X/XL driver control
3	S/XR-DRV	S/XR driver control
4	Y/YT-DRV	Y/YT driver control
5	L/YB-DRV	L/YB driver control

4.10 USB 1-4

The USB channels 1 to 4 are available as standard USB connectors.
The USB channels support USB 2.0. You may note that the setting of USB keyboard or USB mouse support in the BIOS-setup is only necessary and advisable, if the OS offers no USB-support. BIOS-setup can be changed with a USB keyboard without enabling USB keyboard support. Running Windows with these features enabled may lead to significant performance or functionality limitations.
Every USB interface provides up to 500 mA current and is protected by an electronically resettable fuse.

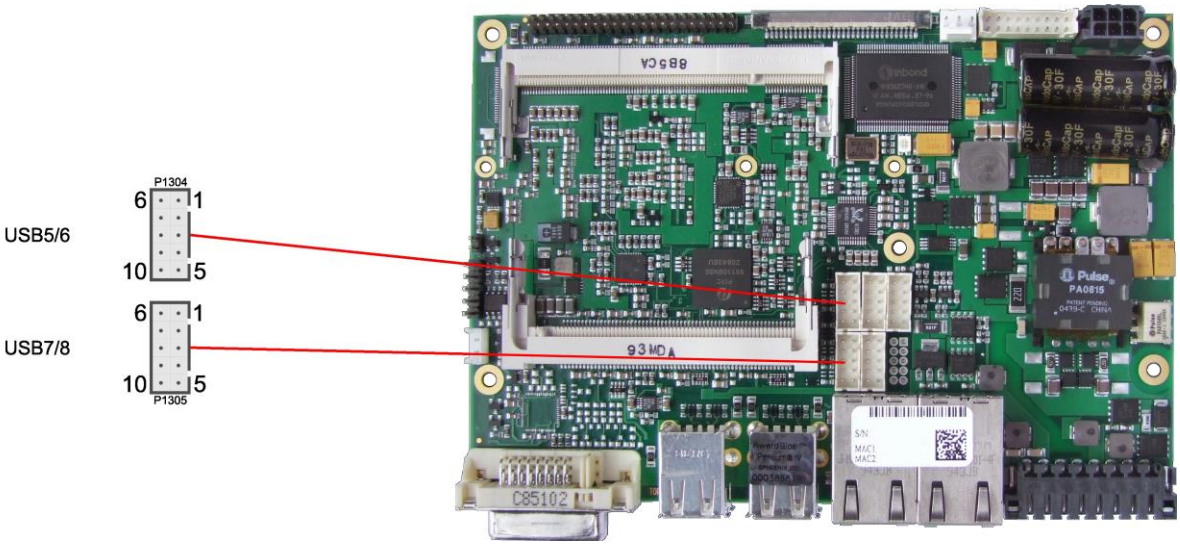


Pinout USB connector for channel X:

Pin	Name	Description
1	VCC	5 volt for USBX
2	USBX#	minus channel USBX
3	USBX	plus channel USBX
4	GND	ground

4.11 USB 5-8

The USB channels 5 to 8 are provided via two 2x5 pin connectors (JST B10B-PHDSSLFSN, mating connector: PHDR-10VS).
The USB channels support USB 2.0. You may note that the setting of USB keyboard or USB mouse support in the BIOS-setup is only necessary and advisable, if the OS offers no USB-support. BIOS-setup can be changed with a USB keyboard without enabling USB keyboard support. Running Windows with these features enabled may lead to significant performance or functionality limitations.
Every USB interface provides up to 500 mA current and is protected by an electronically resettable fuse.



Pinout 2x5 pin connector USB 5/6

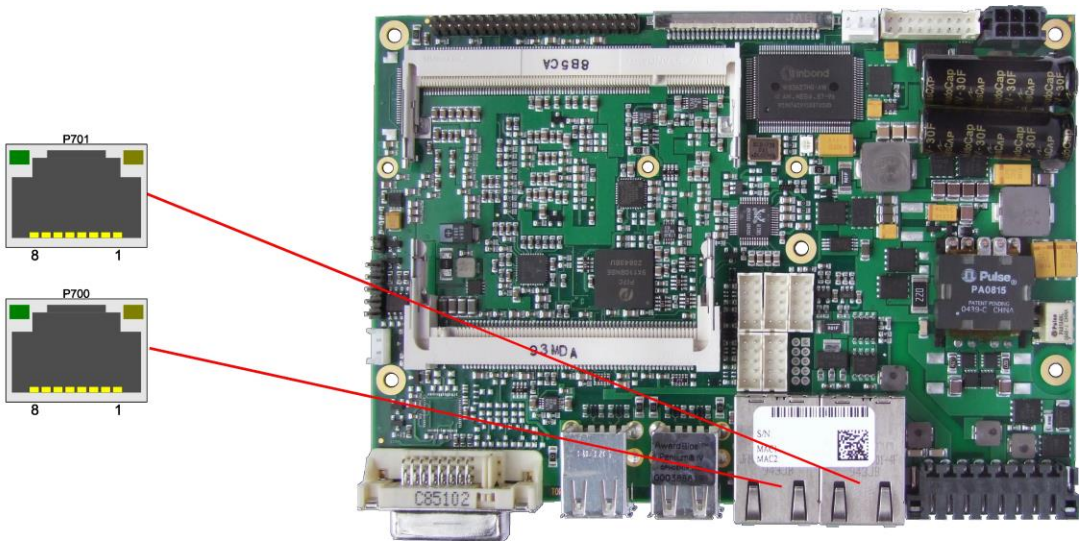
Description	Name	Pin		Name	Description
5 volt for USB5	VCC	1	6	VCC	5 volt for USB6
minus channel USB5	USB5#	2	7	USB6#	minus channel USB6
plus channel USB5	USB5	3	8	USB6	plus channel USB6
ground	GND	4	9	GND	ground
reserved	N/C	5	10	N/C	reserved

Pinout 2x5 pin connector USB 7/8

Description	Name	Pin		Name	Description
5 volt for USB7	VCC	1	6	VCC	5 volt for USB8
minus channel USB7	USB7#	2	7	USB8#	minus channel USB8
plus channel USB7	USB7	3	8	USB8	plus channel USB8
ground	GND	4	9	GND	ground
reserved	N/C	5	10	N/C	reserved

4.12 LAN

The module has two LAN interfaces both of which support 10BaseT, 100BaseT, and 1000BaseT compatible net components with automatic bandwidth selection. The controller chip is the Intel® 82575EB. Auto-cross and auto-negotiate functionality is available as is PXE and RPL.



Pinout LAN 10/100/1000:

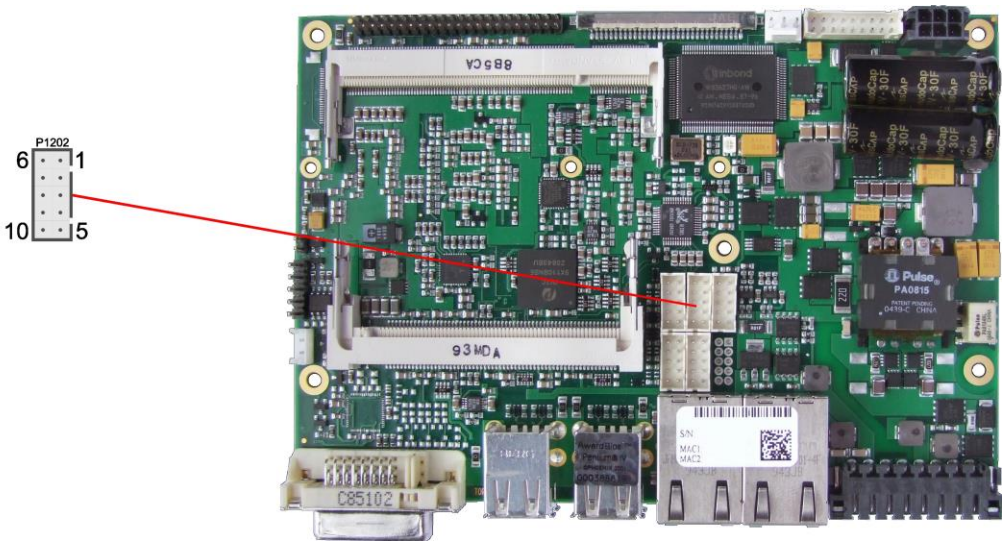
Pin	Name	Description
1	LAN1-0	LAN1 channel 0 plus
2	LAN1-0#	LAN1 channel 0 minus
3	LAN1-1	LAN1 channel 1 plus
4	LAN1-1#	LAN1 channel 1 minus
5	LAN1-2	LAN1 channel 2 plus
6	LAN1-2#	LAN1 channel 2 minus
7	LAN1-3	LAN1 channel 3 plus
8	LAN1-3#	LAN1 channel 3 minus

Pinout LAN 10/100/1000:

Pin	Name	Description
1	LAN2-0	LAN2 channel 0 plus
2	LAN2-0#	LAN2 channel 0 minus
3	LAN2-1	LAN2 channel 1 plus
4	LAN2-2	LAN2 channel 2 plus
5	LAN2-2#	LAN2 channel 2 minus
6	LAN2-1#	LAN2 channel 1 minus
7	LAN2-3	LAN2 channel 3 plus
8	LAN2-3#	LAN2 channel 3 minus

4.13 Audio

Audio input and output functions can be accessed via a 2x5 pin connector (JST B10B-PHDSSLFSN, mating connector: PHDR-10VS). There are two ways to use this connector. Default functionality is the familiar audio in, audio out, and microphone. OS dependent device drivers can switch these signals to support a 5.1 output; thus in this mode no audio input signals are available.
Signals "SPDIFI" and "SPDIFO" provide digital input and output. If a transformation to a coaxial or optical connector is necessary this must be performed externally.



Pinout audio 2x5 pin connector:

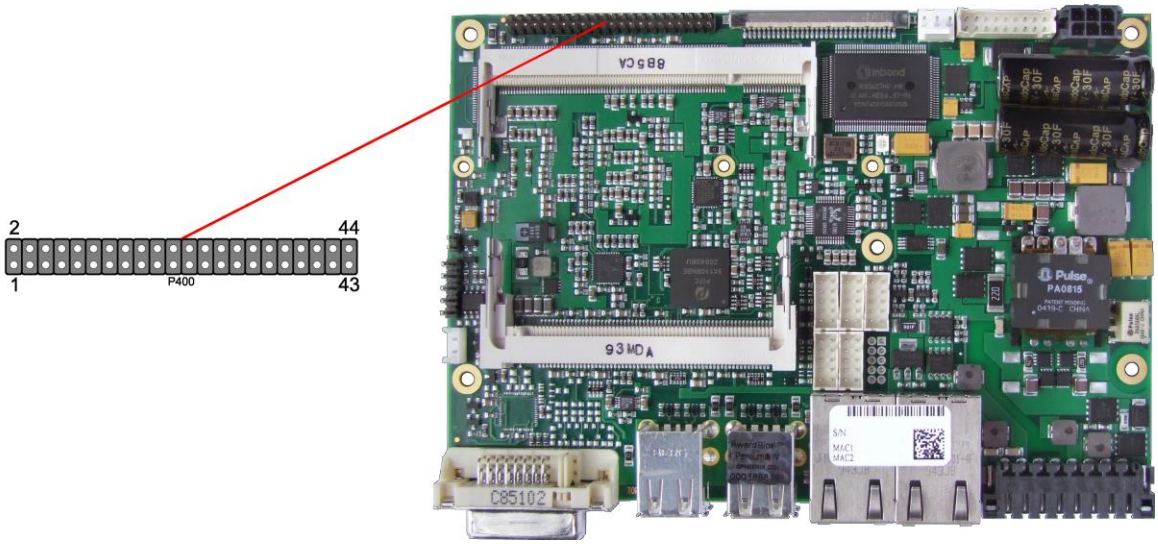
Description	Name	Pin		Name	Description
digital output SPDIF	SPDIFO	1	6	3.3V	3.3 volt supply
digital input SPDIF	SPDIFI	2	7	S_AGND	analog ground sound
sound output right / front output right	LOUT_R / FRONT_R	3	8	LOUT_L / FRONT_L	sound output left / front output left
AUX input right / rear output right	AUXA_R / REAR_R	4	9	AUXA_L / REAR_L	AUX input left / rear output left
microphone input 1 / center output	MIC1 / CENTER	5	10	MIC2 / LFE	microphone input 2 / LFE output

4.14 IDE Interface

The primary IDE interface is a standard IDC socket connector with a spacing of 2 mm. All commercial IDE devices are supported but an adapter to connect may be necessary.
The required settings are made in the BIOS setup.

CAUTION

Pins are not keyed! Please be sure to connect the cable properly, otherwise you risk damaging the IDE interface, the CPU and the drive, voiding respective warranties.

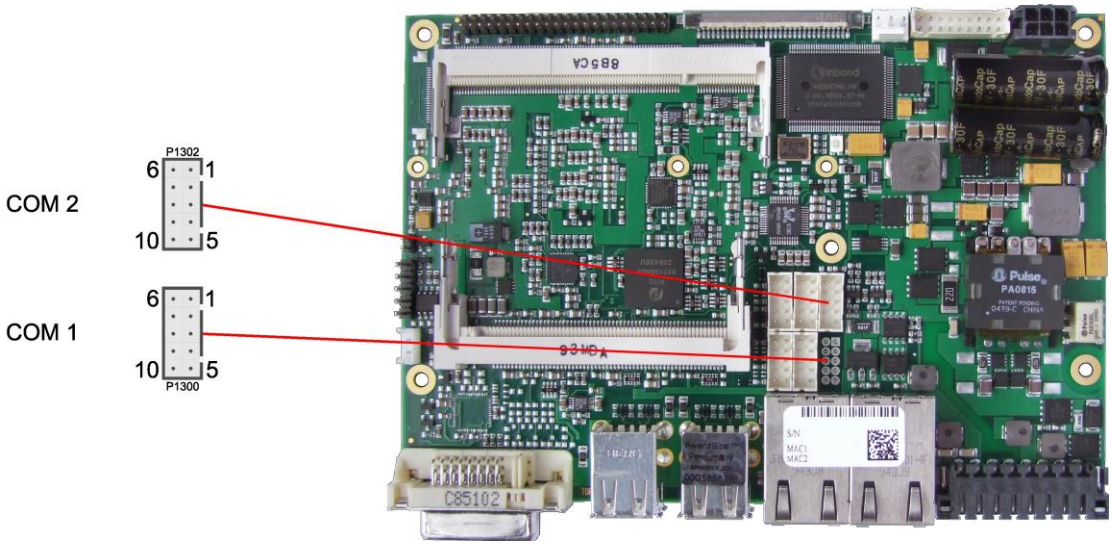


Pinout for primary IDE

Description	Name	Pin		Name	Description
reset	PRST#	1	2	GND	ground
data bit 7	PDD7	3	4	PDD8	data bit 8
data bit 6	PDD6	5	6	PDD9	data bit 9
data bit 5	PDD5	7	8	PDD10	data bit 10
data bit 4	PDD4	9	10	PDD11	data bit 11
data bit 3	PDD3	11	12	PDD12	data bit 12
data bit 2	PDD2	13	14	PDD13	data bit 13
data bit 1	PDD1	15	16	PDD14	data bit 14
data bit 0	PDD0	17	18	PDD15	data bit 15
ground	GND	19	20	N/C	reserved
DMA request signal	PDDREQ	21	22	GND	ground
write signal	PDIOW#	23	24	GND	ground
read signal	PDIOR#	25	26	GND	ground
ready signal	PDRDY	27	28	N/C	reserved
DMA acknowledge signal	PDDACK#	29	30	GND	ground
interrupt signal	PDIRQ	31	32	N/C	reserved
address bit 1	PDA1	33	34	PDMA66EN	enable UDMA66
address bit 0	PDA0	35	36	PDA2	address bit 2
chip select signal 0	PDSC0#	37	38	PDCS1#	chip select signal 1
LED	PHDLED	39	40	GND	ground
supply HDD 5V	VCC	41	42	VCC	supply HDD 5V
ground	GND	43	44	N/C	reserved

4.15 Serial Interfaces COM1 and COM2

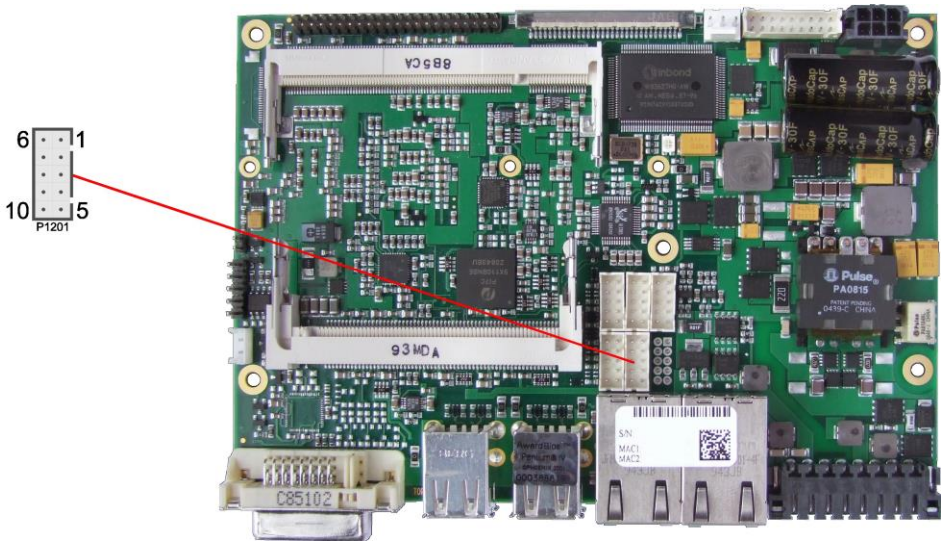
The CB3053 offers two serial interfaces COM1 and COM2, which are made available as 2x5pin connectors (JST B10B-PHDSSLFSN, mating connector: PHDR-10VS). On some board variants COM1 is being used internally so that these boards only have COM2 externally available. Signals default to RS232.
The port address and the interrupt are set via the BIOS setup.



Description	Name	Pin		Name	Description
data carrier detect	DCD	1	6	DSR	data set ready
receive data	RXD	2	7	RTS	request to send
transmit data	TXD	3	8	CTS	clear to send
data terminal ready	DTR	4	9	RI	ring indicator
ground	GND	5	10	VCC	5 volt supply

4.16 SMB/I2C

The CB3053 can communicate with external devices via the SMBus protocol or the I2C protocol. The signals for these protocols are available through a 2x5 pin connector (JST® B10B-PHDSSLFSN, mating connector: PHDR-10VS). The SMBus signals are processed by the SCH chip (Intel® US15W), the I2C signals are processed by the SIO1 unit (Winbond® W83627).

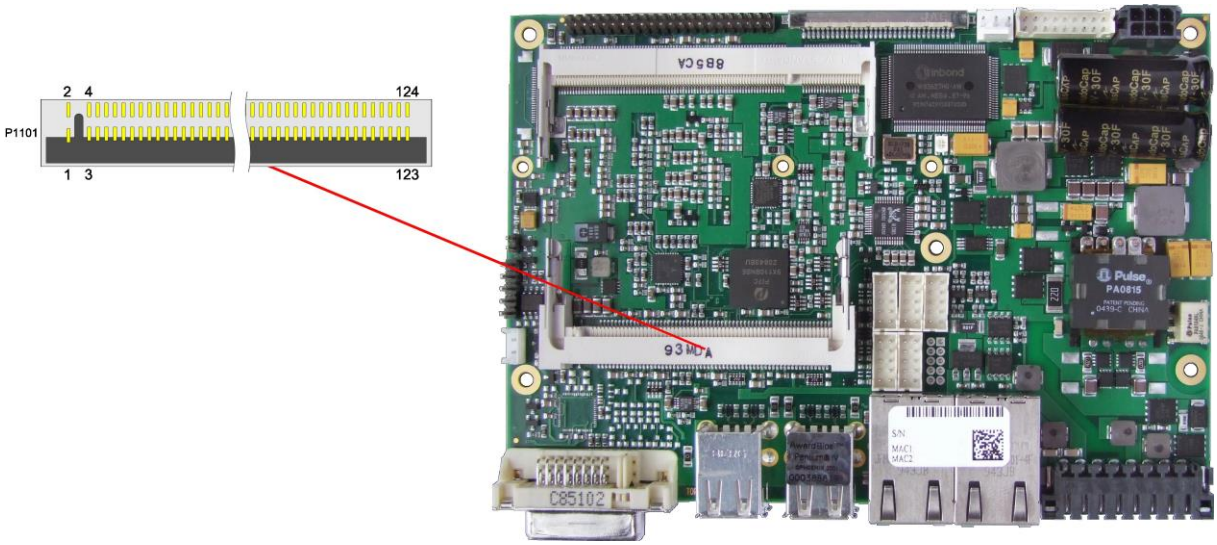


Pinout SMBus/I2C connector:

Description	Name	Pin		Name	Description
3.3 volt supply	3.3V	1	6	GND	ground
SMBus clock	SMBCLK	2	7	SMBDAT	SMBus data
SMBus alarm	SMBALRT#	3	8	SVCC	standby supply 5V
I2C bus clock	I2CLK	4	9	I2DAT	I2C bus data
5 volt supply	VCC	5	10	GND	ground

4.17 Mini-PCI

The CB3053 allows you to add expansion cards complying to the Mini-PCI standard (type III). One such card can be inserted into the Mini-PCI slot available on the board.

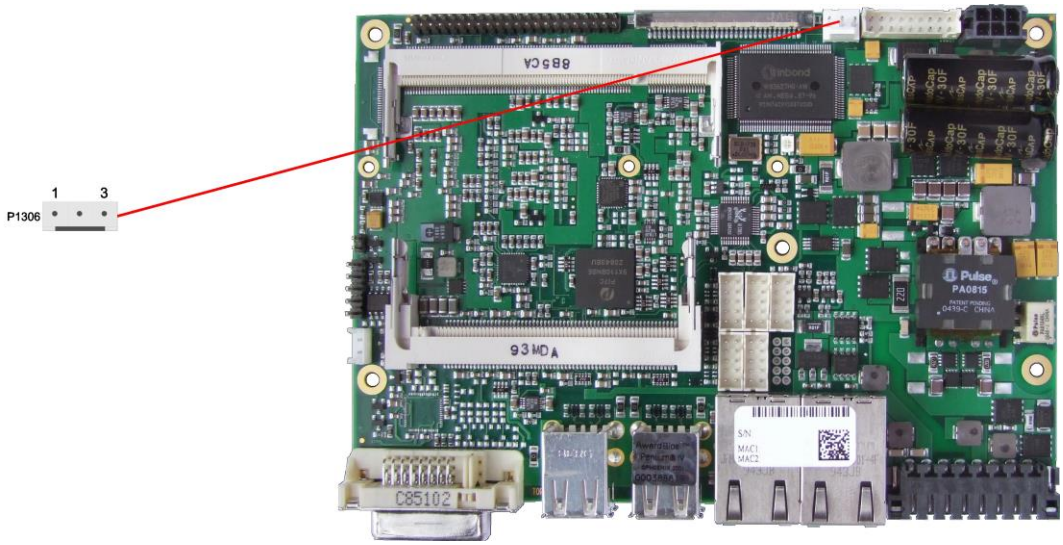


Description	Name	Pin		Name	Description
reserved	N/C	1	2	N/C	reserved
reserved	N/C	3	4	N/C	reserved
reserved	N/C	5	6	N/C	reserved
reserved	N/C	7	8	N/C	reserved
reserved	N/C	9	10	N/C	reserved
reserved	N/C	11	12	N/C	reserved
reserved	N/C	13	14	N/C	reserved
reserved	N/C	15	16	N/C	reserved
interrupt B	INTB#	17	18	VCC	5 volt supply
3.3 volt supply	3.3V	19	20	INTA#	interrupt A
serial interrupt (legacy)	SERIRQ	21	22	N/C	reserved
ground	GND	23	24	S3.3V	3.3 volt supply
PCI clock	PCLK	25	26	PRST#	reset
ground	GND	27	28	3.3V	3.3 volt supply
PCI request	REQ#	29	30	GNT#	PCI grant
3.3 volt supply	3.3V	31	32	GND	ground
address/data 31	AD31	33	34	PME#	power management event
address/data 29	AD29	35	36	N/C	reserved
ground	GND	37	38	AD30	address/data 30
address/data 27	AD27	39	40	3.3V	3.3 volt supply
address/data 25	AD25	41	42	AD28	address/data 28
interrupt C	INTC#	43	44	AD26	address/data 26
bus cmd/byte enables 3	CBE3#	45	46	AD24	address/data 24
address/data 23	AD23	47	48	IDSEL	init device select
ground	GND	49	50	GND	ground
address/data 21	AD21	51	52	AD22	address/data 22
address/data 19	AD19	53	54	AD20	address/data 20
ground	GND	55	56	PAR	parity
address/data 17	AD17	57	58	AD18	address/data 18

Description	Name	Pin		Name	Description
bus cmd/byte enables 2	CBE2#	59	60	AD16	address/data 16
initiator ready	IRDY#	61	62	GND	ground
3.3 volt supply	3.3V	63	64	FRAME#	cycle frame
clock running	CLKRUN#	65	66	TRDY#	target ready
system error	SERR#	67	68	STOP#	stop request by target
ground	GND	69	70	3.3V	3.3 volt supply
parity error	PERR#	71	72	DEVSEL#	device select
bus cmd/byte enables 1	CBE1#	73	74	GND	ground
address/data 14	AD14	75	76	AD15	address/data 15
ground	GND	77	78	AD13	address/data 13
address/data 12	AD12	79	80	AD11	address/data 11
address/data 10	AD10	81	82	GND	ground
ground	GND	83	84	AD9	address/data 9
address/data 8	AD8	85	86	CBE0#	bus cmd/byte enables 0
address/data 7	AD7	87	88	3.3V	3.3 volt supply
3.3 volt supply	3.3V	89	90	AD6	address/data 6
address/data 5	AD5	91	92	AD4	address/data 4
interrupt D	INTD#	93	94	AD2	address/data 2
address/data 3	AD3	95	96	AD0	address/data 0
5 volt supply	VCC	97	98	N/C	reserved
address/data 1	AD1	99	100	N/C	reserved
ground	GND	101	102	GND	ground
reserved	N/C	103	104	GND	ground
reserved	N/C	105	106	N/C	reserved
reserved	N/C	107	108	N/C	reserved
reserved	N/C	109	110	N/C	reserved
reserved	N/C	111	112	N/C	reserved
reserved	N/C	113	114	GND	ground
reserved	N/C	115	116	N/C	reserved
reserved	N/C	117	118	N/C	reserved
reserved	N/C	119	120	N/C	reserved
lock	PLOCK#	121	122	N/C	reserved
reserved	N/C	123	124	S3.3V	3.3 volt supply

4.18 Fan Connector

A 3 pin connector is available for controlling and monitoring an external fan (12 volt). For the monitoring the fan must provide a corresponding speed signal.



Pinout fan connector:

Pin	Name	Description
1	GND	ground
2	12V	12 volt supply regulated
3	TACHO	fan monitoring signal

5 BIOS Settings

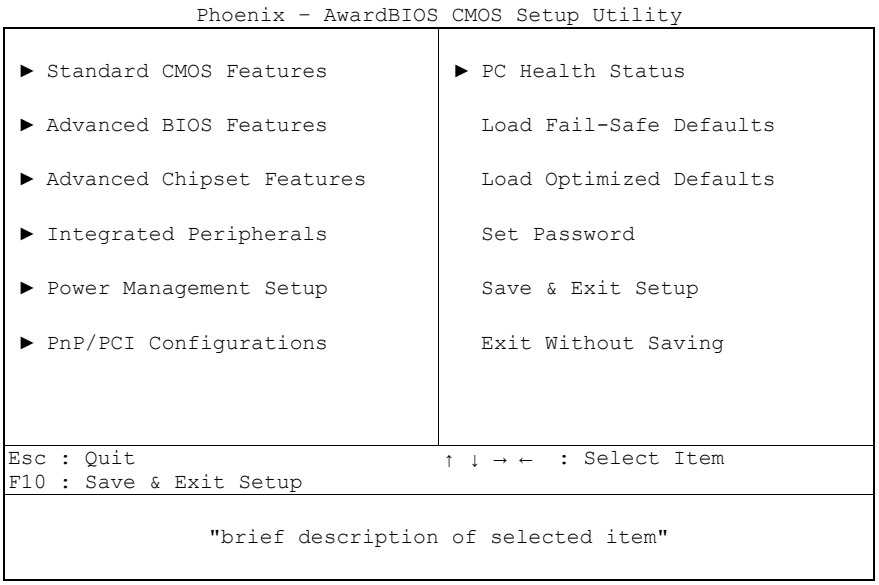
5.1 Remarks for Setup Use

In a setup page, standard values for its setup entries can be loaded. Fail-safe defaults are loaded with F6 and optimized defaults are loaded with F7. These standard values are independent of the fact that a board has successfully booted with a setup setting before.
This is different if these defaults are called from the Top Menu. Once a setup setting was saved, which subsequently leads to a successful boot process, those values are loaded as default for all setup items afterwards.
See also the chapters “Load Fail-Safe Defaults" (5.10) and “Load Optimized Defaults” (5.11).

NOTE

BIOS features and setup options are subject to change without notice. The settings displayed in the screenshots on the following pages are meant to be examples only. They do not represent the recommended settings or the default settings. Determination of the appropriate settings is dependent upon the particular application scenario in which the board is used.

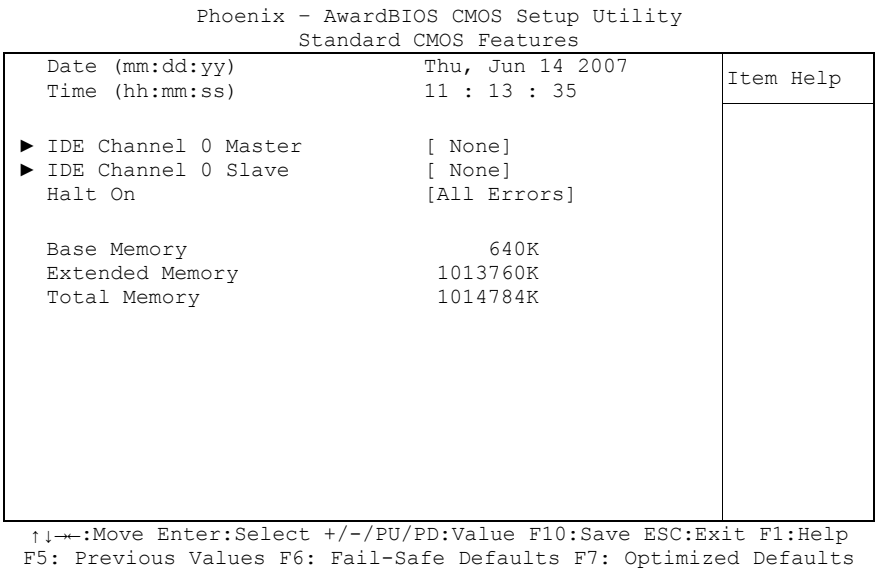
5.2 Top Level Menu



The sign „►“ in front of an item means that there is a sub menu.
The „x“ sign in front of an item means, that the item is disabled but can be enabled by changing or selecting some other item (usually somewhere above the disabled item on the same screen).

Use the arrow buttons to navigate from one item to another. For selecting an item press Enter which will open either a sub menu or a dialog screen.

5.3 Standard CMOS Features



- ✓ **Date (mm:dd:yy)**
  Options: mm: month
  dd: day
  yy: year

- ✓ **Time (hh:mm:ss)**
  Options: hh: hours
  mm: minutes
  ss: seconds

- ✓ **IDE Channel 0 Master**
  Sub menu: see "IDE Channel 0 Master/Slave" (page 41)

- ✓ **IDE Channel 0 Slave**
  Sub menu: see "IDE Channel 0 Master/Slave" (page 41)

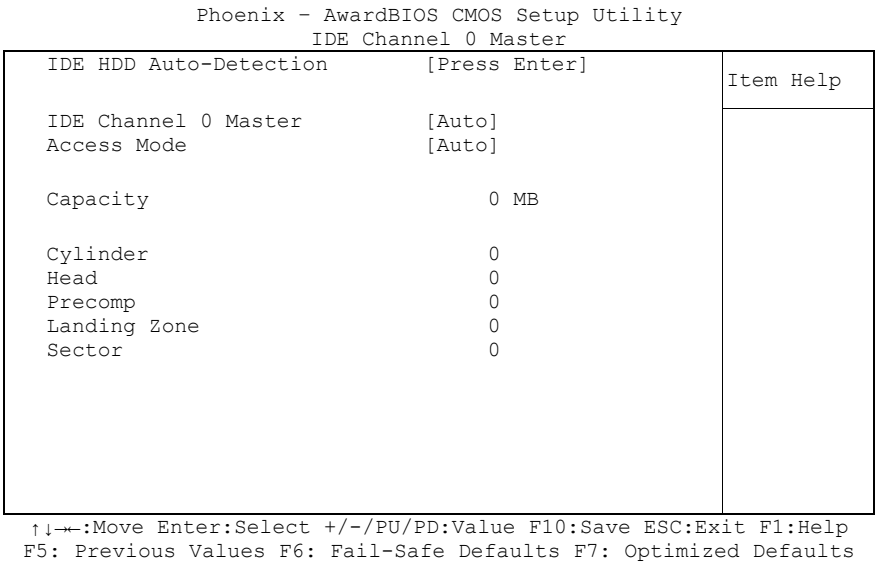
- ✓ **Halt On**
  Options: All Errors / No Errors / All, But Keyboard

- ✓ **Base Memory**
  Options: none

- ✓ **Extended Memory**
  Options: none

- ✓ **Total Memory**
  Options: none

5.3.1 IDE Channel 0 Master/Slave



- ✓ **IDE HDD Auto-Detection**
  Options: none

- ✓ **IDE Channel 0 Master**
  Options: None / Auto / Manual

- ✓ **Access Mode**
  Options: CHS / LBA / Large / Auto

- ✓ **Capacity**
  Options: none

- ✓ **Cylinder**
  Options: none

- ✓ **Head**
  Options: none

- ✓ **Precomp**
  Options: none

- ✓ **Landing Zone**
  Options: none

- ✓ **Sector**
  Options: none

5.4 Advanced BIOS Features

```
                Phoenix – AwardBIOS CMOS Setup Utility
                      Advanced BIOS Features
┌──────────────────────────────────────────────┬──────────────┐
│ ► CPU Feature                 [Press Enter]  │ Item Help    │
│ ► Hard Disk Boot Priority     [Press Enter]  │              │
│   CPU L1 & L2 Cache           [Enabled]      │              │
│   Hyper-Threading Technology   Enabled       │              │
│   Quick Power On Self Test    [Enabled]      │              │
│   First Boot Device           [USB-FDD]      │              │
│   Second Boot Device          [USB-CDROM]    │              │
│   Third Boot Device           [Hard Disk]    │              │
│   Boot Other Device           [Enabled]      │              │
│   Boot Up NumLock Status      [On]           │              │
│   Gate A20 Option             [Fast]         │              │
│   Typematic Rate Setting      [Disabled]     │              │
│ x Typematic Rate (Chars/Sec)   6             │              │
│ x Typematic Delay (Msec)       250           │              │
│   Security Option             [Setup]        │              │
│   APIC Mode                    Enabled       │              │
│   MPS Version Control For OS  [1.4]          │              │
│   OS Select For DRAM > 64MB   [Non-OS2]      │              │
│   HDD S.M.A.R.T. Capability   [Disabled]     │              │
│   Full Screen LOGO Show       [Disabled]     │              │
└──────────────────────────────────────────────┴──────────────┘
  ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- ✓ **CPU Feature**
  Sub menu: see "CPU Feature" (page 44)

- ✓ **Hard Disk Boot Priority**
  Sub menu: see "Hard Disk Boot Priority" (page 45)

- ✓ **CPU L1 & L2 Cache**
  Options: Enabled / Disabled

- ✓ **Hyper-Threading Technology**
  Options: none

- ✓ **Quick Power On Self Test**
  Options: Enabled / Disabled

- ✓ **First Boot Device**
  Options: LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / Legacy LAN / IBA GE Slot 010 / IBA GE Slot 010 / WinCE / Disabled

- ✓ **Second Boot Device**
  Options: LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / Legacy LAN / IBA GE Slot 010 / IBA GE Slot 010 / WinCE / Disabled

- ✓ **Third Boot Device**
  Options: LS120 / Hard Disk / CDROM / ZIP100 / USB-FDD / USB-ZIP / USB-CDROM / Legacy LAN / IBA GE Slot 010 / IBA GE Slot 010 / WinCE / Disabled

- ✓ **Boot Other Device**
  Options: Enabled / Disabled

- ✓ **Boot Up NumLock Status**
  Options: Off / On

- ✓ **Gate A20 Option**
  Options: Normal / Fast

- ✓ **Typematic Rate Setting**
  Options: Enabled / Disabled

- ✓ **Typematic Rate (Chars/Sec)**
  Options: 6 / 8 / 10 / 12 / 15 / 20 / 24 / 30

- ✓ **Typematic Delay (Msec)**
  Options: 250 / 500 / 750 / 1000

- ✓ **Security Option**
  Options: Setup / System

- ✓ **APIC Mode**
  Options: none

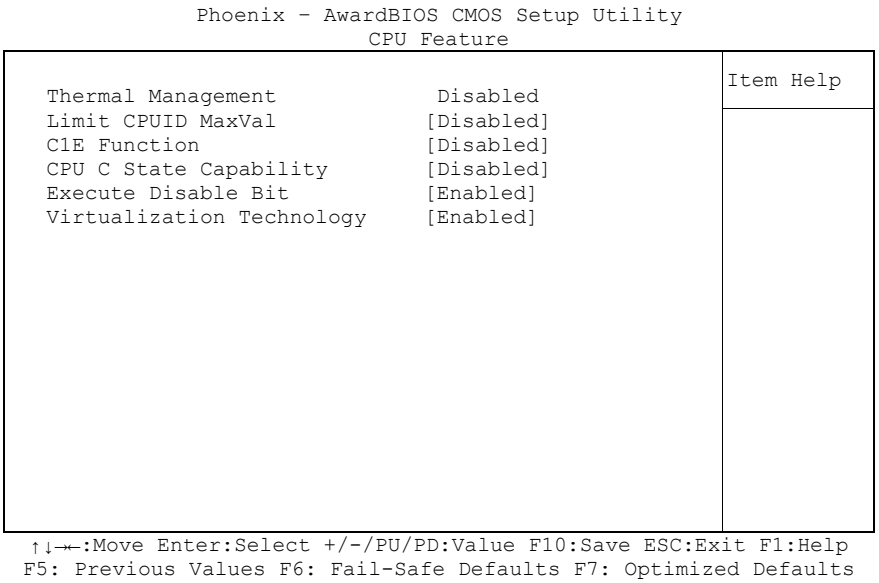
- ✓ **MPS Version Control For OS**
  Options: 1.1 / 1.4

- ✓ **OS Select For DRAM > 64MB**
  Options: Non-OS2 / OS2

- ✓ **HDD S.M.A.R.T. Capability**
  Options: Enabled / Disabled

- ✓ **Full Screen LOGO Show**
  Options: Enabled / Disabled

5.4.1 CPU Feature



- ✓ **Thermal Management**
  Options: none

- ✓ **Limit CPUID MaxVal**
  Options: Enabled / Disabled

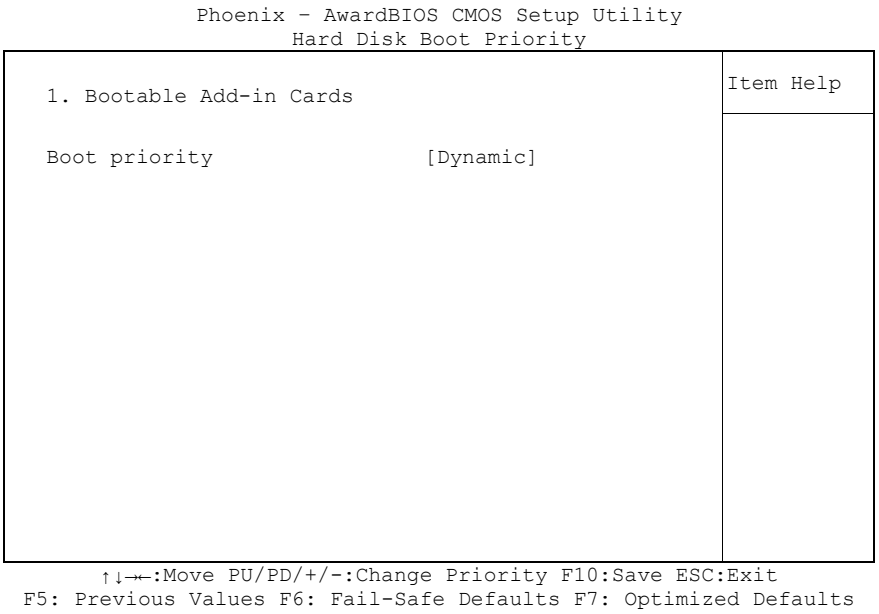
- ✓ **C1E Function**
  Options: Auto / Disabled

- ✓ **CPU C State Capability**
  Options: Disabled / C2 / C4 / C6

- ✓ **Execute Disable Bit**
  Options: Enabled / Disabled

- ✓ **Virtualization Technology**
  Options: Enabled / Disabled

5.4.2 Hard Disk Boot Priority

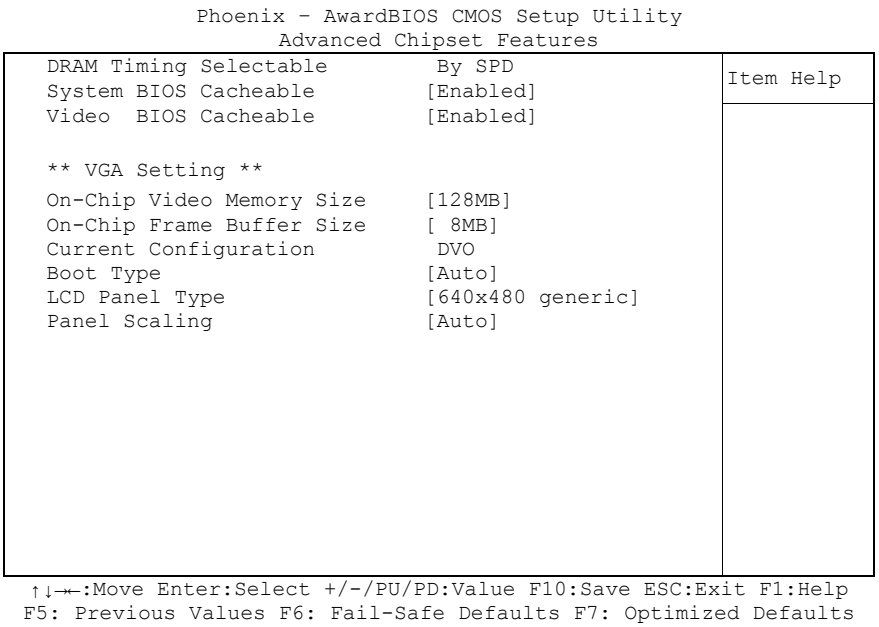


- ✓ **[Liste der verfügbaren Devices]**
  Optionen: bei mehreren bootfähigen HDD-Devices kann hier ausgewählt werden, in welcher Reihenfolge die Devices für einen Bootversuch angesprochen werden sollen.

- ✓ **Achtung!**
  In diesem Untermenü haben die Tasten <Page Up>, <Page Down>, <+> und <-> eine andere Funktion als sonst: Sie dienen dazu, die in der Liste aufgeführten Devices nach oben bzw. unten zu verschieben.

- ✓ **Boot Priority**
  Options: Dynamic / Fixed / Manual

5.5 Advanced Chipset Features



- ✓ **DRAM Timing Selectable**
  Options: none

- ✓ **System BIOS Cacheable**
  Options: Enabled / Disabled

- ✓ **Video BIOS Cacheable**
  Options: Enabled / Disabled

- ✓ **On Chip Video Memory Size**
  Options: 256MB / 128MB

- ✓ **On Chip Frame Buffer Size**
  Options: 1MB / 4MB / 8MB

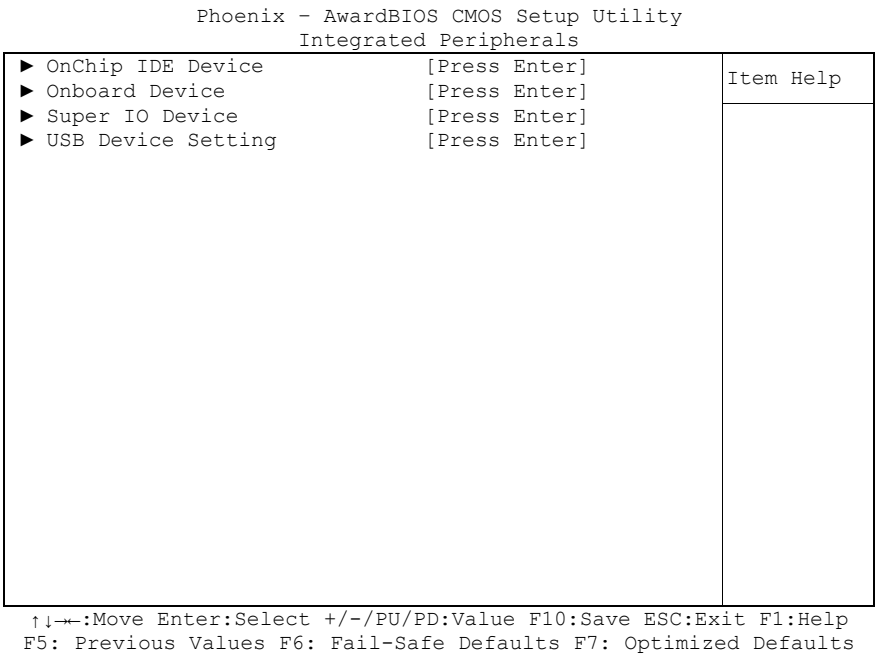
- ✓ **Current Configuration**
  Options: none

- ✓ **Boot Type**
  Options: Auto / LVDS / DVI

- ✓ **LCD Panel Type**
  Options: 640x480 generic / 800x600 generic / 1024x768 generic / 640x480 NEC 8.4" / 800x480 NEC 9" / 1024x600 TMD 5.61" / 1024x600 Samsung 4.8" / 1024x768 Samsung 15" / 1024x768 Sharp 7.2" / 1280x800 Samsung 15.4

- ✓ **Panel Scaling**
  Options: Auto / Force / Off

5.6 Integrated Peripherals



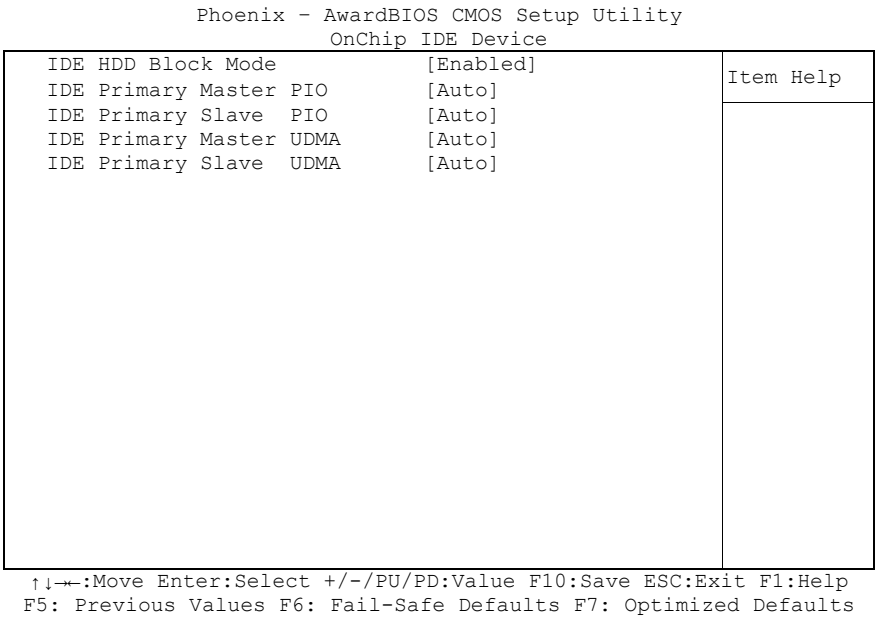
- ✓ **OnChip IDE Device**
  Sub menu: see "OnChip IDE Devices" (page 48)

- ✓ **Onboard Device**
  Sub menu: see "Onboard Devices" (page 49)

- ✓ **SuperIO Device**
  Sub menu: see "SuperIO Devices" (page 50)

- ✓ **USB Device Setting**
  Sub menu: see "USB Device Setting" (page 51)

5.6.1 OnChip IDE Devices



- ✓ **IDE HDD Block Mode**
  Options: Enabled / Disabled

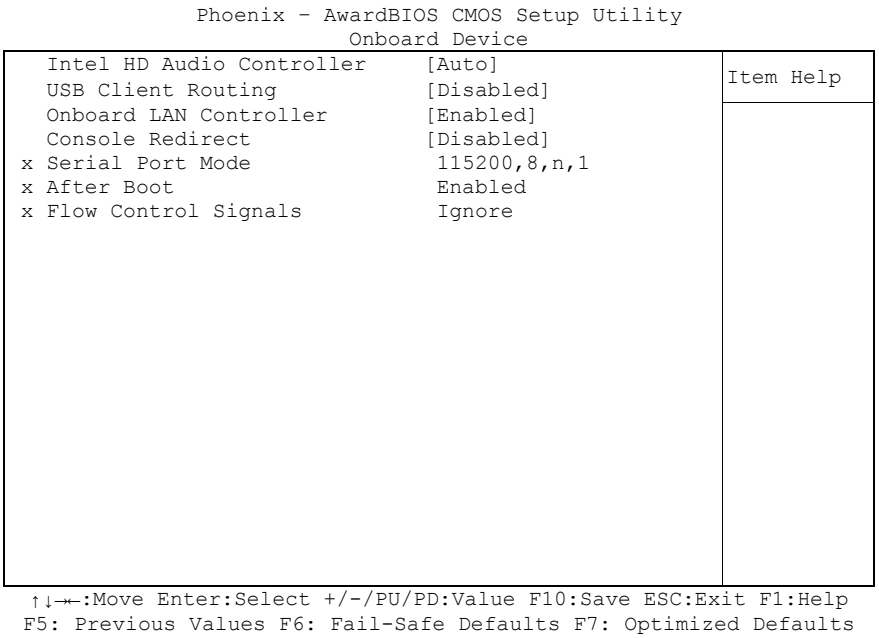
- ✓ **IDE Primary Master PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

- ✓ **IDE Primary Slave PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

- ✓ **IDE Primary Master UDMA**
  Options: Disabled / UDMA33

- ✓ **IDE Primary Slave UDMA**
  Options: Disabled / UDMA33

5.6.2 Onboard Devices



- ✓ **Intel HD Audio Controller**
  Options: Auto / Disabled

- ✓ **USB Client Routing**
  Options: Enabled / Disabled

- ✓ **Onboard LAN Controller**
  Options: Enabled / Disabled

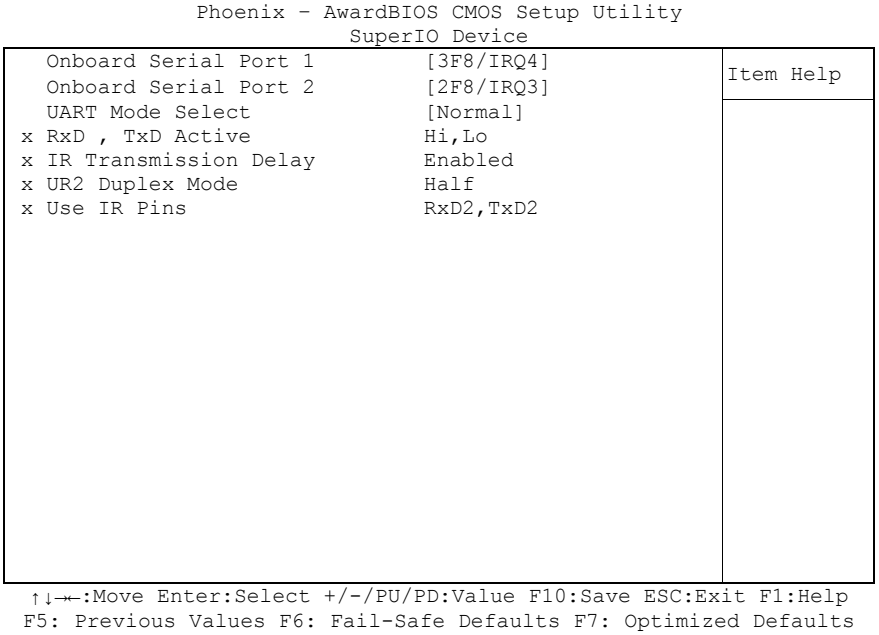
- ✓ **Console Redirect**
  Options: Disabled / COM1 / COM2

- ✓ **Serial Port Mode**
  Options: 9600,8,n,1 / 19200,8,n,1 / 115200,8,n,1

- ✓ **After Boot**
  Options: Enabled / Disabled

- ✓ **Flow Control Signals**
  Options: Ignore / Tested

5.6.3 SuperIO Devices



- ✓ **Onboard Serial Port 1**
  Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3 / Auto

- ✓ **Onboard Serial Port 2**
  Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3 / Auto

- ✓ **UART Mode Select**
  Options: IrDA / ASKIR / Normal

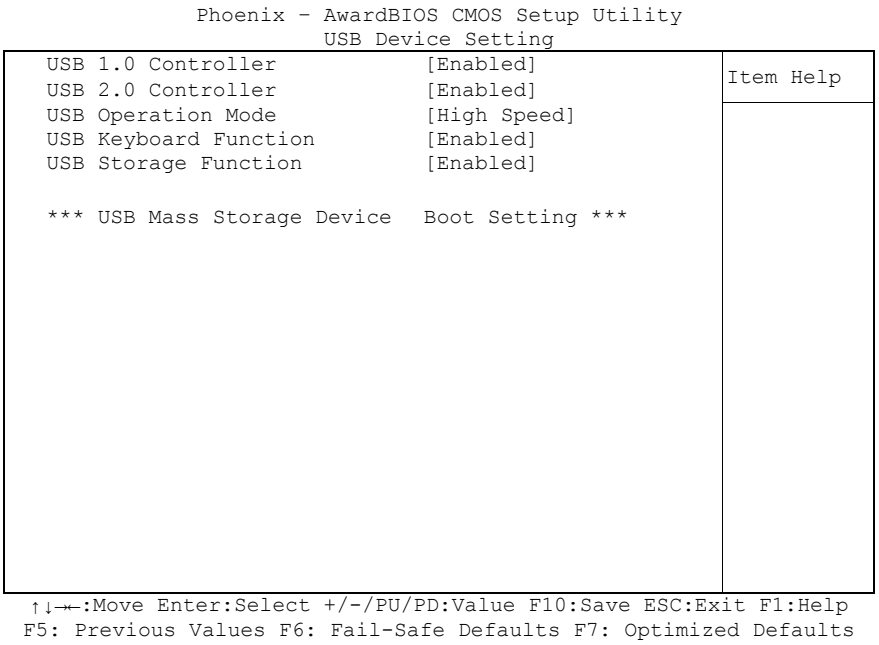
- ✓ **RxD , TxD Active**
  Options: Hi,Hi / Hi,Lo / Lo,Hi / Lo,Lo

- ✓ **IR Transmission Delay**
  Options: Enabled / Disabled

- ✓ **UR2 Duplex Mode**
  Options: Full / Half

- ✓ **Use IR Pins**
  Options: RxD2,TxD2 / IR-Rx2Tx2

5.6.4 USB Device Setting



- ✓ **USB 1.0 Controller**
  Options: Enabled / Disabled

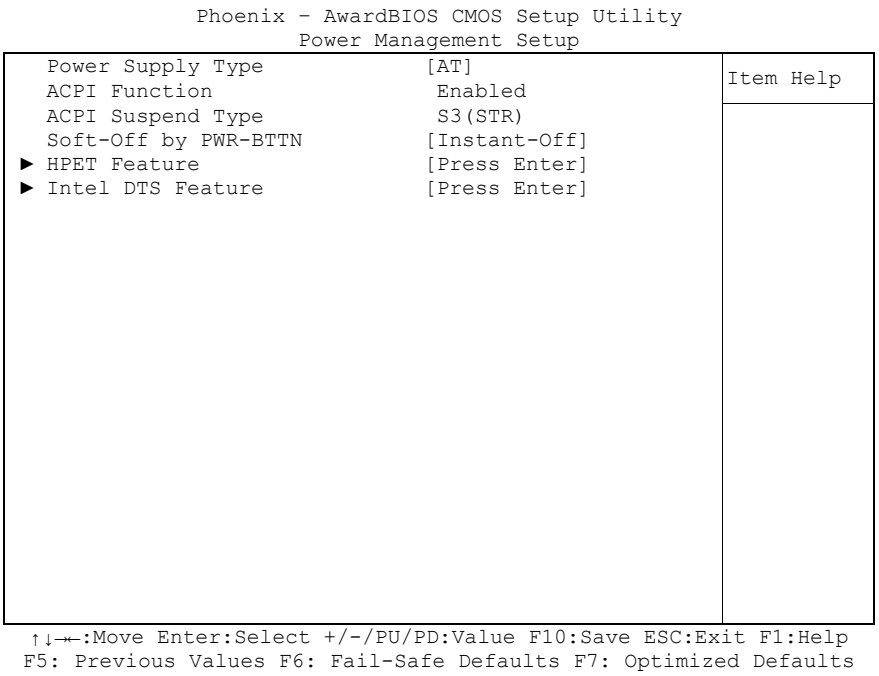
- ✓ **USB 2.0 Controller**
  Options: Enabled / Disabled

- ✓ **USB Operation Mode**
  Options: Full/Low Speed / High Speed

- ✓ **USB Keyboard Function**
  Options: Enabled / Disabled

- ✓ **USB Storage Function**
  Options: Enabled / Disabled

5.7 Power Management Setup



- ✓ **Power Supply Type**
  Options: AT / ATX

- ✓ **ACPI Function**
  Options: none

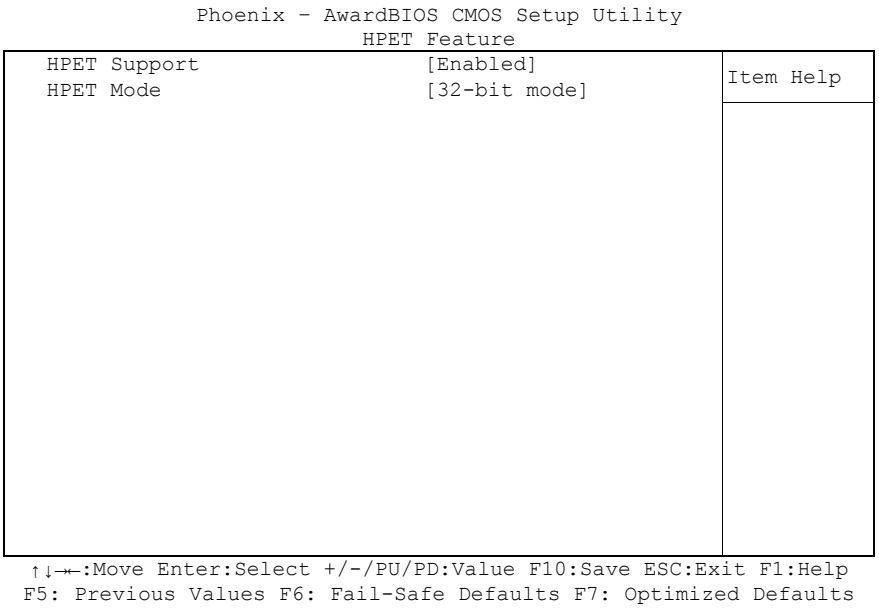
- ✓ **ACPI Suspend Type**
  Options: none

- ✓ **Soft-Off by PWR-BTTN**
  Options: Instant-Off / Delay 4 Sec

- ✓ **HPET Feature**
  Sub menu: see "HPET Feature" (page 53)

- ✓ **Intel DTS Feature**
  Sub menu: see "Intel DTS Feature" (page 54)

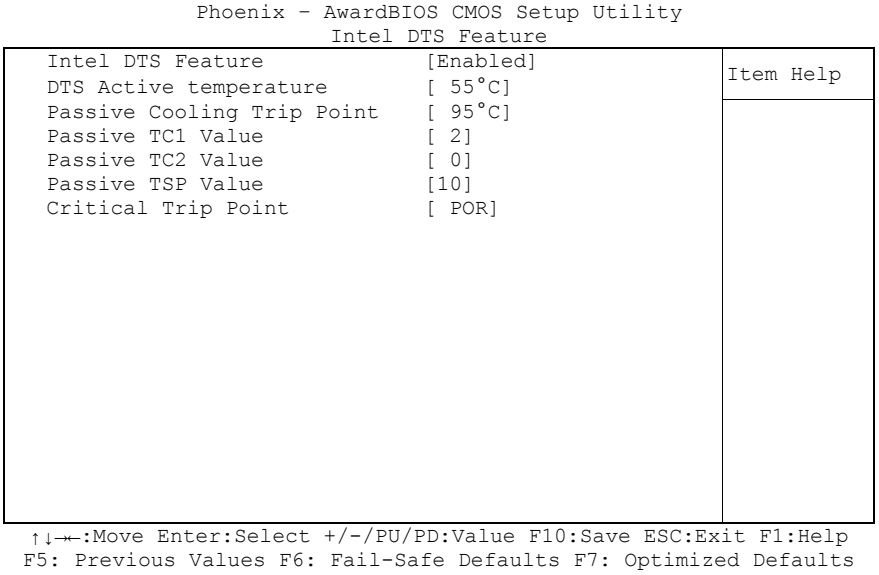
5.7.1 HPET Feature



- ✓ **HPET Support**
  Options: Enabled / Disabled

- ✓ **HPET Mode**
  Options: 32-bit mode / 64-bit mode

5.7.2 Intel DTS Feature



- ✓ **Intel DTS Function**
  Options: Enabled / Disabled

- ✓ **DTS Active temperature**
  Options: 15°C / 23°C / 31°C / 39°C / 47°C / 55°C / 63°C / 71°C / 79°C / 87°C / 95°C / 103°C / 111°C / 119°C

- ✓ **Passive Cooling Trip Point**
  Options: 15°C / 23°C / 31°C / 39°C / 47°C / 55°C / 63°C / 71°C / 79°C / 87°C / 95°C / 103°C / 111°C / 119°C

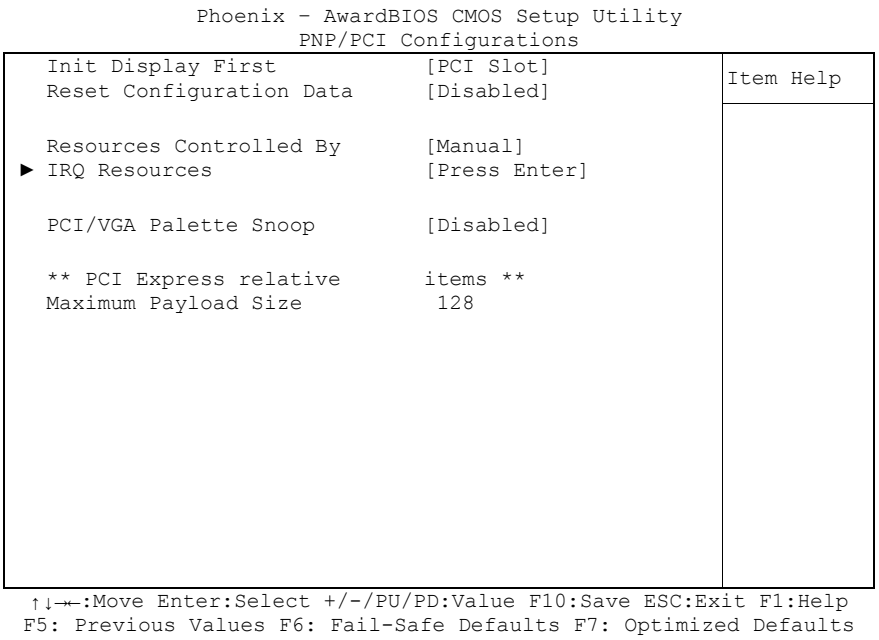
- ✓ **Passive TC1 Value**
  Options: 0 / 1 / ... / 14 / 15

- ✓ **Passive TC2 Value**
  Options: 0 / 1 / ... / 14 / 15

- ✓ **Passive TSP Value**
  Options: 0 / 1 / ... / 14 / 15

- ✓ **Critical Trip Point**
  Options: POR / 15°C / 23°C / 31°C / 39°C / 47°C / 55°C / 63°C / 71°C / 79°C / 87°C / 95°C / 103°C / 111°C / 119°C / 127°C

5.8 PnP/PCI Configuration



- ✓ **Init Display First**
  Options: PCI Slot / Onboard

- ✓ **Reset Configuration Data**
  Options: Enabled / Disabled

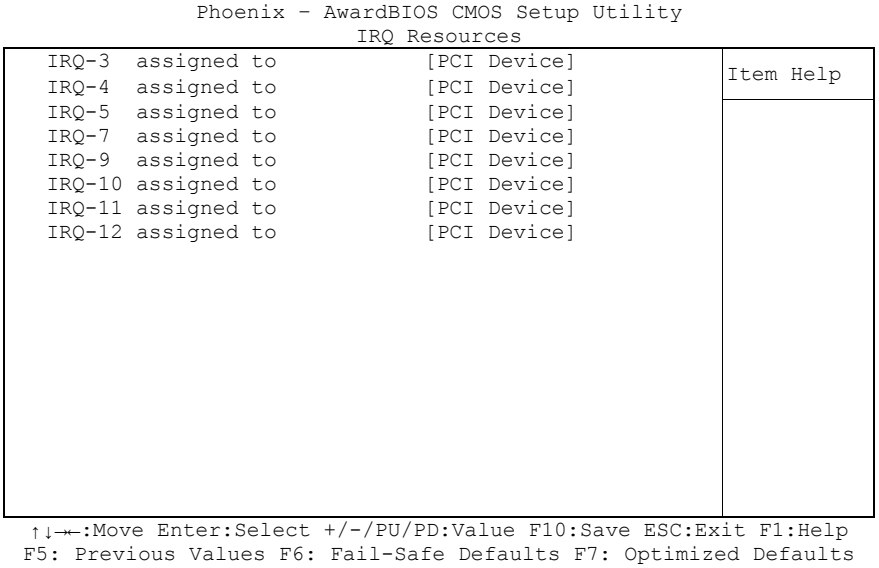
- ✓ **Resources Controlled By**
  Options: Auto(ESCD) / Manual

- ✓ **IRQ Resources**
  Sub menu: see "IRQ Resources" (page 56)

- ✓ **PCI/VGA Palette Snoop**
  Options: Enabled / Disabled

- ✓ **Maximum Payload Size**
  Options: none

5.8.1 IRQ Resources



- ✓ **IRQ-3 assigned to**
  Options: PCI Device / Reserved

- ✓ **IRQ-4 assigned to**
  Options: PCI Device / Reserved

- ✓ **IRQ-5 assigned to**
  Options: PCI Device / Reserved

- ✓ **IRQ-7 assigned to**
  Options: PCI Device / Reserved

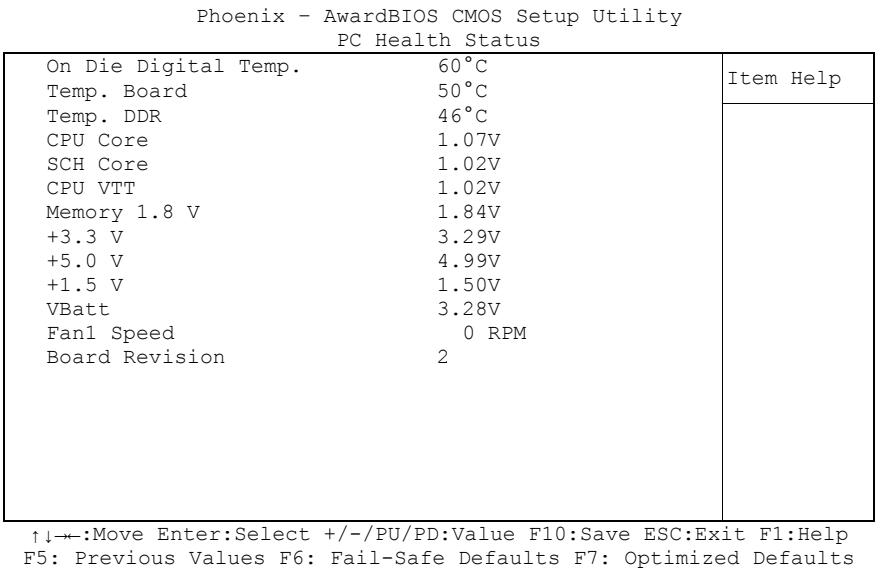
- ✓ **IRQ-9 assigned to**
  Options: PCI Device / Reserved

- ✓ **IRQ-10 assigned to**
  Options: PCI Device / Reserved

- ✓ **IRQ-11 assigned to**
  Options: PCI Device / Reserved

- ✓ **IRQ-12 assigned to**
  Options: PCI Device / Reserved

5.9 PC Health Status



- ✓ **On Die Digital Temp.**
  Options: none
- ✓ **Temp. Board**
  Options: none
- ✓ **Temp. DDR**
  Options: none
- ✓ **CPU Core**
  Options: none
- ✓ **SCH Core**
  Options: none
- ✓ **CPU VTT**
  Options: none
- ✓ **Memory 1.8 V**
  Options: none
- ✓ **+3.3 V**
  Options: none
- ✓ **+5.0 V**
  Options: none
- ✓ **+1.5 V**
  Options: none
- ✓ **VBatt**
  Options: none
- ✓ **Fan1 Speed**
  Options: none

✓ **Board Revision**
Options: none

5.10 Load Fail-Safe Defaults

If this option is chosen, the last working setup is loaded from flash. Working means that the setup setting has already led to a successful boot process.
At the first setting of the BIOS setup, safe values are loaded which lets the board boot. This status is reached again, if the board is reprogrammed with the corresponding flash-program and the required parameters.

5.11 Load Optimized Defaults

This option applies like described under “Remarks for Setup Use” (5.1).
At first start of the BIOS, optimized values are loaded from the setup, which are supposed to make the board boot. This status is achieved again, if the board is reprogrammed using the flash program with the required parameters.

5.12 Set Password

Here you can enter a password to protect the BIOS settings against unauthorized changes. Use this option with care! Forgotten or lost passwords are a frequent problem.

5.13 Save & Exit Setup

Settings are saved and the board is restarted.

5.14 Exit Without Saving

This option leaves the setup without saving any changes.

6 BIOS update

If a BIOS update becomes necessary, the program “AWDFLASH.EXE” from Phoenix Technologies is used for this. It is important, that the program is started from a DOS environment without a virtual memory manager such as for example “EMM386.EXE”. In case such a memory manager is loaded, the program will stop with an error message.
The system must not be interrupted during the flash process, otherwise the update is stopped and the BIOS is destroyed afterwards.
The program should be started as follows:

```
awdflash [biosfilename] /sn /cc /cp
```

/sn	Do not save the current BIOS
/cc	Clear the CMOS
/cp	Clear the PnP information

The erasure of CMOS and PnP is strongly recommended. This ensures, that the new BIOS works correctly and that all chipset registers, which were saved in the setup, are reinitialized through the BIOS. DMI should only be erased (option /cd) if the BIOS supplier advises to do so.
A complete description of all valid parameters is shown with the parameter “/?”.
In order to make the updating process run automatically, the parameter “/py” must be added. This parameter bypasses all security checks during programming.

CAUTION

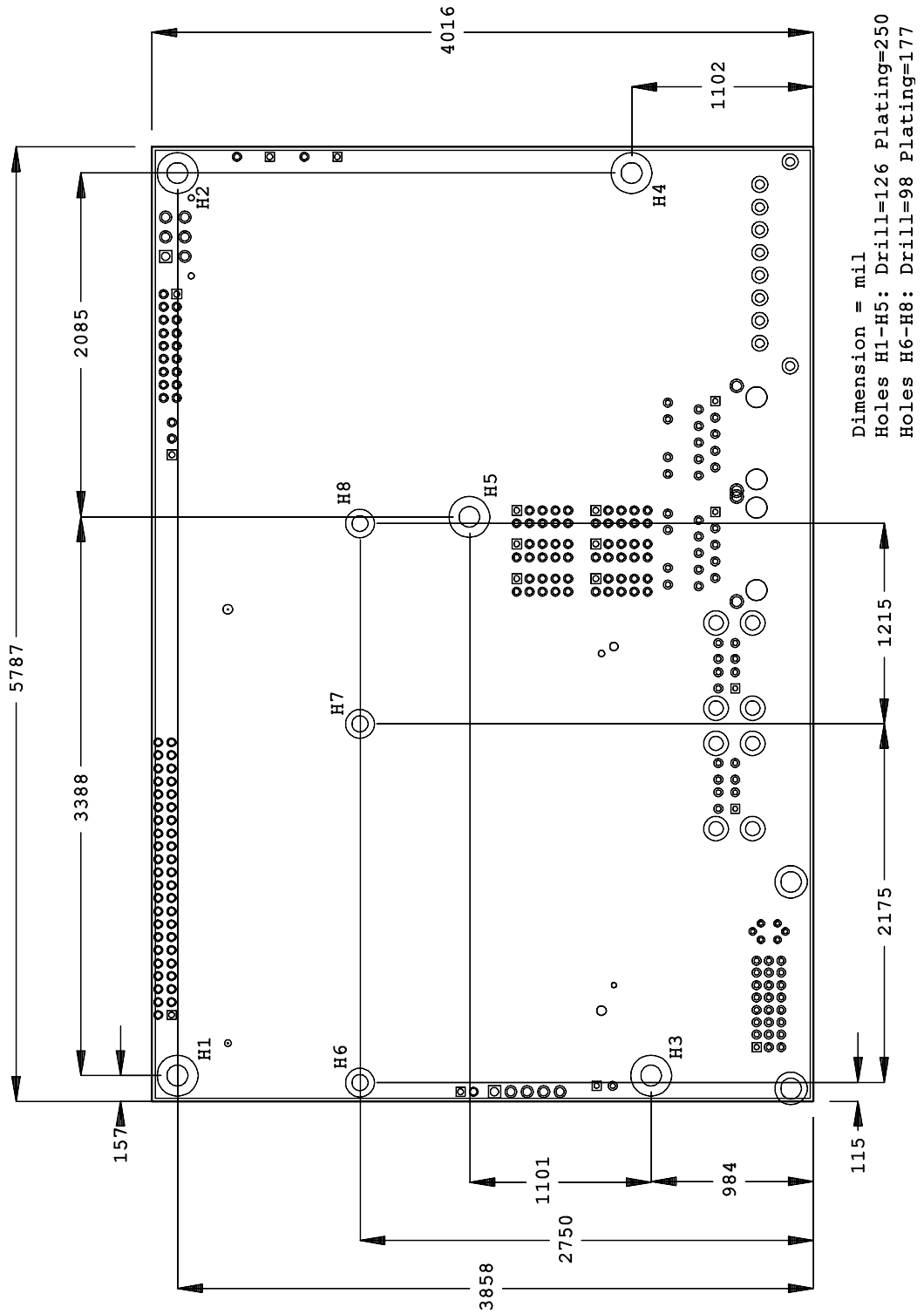
Updating the BIOS in an improper way can render the board unusable. Therefore, you should only update the BIOS if you really need the changes/corrections which come with the new BIOS version.

CAUTION

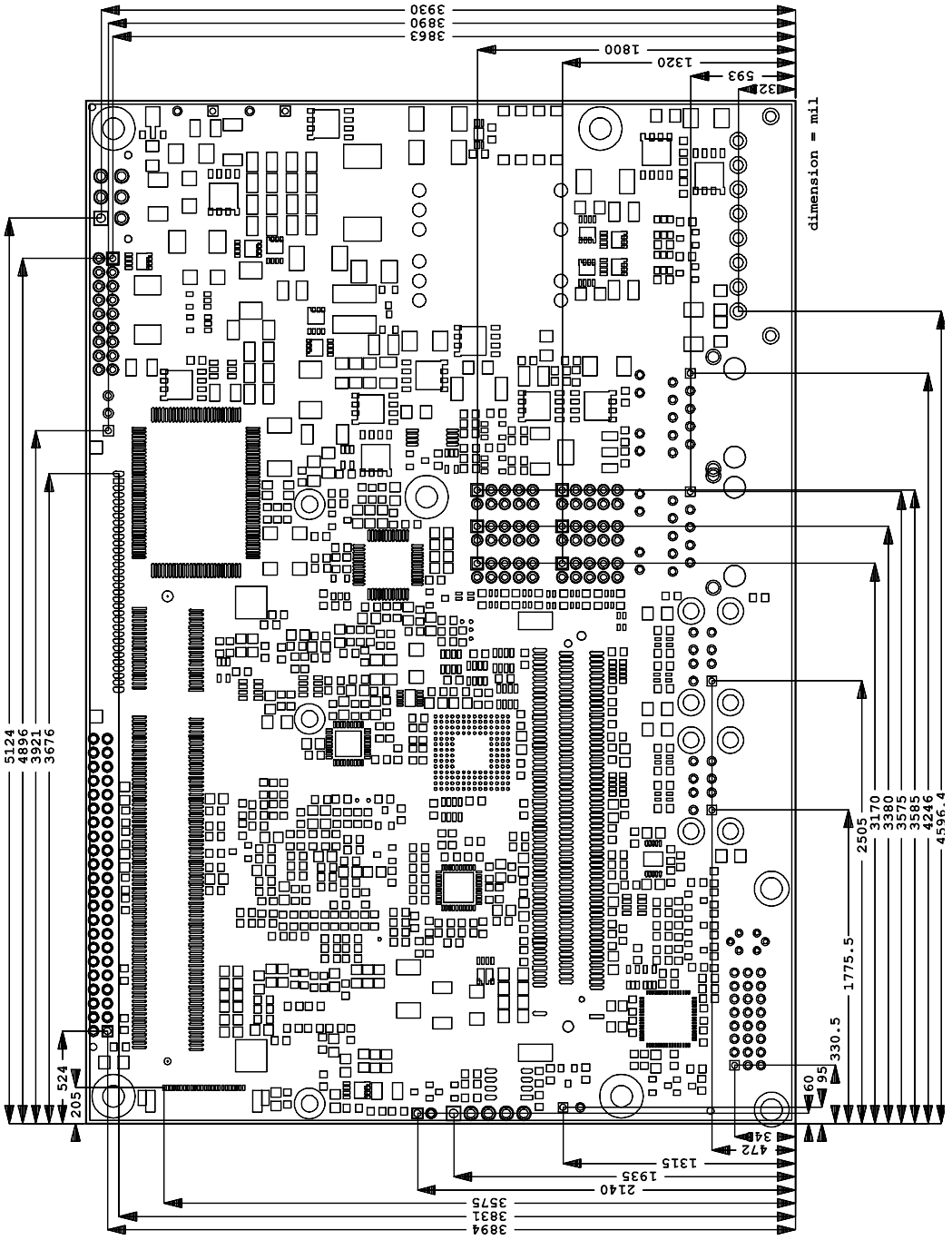
Before you proceed to update the BIOS you need to make absolutely sure that you have the right BIOS file which was issued for the exact board and exact board revision that you wish to update. If you try to update the BIOS using the wrong file the board will not start up again.

7 Mechanical Drawings

7.1 PCB: Mounting Holes



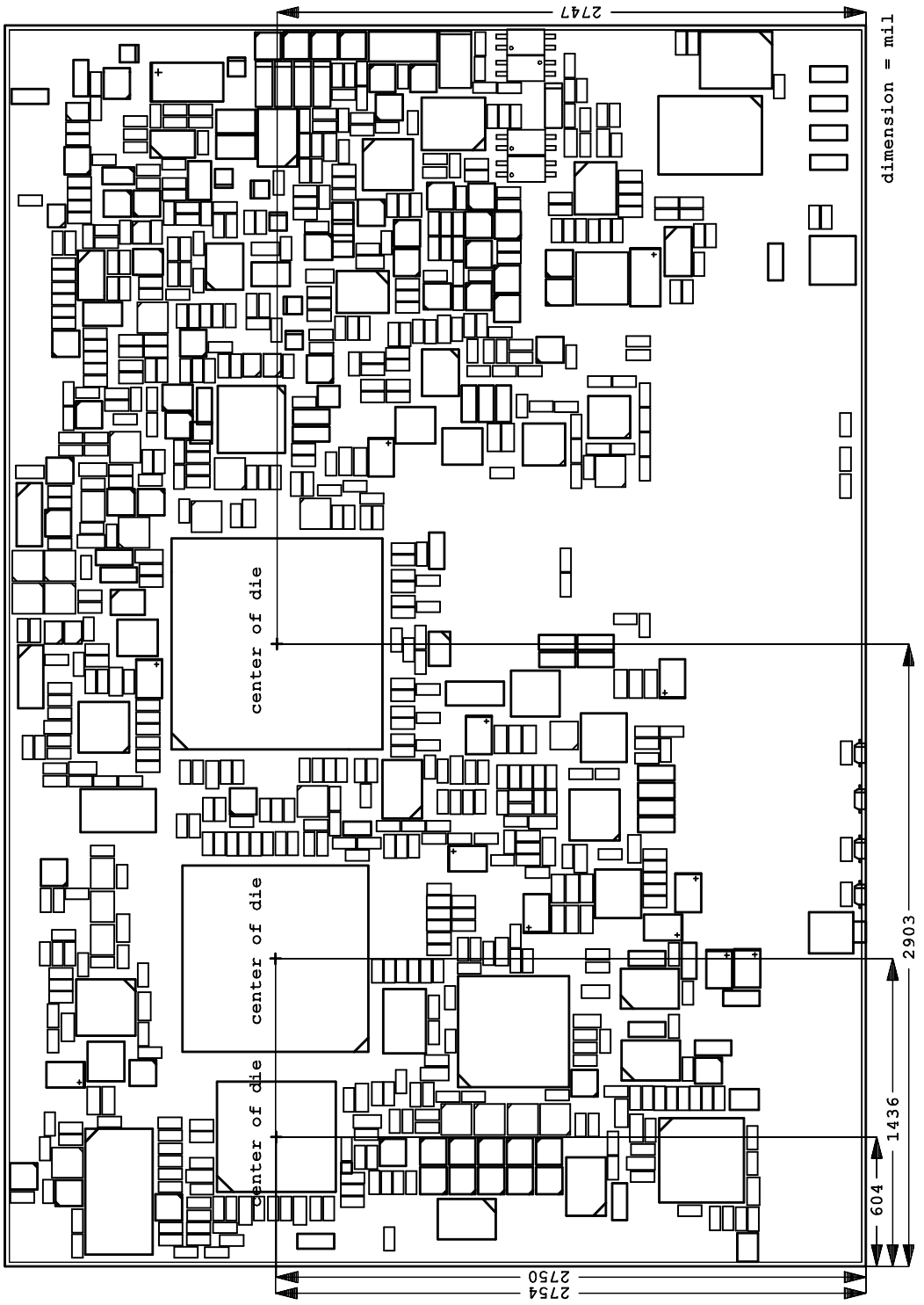
7.2 PCB: Pin 1 Dimensions



7.3 PCB: Die Center

NOTE

All dimensions are in mil (1 mil = 0,0254 mm)



8 Technical Data

8.1 Electrical Data

Power Supply:

Board:	24 Volt (20V - 30V tolerated)
RTC:	>= 3 Volt

Electric Power Consumption:

Board:	tbd
RTC:	<= 10µA

8.2 Environmental Conditions

Temperature Range:

Operating:	0°C to +60°C (extended temperature on request)
Storage:	-25°C up to +85°C
Shipping:	-25°C up to +85°C, for packaged boards

Temperature Changes:

Operating:	0.5°C per minute, 7.5°C per 30 minutes
Storage:	1.0°C per minute
Shipping:	1.0°C per minute, for packaged boards

Relative Humidity:

Operating:	5% up to 85% (non condensing)
Storage:	5% up to 95% (non condensing)
Shipping:	5% up to 100% (non condensing), for packaged boards

Shock:

Operating:	150m/s^2, 6ms
Storage:	400m/s^2, 6ms
Shipping:	400m/s^2, 6ms, for packaged boards

Vibration:

Operating:	10 up to 58Hz, 0.075mm amplitude
	58 up to 500Hz, 10m/s^2
Storage:	5 up to 9Hz, 3.5mm amplitude
	9 up to 500Hz, 10m/s^2
Shipping:	5 up to 9Hz, 3.5mm amplitude
	9 up to 500Hz, 10m/s^2, for packaged boards

CAUTION

Shock and vibration figures pertain to the motherboard alone and do not include additional components such as heat sinks, memory modules, cables etc.

8.3 Thermal Specifications

The board is specified to operate in an environmental temperature range from 0°C to +60°C (extended temperature on request). Maximum die temperature is 90°C. To keep the processor under this threshold an appropriate cooling solution needs to be applied. This solution has to take typical and maximum power consumption into account. The maximum power consumption may be twice as high and should be used as a basis for the cooling concept. Additional controllers may also affect the cooling concept. The power consumption of such components may be comparable to the consumption of the processor.
The board design includes thermal solution mounting points that will provide the best possible thermal interface between die and solution. Since we take thermal solutions seriously we have several advanced, aggressive cooling solutions in our product portfolio. Please contact your sales representative to order or discuss your thermal solution needs.

CAUTION

The end customer has the responsibility to ensure that the die temperature of the processor does not exceed 90°C. Permanent overheating may destroy the board!
In case the temperature exceeds 90°C the environmental temperature must be reduced. Under certain circumstances sufficient air circulation must be provided.

9 Support and Service

Beckhoff and their partners around the world offer comprehensive support and service, making available fast and competent assistance with all questions related to Beckhoff products and system solutions.

9.1 Beckhoff's Branch Offices and Representatives

Please contact your Beckhoff branch office or representative for local support and service on Beckhoff products.
The addresses of Beckhoff's branch offices and representatives around the world can be found on her internet pages: http://www.beckhoff.com
You will also find further documentation for Beckhoff components there.

9.2 Beckhoff Headquarters

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Eiserstr. 5
33415 Verl
Germany

phone:	+49(0)5246/963-0
fax:	+49(0)5246/963-198
e-mail:	info@beckhoff.com
web:	www.beckhoff.com

9.2.1 Beckhoff Support

Support offers you comprehensive technical assistance, helping you not only with the application of individual Beckhoff products, but also with other, wide-ranging services:

- support
- design, programming and commissioning of complex automation systems
- and extensive training programs for Beckhoff system components

hotline:	+49(0)5246/963-157
fax:	+49(0)5246/963-9157
e-mail:	support@beckhoff.com

9.2.2 Beckhoff Service

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- repair service
- spare parts service
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fax:	+49(0)5246/963-479
e-mail:	service@beckhoff.com

I Annex: Post-Codes

Code	Description
01h	The Xgroup-program code is written in the random access memory from address 1000:0 onwards.
03h	Initialise Variable/Routine "Superio_Early_Init".
05h	1. Cancel display 2. Cancel CMOS error flag
07h	1. Cancel 8042 (keyboard controller) Interface Register 2. Initialising and self testing of 8042 (keyboard controller)
08h	1. Test of special keyboard controllers (Winbond 977 super I/O Chip-series). 2. Enabling of the keyboard-interface register
0Ah	1. Disabling of the PS/2 mouse interface (optional). 2. Auto-detection of the connectors for Keyboard and mouse, optional: swap of PS/2 mouse ports and PS/2 interfaces.
0Eh	Test of the F000h-memory segment (Read/Write ability). In case of an error a signal will come out of the loud speakers.
10h	Auto-detection of the flash-rom-type and loading of the suitable Read/Write program into the run time memory segment F000 (it is required for ESCD-data & the DMI-pool-support).
12h	Interface-test of the CMOS RAM-logic (walking 1's"-algorithm). Setting of the power status of the real-time-clock (RTC), afterwards test of register overflow.
14h	Initialising of the chip-set with default values. They can be modified through a software (MODBIN) by the OEM-customer.
16h	Initialise Variable/Routine "Early_Init_Onboard_Generator".
18h	CPU auto-detection (manufacturer, SMI type (Cyrix or Intel), CPU-class (586 or 686).
1Bh	Initialising if the interrupt pointer table. If nothing else is pretended, the hardware interrupts will point on "SPURIOUS_INT_HDLR and the software interrupts will point on SPURIOUS_soft_HDLR.
1Dh	Initialise Variable/Routine EARLY_PM_INIT.
1Fh	Load the keyboard table (Notebooks)
21h	Initialising of the hardware power management (HPM) (Notebooks)
23h	1. Test the validity of the RTC-values (Example: "5Ah" is an invalid value for an RTC-minute). 2. Load the CMOS-values into the BIOS Stack. Default-values are loaded if CMOS-checksum errors occur. 3. Preparing of the BIOS 'resource map' for the PCI & plug and play configuration. If ESCD is valid, take into consideration the ESCD's legacy information. 4. Initialise the onboard clock generator. Clock circuit at non-used PCI- and DIMM slots. 5. First initialising of PCI-devices: assign PCI-bus numbers - alot memory- & I/O resources - search for functional VGA-controllers and VGA-BIOS and copy the latter into memory segment C000:0 (Video ROM Shadow).
27h	Initialise cache memory for INT 09
29h	1. Program the CPU (internal MTRR at P6 and PII) for the first memory address range (0-640K). 2. Initialising of the APIC at CPUs of the Pentium-class. 3. Program the chip-set according to the settings of the CMOS-set-up (Example: Onboard IDE-controller). 4. Measuring of the CPU clock speed. 5. Initialise the video BIOS.
2Dh	1. Initialise the "Multi-Language"-function of the BIOS 2. Soft copy, e.g. Award-Logo, CPU-type and CPU clock speed…
33h	Keyboard-reset (except super I/O chips of the Winbond 977 series)
3Ch	Test the 8254 (timer device)
3Eh	Test the interrupt Mask bits of IRQ-channel 1 of the interrupt controller 8259.
40h	Test the interrupt Mask bits of IRQ-channel 2 of the interrupt controller 8259
43h	Testing the function of the interrupt controller (8259).
47h	Initialise EISA slot (if existent).

Code	Description
49h	1. Determination of the entire memory size by revising the last 32-Bit double word of each 64k memory segment. 2. Program “write allocation” at AMD K5-CPUs.
4Eh	1. Program MTRR at M1 CPUs 2. Initialise level 2-cache at CPUs of the class P6 and set the “cacheable range” of the random access memory. 3. Initialise APIC at CPUs of the class P6. 4. Only for multiprocessor systems (MP platform): Setting of the “cacheable range” on the respective smallest value (for the case of non-identical values).
50h	Initialise USB interface
52h	Testing of the entire random access memory and deleting of the extended memory (put on “0”)
55h	Only for multi processor systems (MP platform): Indicate the number of CPUs.
57h	1. Indicate the plug and play logo 2. First ISA plug and play initialising – CSN-assignment for each identified ISA plug and play device.
59h	Initialise TrendMicro anti virus program code.
5Bh	(Optional:) Indication of the possibility to start AWDFLASH.EXE (Flash ROM programming) from the hard disk.
5Dh	1. Initialise Variable/Routine Init_Onboard_Super_IO. 2. Initialise Variable/Routine Init_Onbaord_AUDIO.
60h	Release for starting the CMOS set-up (this means that before this step of POST, users are not able to access the BIOS set-up).
65h	Initialising of the PS/2 mouse.
67h	Information concerning the size of random access memory for function call (INT 15h with AX-Reg. = E820h).
69h	Enable level 2 cache
6Bh	Programming of the chip set register according to the BIOS set-up and auto-detection table.
6Dh	1. Assignment of resources for all ISA plug and play devices. 2. Assignment of the port address for onboard COM-ports (only if an automatic junction has been defined in the setup).
6Fh	1. Initialising of the floppy controller 2. Programming of all relevant registers and variables (floppy and floppy controller).
73h	Optional feature: Call of AWDFLASH.EXE if: - the AWDFLASH program was found on a disk in the floppy drive. - the shortcut ALT+F2 was pressed.
75h	Detection and installation of the IDE drives: HDD, LS120, ZIP, CDROM…
77h	Detection of parallel and serial ports.
7Ah	Co-processor is detected and enabled.
7Fh	1. Switch over to the text mode, the logo output is supported. - Indication of possibly emerged errors. Waiting for keyboard entry. - No errors emerged, respective F1 key was pressed (continue): Deleting of the EPA- or own logo.
82h	1. Call the pointer to the “chip set power management”. 2. Load the text font of the EPA-logo (not if a complete picture is displayed) 3. If a password is set, it is asked here.
83h	Saving of the data in the stack, back to CMOS.
84h	Initialising of ISA plug and play boot drives (also Boot-ROMs)
85h	1. Final initialising of the USB-host. 2. At network PCs (Boot-ROM): Construction of a SYSID structure table 3. Backspace the scope presentation into the text mode 4. Initialise the ACPI table (top of memory). 5. Initialise and link ROMs on ISA cards 6. Assignment of PCI-IRQs 7. Initialising of the advanced power management (APM) 8. Set back the IRQ-register.

Code	Description
93h	Reading in of the hard disk boot sector for the inspection through the internal anti virus program (trend anti virus code)
94h	1. Enabling of level 2 cache 2. Setting of the clock speed during the boot process 3. Final initialising of the chip set. 4. Final initialising of the power management. 5. Erase the onscreen and display the overview table (rectangular box). 6. Program “write allocation” at K6 CPUs (AMD) 7. Program “write combining” at P6 CPUs (INTEL)
95h	1. Program the changeover of summer-and winter-time 2. Update settings of keyboard-LED and keyboard repeat rates
96h	1. Multi processor system: generate MP-table 2. Generate and update ESCD-table 3. Correct century settings in the CMOS (20xx or 19xx) 4. Synchronise the DOS-system timer with CMOS-time 5. Generate an MSIRQ-Routing table..
C0h	Chip set initialising: - Cut off shadow RAM - Cut off L2 cache (apron 7 or older) - Initialise chip set register
C1h	Memory detection: Auto detection of DRAM size, type and error correction (ECC or none) Auto detection of L2 cache size (apron 7 or older)
C3h	Unpacking of the packed BIOS program codes into the random access memory.
C5h	Copying of the BIOS program code into the shadow RAM (segments E000 & F000) via chipset hook.
CFh	Testing of the CMOS read/write functionality
FFh	Boot trial over boot-loader-routine (software-interrupt INT 19h)

II Annex: Resources

IO Range

The used resources depend on setup settings.
The given values are ranges, which are fixed by AT compatibility. Other IO ranges are used, which are dynamically adjusted by Plug & Play BIOS while booting.

Address	Function
0-FF	Reserved IO area of the board
170-17F	
1F0-1F7	IDE1
278-27F	
2E8-2EF	
2F8-2FF	COM2
370-377	
378-37F	
3BC-3BF	
3E8-3EF	
3F0-3F7	
3F8-3FF	COM1

Memory Range

The used resources depend on setup settings.
If the entire range is clogged through option ROMs, these functions do not work anymore.

Address	Function
A0000-BFFFF	VGA RAM
C0000-CFFFF	VGA BIOS
D0000-DFFFF	AHCI BIOS / RAID / PXE (if available)
E0000-EFFFF	System BIOS while booting
F0000-FFFFF	System BIOS

Interrupt

The used resources depend on setup settings.
The listed interrupts and their use are given through AT compatibility.
If interrupts must exclusively be available on the ISA side, they have to be reserved through the BIOS setup.
The exclusivity is not given and not possible on the PCI side.

Address	Function
IRQ0	Timer
IRQ1	PS/2 Keyboard
IRQ2 (9)	
IRQ3	COM1
IRQ4	COM2
IRQ5	
IRQ6	
IRQ7	
IRQ8	RTC
IRQ9	
IRQ10	
IRQ11	
IRQ12	PS/2 Mouse

Address	Function
IRQ13	FPU
IRQ14	IDE Primary
IRQ15	

PCI Devices

All listed PCI devices exist on the board. Some PCI devices or functions of devices may be disabled in the BIOS setup. Once a device is disabled other devices may get PCI bus numbers different from the ones listed in the table.

AD	INTA	REQ	Bus	Dev.	Fct.	Controller / Slot
	-	-	0	0	0	Host Bridge ID8100h
	A	-	0	2	0	VGA Graphics ID8108h
	A	-	0	27	0	HDA Controller ID811Bh
	A	-	0	28	0	PCI Express Port 1 ID8110h
	B	-	0	28	1	PCI Express Port 2 ID8112h
	A	-	0	29	0	USB UHCI Controller #1 ID8114h
	B	-	0	29	1	USB UHCI Controller #2 ID8115h
	C	-	0	29	2	USB UHCI Controller #3 ID8116h
	D	-	0	29	7	USB 2.0 EHCI Controller ID8117h
	-	-	0	31	0	LPC Interface ID8119h
	-	-	0	31	1	IDE Controller ID811Ah
	A	-	(1)	0	0	LAN i82575EB ID10A7h
	B	-	(1)	0	1	LAN i82575EB ID10A7h
	A	-	(2)	0	0	PCI Bridge IDE110h
21	A	0	(3)	5	0	mPCI

SMB Devices

The following table contains all reserved SM-Bus device addresses in 8-bit notation. Note that external devices must not use any of these addresses even if the component mentioned in the table is not present on the motherboard.

Address	Function
10-11	Standard slave address
40-41	GPIO
60-61	BIOS internal
70-73	POST code output
88-89	BIOS-defined slave address
A0-A1	DIMM 1
A2-A3	DIMM 2
A4-AF	BIOS internal
B0-BF	BIOS internal
D2-D3	Clock