BECKHOFF

CB1052

Manual

rev 0.2

ATX power supply

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Contents

0 Document History

Version	Changes
0.1	first pre-release
0.2	corrected LAN pinout in chapter 3.2.3; corrected chapter 3.4.9

NOTE

1 Introduction

1.1 Notes on the Documentation

This description is only intended for the use of trained specialists in control and automation engineering who are familiar with the applicable national standards. It is essential that the following notes and explanations are followed when installing and commissioning these components.

1.1.1 Liability Conditions

The responsible staff must ensure that the application or use of the products described satisfy all the requirements for safety, including all the relevant laws, regulations, guidelines and standards.
The documentation has been prepared with care. The products described are, however, constantly under development. For that reason the documentation is not in every case checked for consistency with performance data, standards or other characteristics. None of the statements of this manual represents a guarantee (Garantie) in the meaning of § 443 BGB of the German Civil Code or a statement about the contractually expected fitness for a particular purpose in the meaning of § 434 par. 1 sentence 1 BGB. In the event that it contains technical or editorial errors, we retain the right to make alterations at any time and without warning. No claims for the modification of products that have already been supplied may be made on the basis of the data, diagrams and descriptions in this documentation.

1.1.2 Copyright

1.2 Safety Instructions

Please consider the following safety instructions and descriptions. Product specific safety instructions are to be found on the following pages or in the areas mounting, wiring, commissioning etc.

1.2.1 Disclaimer

All the components are supplied in particular hardware and software configurations appropriate for the application. Modifications to hardware or software configurations other than those described in the documentation are not permitted, and nullify the liability of Beckhoff Automation GmbH.

1.2.2 Description of Safety Symbols

The following safety symbols are used in this documentation. They are intended to alert the reader to the associated safety instructions.

ACUTE RISK OF INJURY!

If you do not adhere to the safety advise next to this symbol, there is immediate danger to life and health of individuals!

RISK OF INJURY!

If you do not adhere to the safety advise next to this symbol, there is danger to life and health of individuals!

HAZARD TO INDIVIDUALS, ENVIRONMENT, DEVICES, OR DATA!

If you do not adhere to the safety advise next to this symbol, there is obvious hazard to individuals, to environment, to materials, or to data.

NOTE OR POINTER

This symbol indicates information that contributes to better understanding.

1.3 Essential Safety Measures

1.3.1 Operator's Obligation to Exercise Diligence

The operator must ensure that

- the product is only used for its intended purpose
- the product is only operated in sound condition and in working order
- the instruction manual is in good condition and complete, and always available for reference at the location where the products are used
- the product is only used by suitably qualified and authorised personnel
- the personnel is instructed regularly about relevant occupational safety and environmental protection aspects
- the operating personnel is familiar with the operating manual and in particular the safety notes contained herein

1.3.2 National Regulations Depending on the Machine Type

Depending on the type of machine and plant in which the product is used, national regulations governing the controllers of such machines will apply, and must be observed by the operator. These regulations cover, amongst other things, the intervals between inspections of the controller. The operator must initiate such inspections in good time.

1.3.3 Operator Requirements

- Read the operating instructions

All users of the product must have read the operating instructions for the system they work with.

- System know-how

All users must be familiar with all accessible functions of the product.

1.4 Functional Range

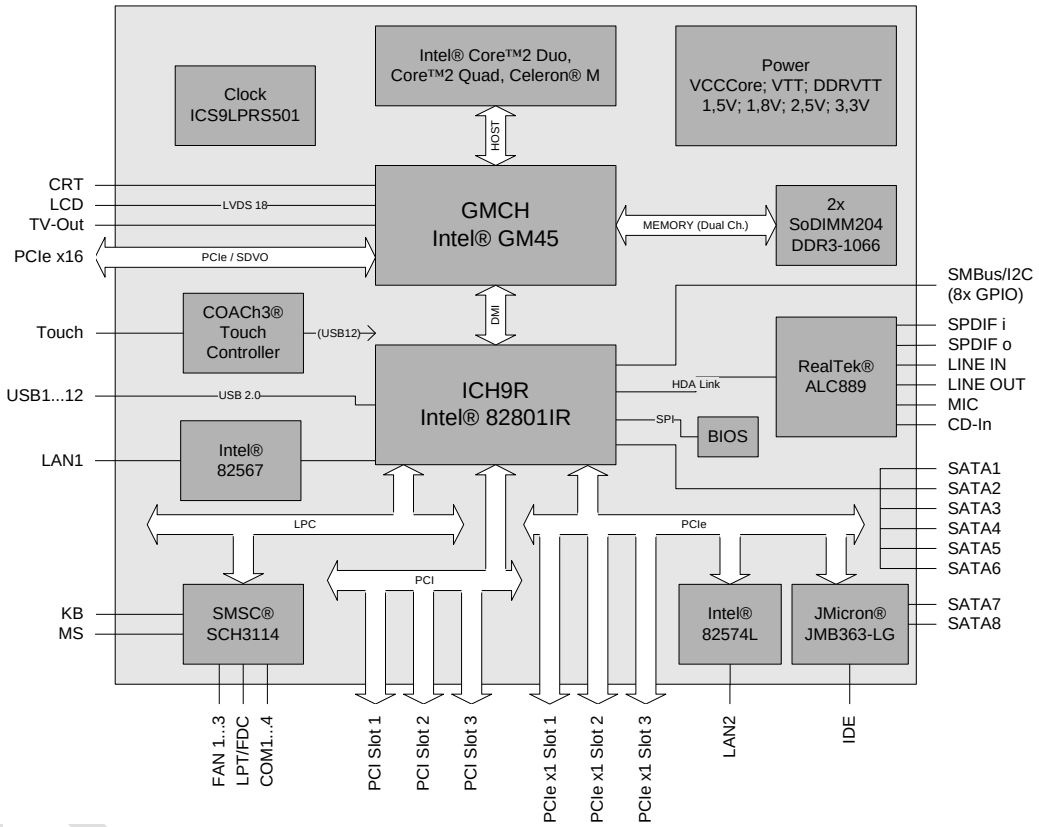
NOTE

The descriptions contained in the present documentation represent a detailed and extensive product description. As far as the described motherboard was acquired as an integral component of an Industrial PC from Beckhoff Automation GmbH, this product description shall be applied only in limited scope. Only the contractually agreed specifications of the corresponding Industrial PC from Beckhoff Automation GmbH shall be relevant. Due to several models of Industrial PCs, variations in the component placement of the motherboards are possible. Support and service benefits for the built-in motherboard will be rendered by Beckhoff Automation GmbH exclusively as specified in the product description (inclusive operation system) of the particular Industrial PC.

2 Overview

2.1 Features

The CB1052 is a computer motherboard for industrial applications. Complying to the ATX form factor, it is equipped with an mPGA479M socket which can accomodate Intel® CPUs of the Celeron® M, Core™2 Duo and Core™2 Quad types. With its two SO-DIMM204 sockets memory can be added up to 8 GByte (DDR3-1066 max.). Expansion cards can be added into three PCI slots, three PCIeX1 slots, and one PCIeX16 slots. The CB1052 also offers a wide range of internal and external connectors, such as four serial ports, two LAN connectors, twelve USB channels, one PATA and eight SATA connectors, digital and analogue audio, CRT/LCD connector, TV-Out connector etc.



- Processor Intel® Core™2 Duo/Quad or Celeron® M
- Chipset Intel® GM45 with integrated graphics and ICH9R
- Two SO-DIMM204 sockets for up to 8 GByte DDR3-1066 RAM
- Four serial ports COM1 up to COM4
- 2x Ethernet LAN 10/100/1000 (Base-T)
- IDE interface (PATA)
- Eight SATA connectors
- PS/2 keyboard and mouse interface
- LPT interface
- Twelve USB 2.0 interfaces
- AWARD BIOS
- CRT connection
- TFT connection via LVDS 18 bit
- AC97/HDA compatible sound controller with SPDIF in and out
- RTC with external CMOS battery

- ATX power supply (including 2x2pin 12V connector)
- Three PCI slots
- Three PCIe x1 slots
- One PCIe x16 slot
- Option: Touchscreen connector (4wire/5wire resistive)
- ATX form factor (305mm x 220mm)

2.2 Specifications and Documents

In making this manual and for further reading of technical documentation, the following documents, specifications and web-pages were used and are recommended.

- ATX specification
  Version 2.2
  www.formfactors.org
- PCI specification
  Version 2.3 resp. 3.0
  www.pcisig.com
- PCI-Express specification
  Version 1.1
  www.pcisig.com
- ACPI specification
  Version 3.0
  www.acpi.info
- ATA/ATAPI specification
  Version 7 Rev. 1
  www.t13.org
- USB specifications
  www.usb.org
- SM-Bus specification
  Version 2.0
  www.smbus.org
- Intel®-Chip Description
  Celeron® M, Core™ 2 Duo, Core™ 2 Quad
  www.intel.com
- Intel® Chipset Description
  Intel® 4 Series Express Chipset Family datasheet
  www.intel.com
- Intel® Chip Description
  Intel® ICH9 Datasheet
  www.intel.com
- Intel® Chip Description
  82574L Datasheet
  www.intel.com
- Intel® Chip Description
  82567 Datasheet
  www.intel.com
- Realtek® Chip Description
  ALC885/889 Datasheet
  www.realtek.com.tw
- SMSC® Chip Description
  SCH3114 Datasheet
  www.smsc.com
  (NDA required)
- IDT® Chip Description
  ICS9LPRS501 Datasheet
  www.idt.com

3 Connectors

This section describes all the connectors found on the CB1052.

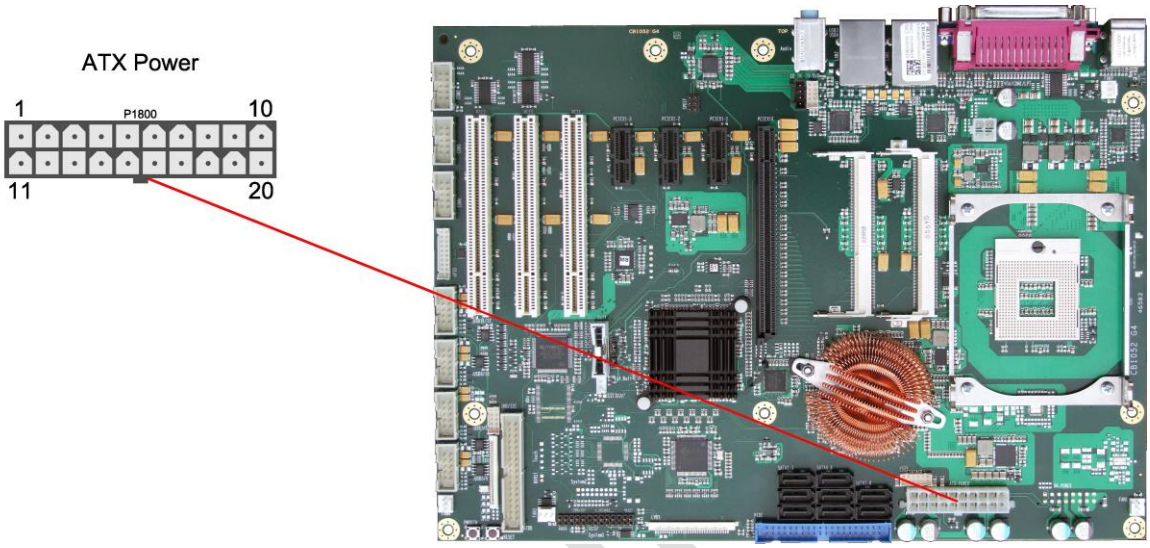
CAUTION

For most interfaces, the cables must meet certain requirements. For instance, USB 2.0 requires twisted and shielded cables to reliably maintain full speed data rates. Restrictions on maximum cable length are also in place for many high speed interfaces and for power supply. Please refer to the respective specifications and use suitable cables at all times.

3.1 Power Supply, System Connectors, CPU

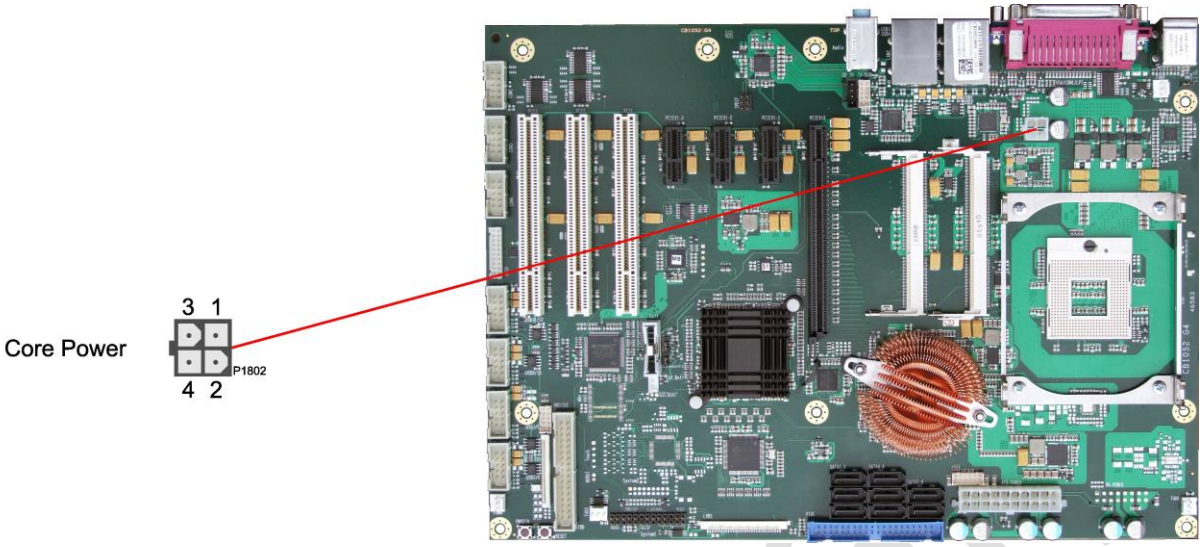
3.1.1 Power Supply

The connector for the power supply is a 2x10pin ATX connector ("ATX20", Foxconn HM3510E-P2). It is accompanied by a 2x2pin connector, which must be used to provide the COREIN power supply.



Pinout "ATX20" power connector:

Description	Name	Pin		Name	Description
3.3 volt supply	3.3V	1	11	3.3V	3.3 volt supply
3.3 volt supply	3.3V	2	12	-12V	12 volt supply
ground	GND	3	13	GND	ground
5 volt supply	VCC	4	14	PWRBTN#	powerbutton
ground	GND	5	15	GND	ground
5 volt supply	VCC	6	16	GND	ground
ground	GND	7	17	GND	ground
power on	PWR_ON	8	18	-5V	volt supply -5V
standby supply 5V	SVCC	9	19	VCC	5 volt supply
12 volt supply	12V	10	20	VCC	5 volt supply

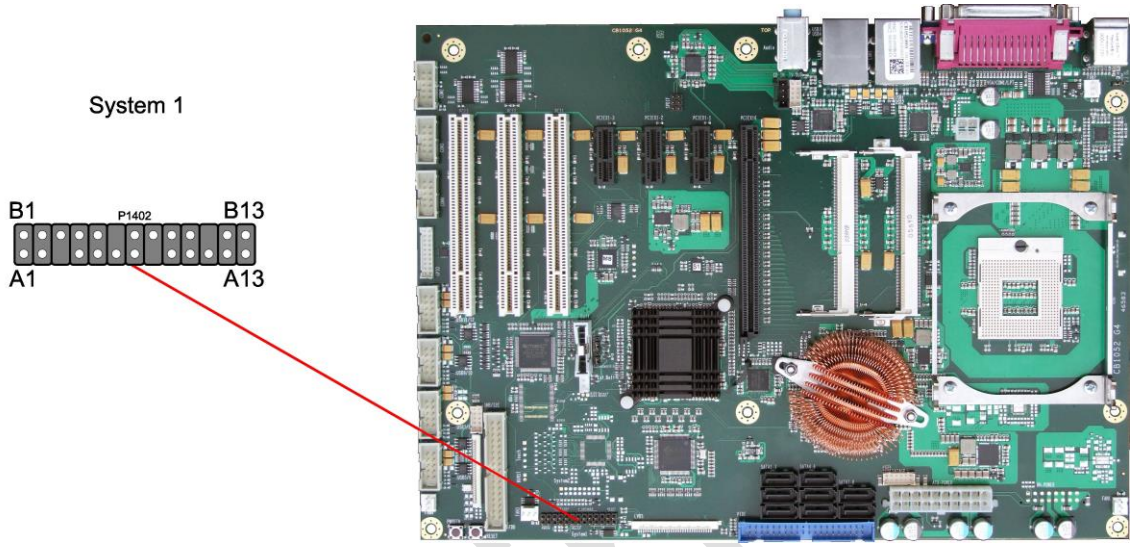


Pinout ATX power connector 2x2:

Description	Name	Pin		Name	Description
ground	GND	1	3	COREIN	12 volt supply
ground	GND	2	4	COREIN	12 volt supply

3.1.2 System

Typical signals for system control are provided through a 2x13 IDC socket connector with a spacing of 2.54mm. This connector combines signals for power button, reset, keyboard lock, IrDA, and several LEDs.



Pinout IDC socket connector "System 1":

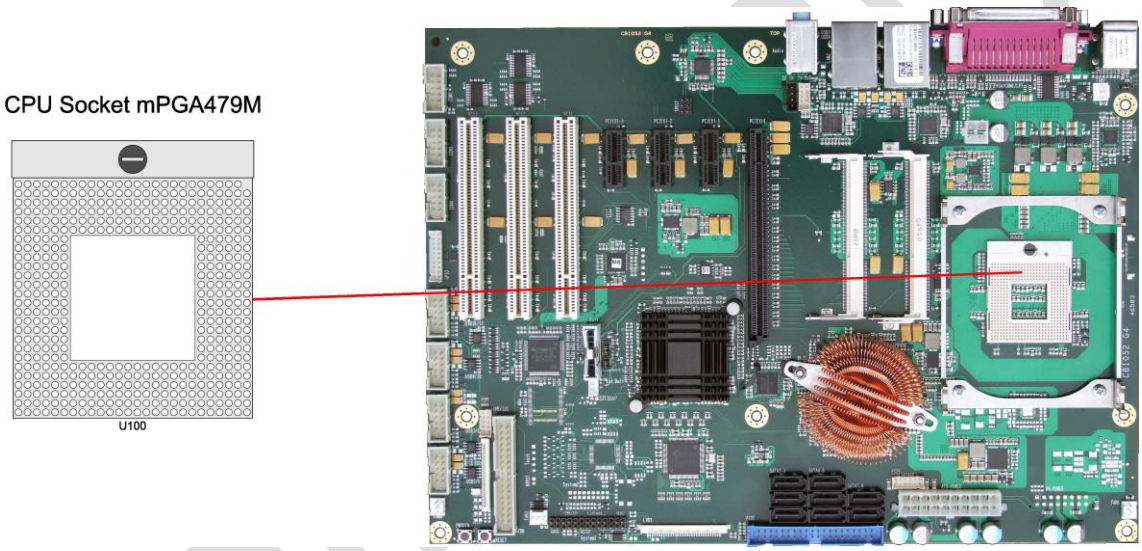
Description	Name	Pin		Name	Description
on/suspend button	PWRBTN#	A1	B1	GND	ground
ground	GND	A2	B2	KBLOCK	keyboard lock
reserved	N/C	A3	B3	PWLED#	power LED
ground	GND	A4	B4	N/C	reserved
5 volt supply	VCC	A5	B5	PWLED	3.3 volt supply
harddisk LED	HDLED#	A6	B6	N/C	reserved
5 volt supply	VCC	A7	B7	VCC	5 volt supply
reserved	N/C	A8	B8	GND	ground
IrDA transmit	IRTX	A9	B9	N/C	reserved
ground	GND	A10	B10	BEEP	speaker
IrDA receive	IRRX	A11	B11	N/C	reserved
IrDA control	CIRRX	A12	B12	GND	ground
5 volt supply	VCC	A13	B13	RESET#	reset

3.1.3 CPU Socket

The CB1052 board has an mPGA479M CPU socket accomodating certain versions of the following types of processors manufactured by Intel®: Celeron® M, Core™2 Duo and Core™2 Quad. The mPGA479M is a ZIF (Zero Insertion Force) socket, which means that you can insert the processor without there being any resistance. There is only one orientation in which the processor will fit into the socket. Once the processor is in place the fastening screw must be tightened to ensure proper electrical contact.
The package type allows a maximum die temperature of 100 degrees Celsius and accords highest possible security even in rough environment.
The processor includes a second level cache of up to 6 MByte, depending on which model is used. Furthermore the processors offer many features known from the desktop range such as MMX2, serial number, loadable microcode etc.

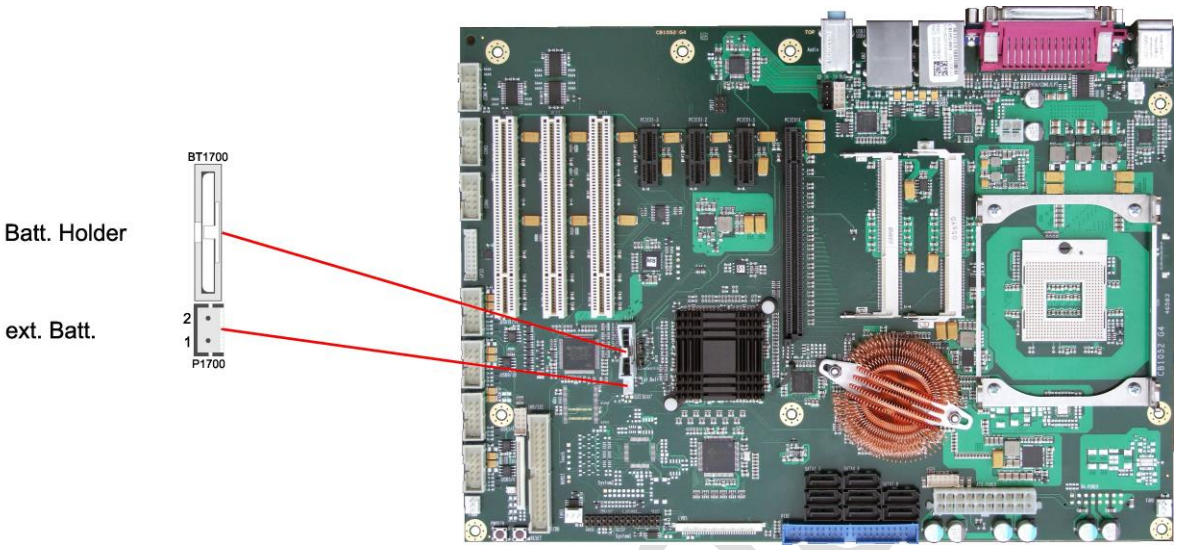
NOTE

Processors must be ordered separately. The board ships without a CPU.



3.1.4 CMOS Battery

The board ships with a CR2032 battery holder (Renata VBH2032-1) and 3V battery. Alternatively, an external battery can be connected via a 2pin connector (JST B2B-EH-A, mating connector: EHR-2).



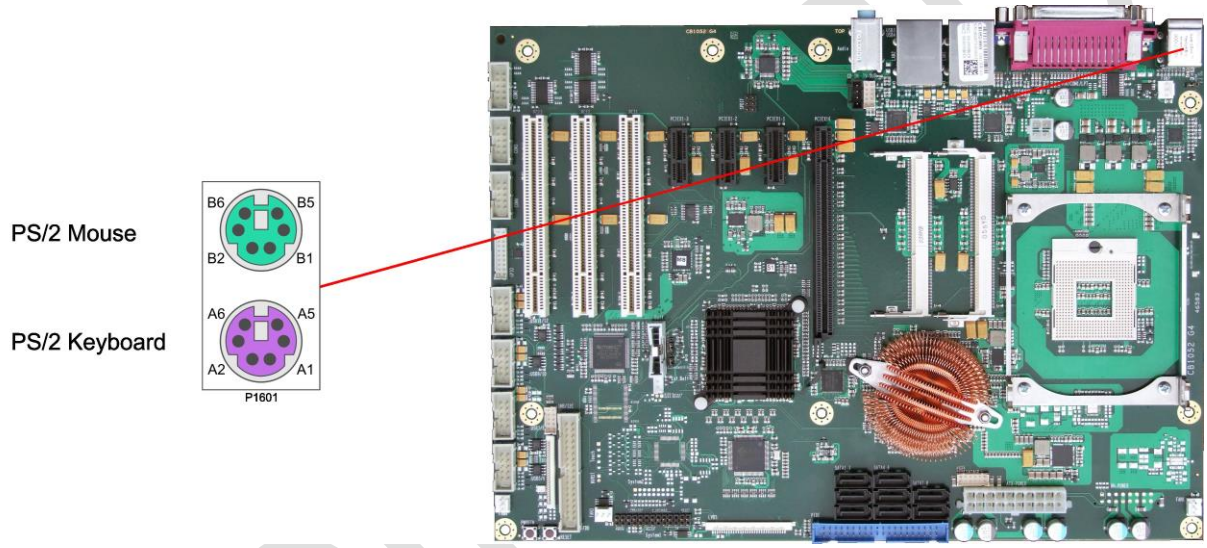
Pin	Name	Description
1	BATT	battery 3.3 volt
2	GND	ground

3.2 Back Panel Connectors

The board complies with the ATX form factor and thus honours the "I/O Connector Area" as defined in the ATX specification. A range of standard connectors are available: You can connect PS/2 keyboard and mouse, printer, display, speakers, microphone, LAN etc. If the board is mounted in a normal ATX compliant case these connectors are located on the back side of the case. In the following sections we will discuss each connector, going from left to right (looking onto the rear side of a desktop case) or from top to bottom (tower case).

3.2.1 PS/2 Keyboard and Mouse

PS/2 mice and keyboards are connected via standard mini-DIN connectors. If you want to use the keyboard or mouse to wake up the board from standby or suspend mode you have to activate this functionality by adjusting the KBPWR jumper settings (page 50). With this jumper you can switch from normal power supply (VCC) to standby power supply (SVCC) for keyboard/mouse. Some relevant settings will have to be adjusted in BIOS setup.



Pinout PS/2 mouse:

Description	Name	Pin		Name	Description
mouse data	MDAT	B1	B2	N/C	reserved
ground	GND	B3	B4	(S)VCC	5 volt supply
mouse clock	MCLK	B5	B6	N/C	reserved

Pinout PS/2 keyboard:

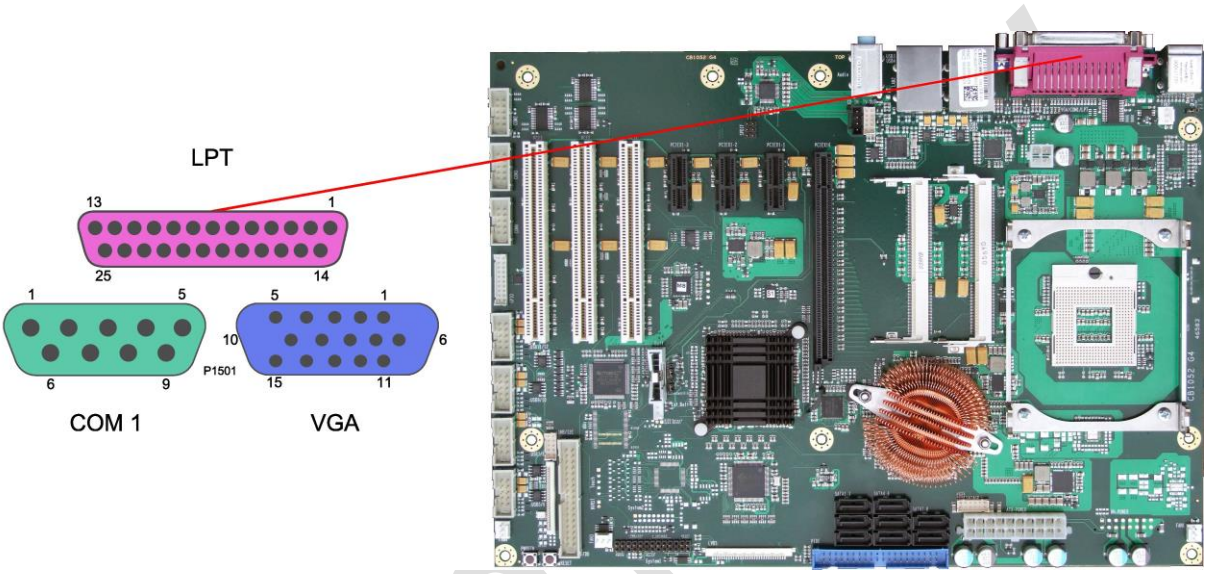
Description	Name	Pin		Name	Description
keyboard data	KDAT	A1	A2	MDAT	mouse data
ground	GND	A3	A4	(S)VCC	5 volt supply
keyboard clock	KCLK	A5	A6	MCLK	mouse clock

3.2.2 Parallel port, serial ports, VGA

On the rear panel, there is a combo connector which comprises three DSUB connectors, one for the parallel port LPT, one for the serial port COM1, and one for VGA signals.
The LPT port is provided via a 25pin DSUB connector (female).

The serial interface COM1 is made available via a 9-pin standard DSUB-connector. According to the product order, TTL level signals or RS232 standard signals are provided.
The port address and the interrupt are set via the BIOS setup.

The remaining 15pin DSUB connector (female) is used to attach a VGA display.



Pinout parallel port LPT:

Description	Name	Pin		Name	Description
strobe	STB#	1	14	AFD#	auto feed
data bit 0	PD0	2	15	ERR#	error
data bit 1	PD1	3	16	INIT#	initialize
data bit 2	PD2	4	17	SLIN#	select in
data bit 3	PD3	5	18	GND	ground
data bit 4	PD4	6	19	GND	ground
data bit 5	PD5	7	20	GND	ground
data bit 6	PD6	8	21	GND	ground
data bit 7	PD7	9	22	GND	ground
acknowledge	ACK#	10	23	GND	ground
busy	BUSY	11	24	GND	ground
paper end	PE	12	25	GND	ground
select	SLCT	13			

Pinout serial port (DSUB connector):

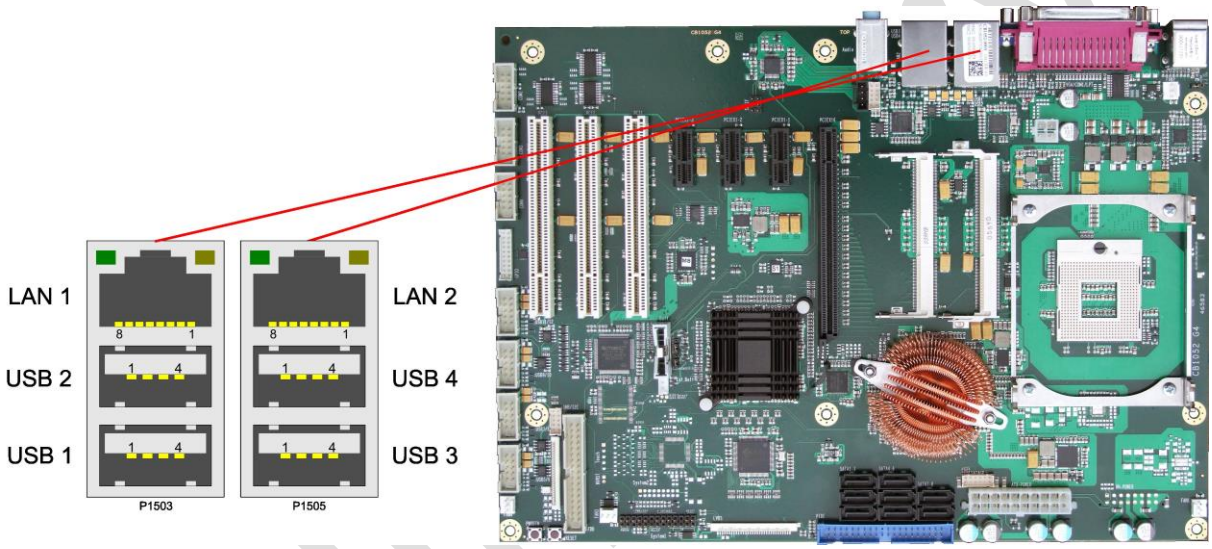
Description	Name	Pin		Name	Description
data carrier detect	DCD	1	6	DSR	data set ready
receive data	RXD	2	7	RTS	request to send
transmit data	TXD	3	8	CTS	clear to send
data terminal ready	DTR	4	9	RI	ring indicator
ground	GND	5			

Pinout VGA connector:

Pin	Name	Description
1	RED	red
2	GREEN	green
3	BLUE	blue
4	N/C	reserved
5	GND	ground
6	GND	ground
7	GND	ground
8	GND	ground
9	VCC	5 volt supply
10	GND	ground
11	N/C	reserved
12	DDDA	DDC data
13	HSYNC	horizontal sync
14	VSYNC	vertical sync
15	DDCK	DDC clock

3.2.3 USB and LAN

To save space USB and LAN connectors are provided in the form of combo connectors. These either comprise two USB connectors or two USB connectors and one LAN connector. This way all board variants provide four external USB channels.
The USB channels support USB 2.0. You may note that the setting of USB keyboard or USB mouse support in the BIOS-setup is only necessary and advisable, if the OS offers no USB-support. BIOS-setup can be changed with a USB keyboard without enabling USB keyboard support. Running Windows with these features enabled may lead to significant performance or functionality limitations.
Every USB interface provides up to 500 mA current and is protected by an electronically resettable fuse.
The board comes in different variants, some with one Gigabit-LAN connector, others with two. All LAN connectors support 10/100/1000 Ethernet with automatic bandwith selection. Controller chips are the ICH9R (MAC) accompanied by the 82567 (PHY) and, if present, the 82574L (MAC/PHY).



Pinout USB connector for channel X:

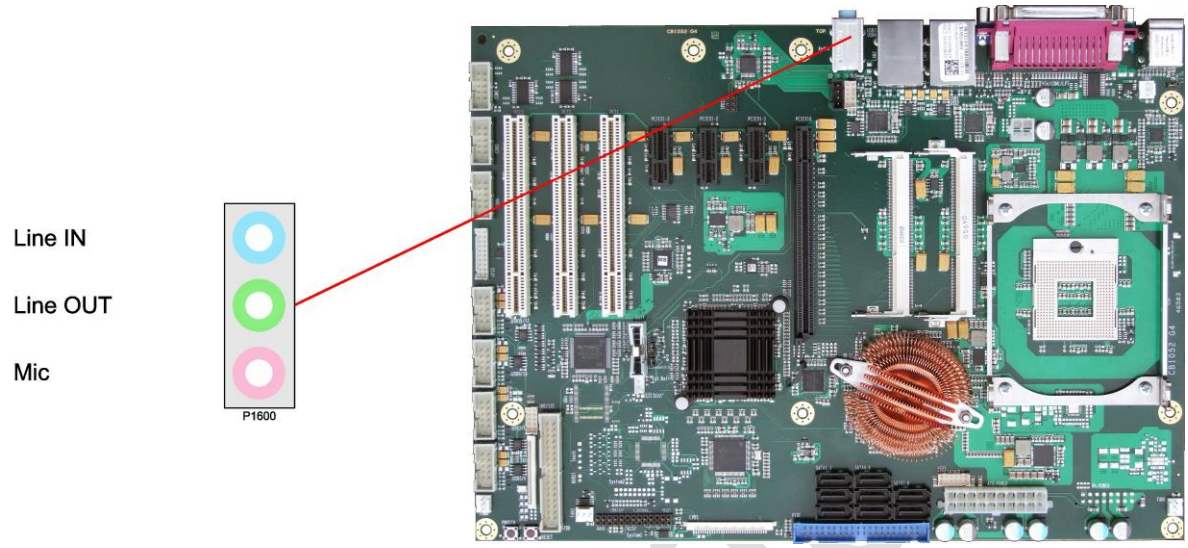
Pin	Name	Description
1	VCC	5 volt for USBX
2	USBX#	minus channel USBX
3	USBX	plus channel USBX
4	GND	ground

Pinout LAN 10/100/1000:

Pin	Name	Description
1	LAN-0	LAN channel 0 plus
2	LAN-0#	LAN channel 0 minus
3	LAN-1	LAN channel 1 plus
4	LAN-2	LAN channel 2 plus
5	LAN-2#	LAN channel 2 minus
6	LAN-1#	LAN channel 1 minus
7	LAN-3	LAN channel 3 plus
8	LAN-3#	LAN channel 3 minus

3.2.4 Audio Connectors

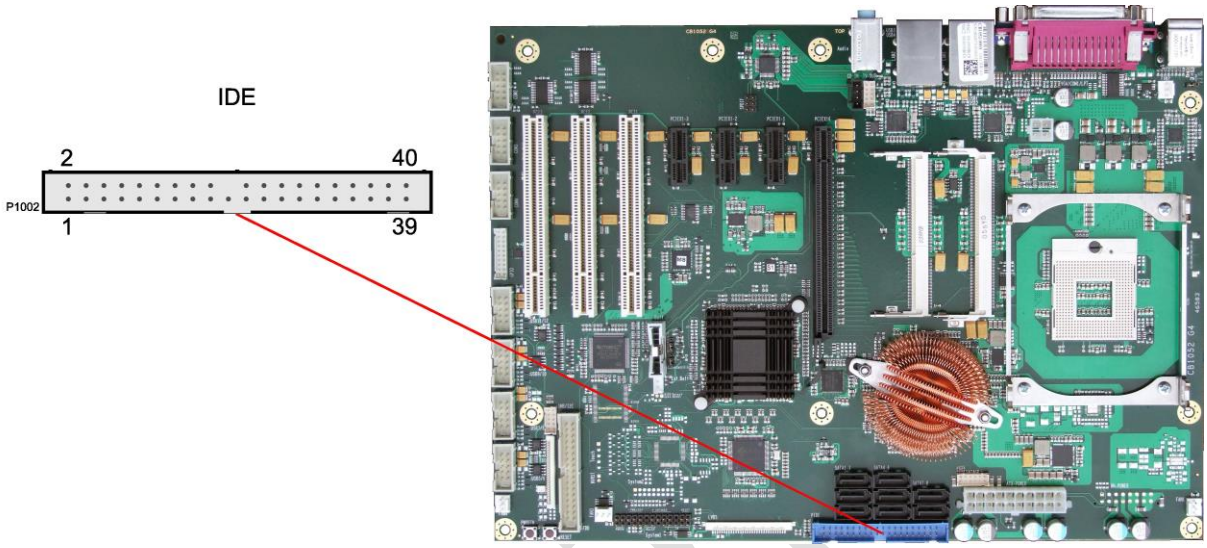
Line-in, line-out, and microphone signals are provided in the form of three 3,5mm-TRS-connectors.



3.3 SATA, PATA, FDD, Memory

3.3.1 IDE interface

To connect IDE devices you can plug a ribbon cable into the standard 40pin connector.

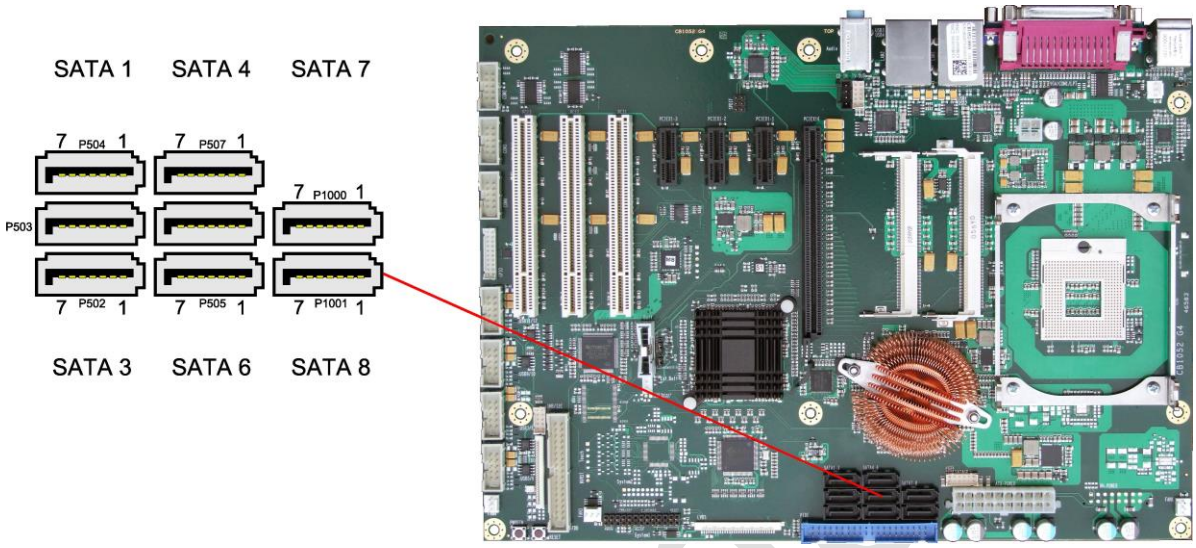


Pinout IDE interface:

Description	Name	Pin		Name	Description
reset	PRST#	1	2	GND	ground
data bit 7	PDD7	3	4	PDD8	data bit 8
data bit 6	PDD6	5	6	PDD9	data bit 9
data bit 5	PDD5	7	8	PDD10	data bit 10
data bit 4	PDD4	9	10	PDD11	data bit 11
data bit 3	PDD3	11	12	PDD12	data bit 12
data bit 2	PDD2	13	14	PDD13	data bit 13
data bit 1	PDD1	15	16	PDD14	data bit 14
data bit 0	PDD0	17	18	PDD15	data bit 15
ground	GND	19	20	N/C	coded
DMA request signal	PDDREQ	21	22	GND	ground
write signal	PDIOW#	23	24	GND	ground
read signal	PDIOR#	25	26	GND	ground
ready signal	PDRDY	27	28	N/C	reserved
DMA acknowledge signal	PDDACK#	29	30	GND	ground
interrupt signal	PDIRQ	31	32	N/C	reserved
address bit 1	PDA1	33	34	PDMA66EN	enable UDMA66
address bit 0	PDA0	35	36	PDA2	address bit 2
chip select signal 0	PDSC0#	37	38	PDCS1#	chip select signal 1
LED	PHDLED	39	40	GND	ground

3.3.2 SATA interfaces

Eight SATA connectors are available to connect SATA devices.



Pinout SATA:

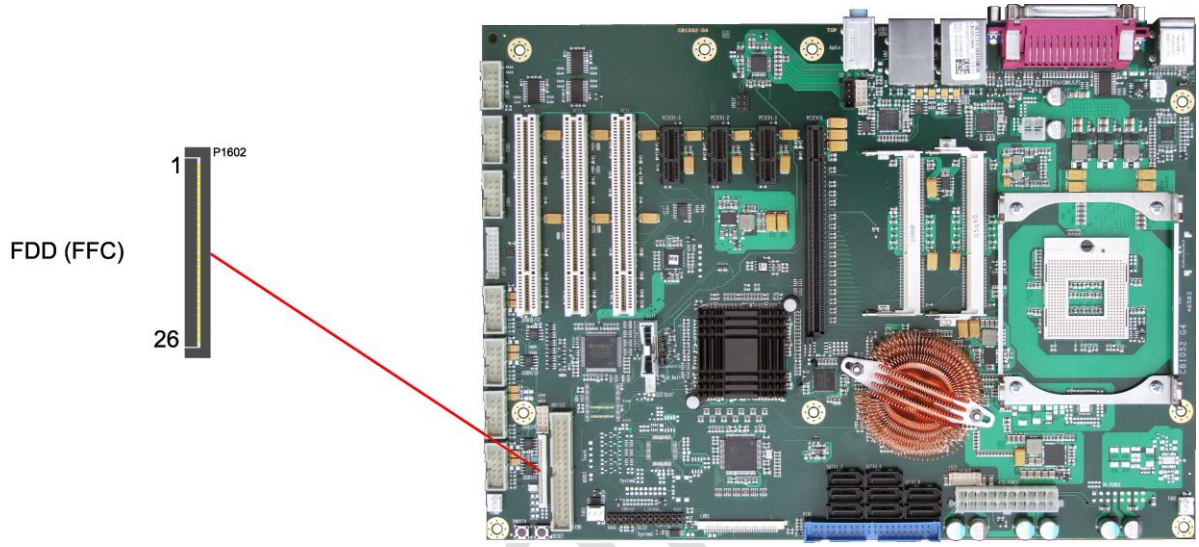
Pin	Name	Description
1	GND	ground
2	SATATX	SATA transmit +
3	SATATX#	SATA transmit -
4	GND	ground
5	SATARX	SATA receive -
6	SATARX#	SATA receive +
7	GND	ground

3.3.3 Floppy interface

A floppy drive can be attached in one of two alternative ways: One is a standard 2x17-pin connector (FCI 75869-306LF) for ribbon cables, the other is a 26-pin connector (JST 26FMZ-BT) for Flat Flex cables (FFC).

CAUTION

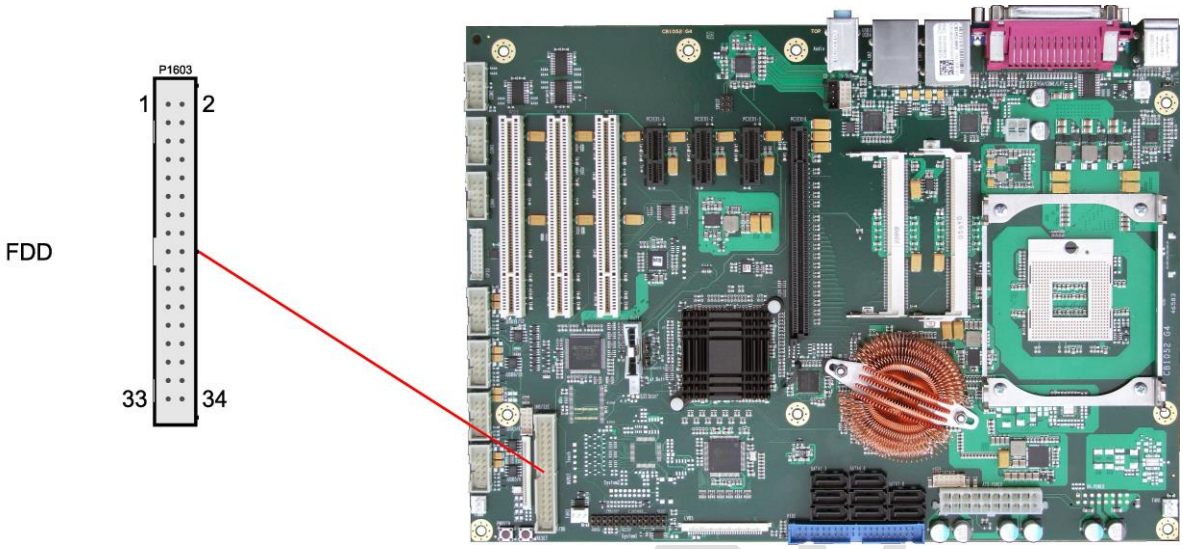
The two connectors can only be used one at a time.



Pinout FFC connector (FDD):

Pin	Name	Description
1	VCC	5 volt supply
2	IDX#	index
3	VCC	5 volt supply
4	DR0#	drive sel 0
5	VCC	5 volt supply
6	DC#	disk change
7	N/C	reserved
8	N/C	reserved
9	N/C	reserved
10	MT0#	motor enable 0
11	N/C	reserved
12	DIR#	direction
13	N/C	reserved
14	STP#	step
15	GND	ground
16	WD#	write data
17	GND	ground
18	WE#	write enable
19	GND	ground
20	TR0#	track 0
21	GND	ground
22	WPRT#	write protect
23	GND	ground
24	RDATA#	read data
25	GND	ground

Pin	Name	Description
26	HDSL#	head select

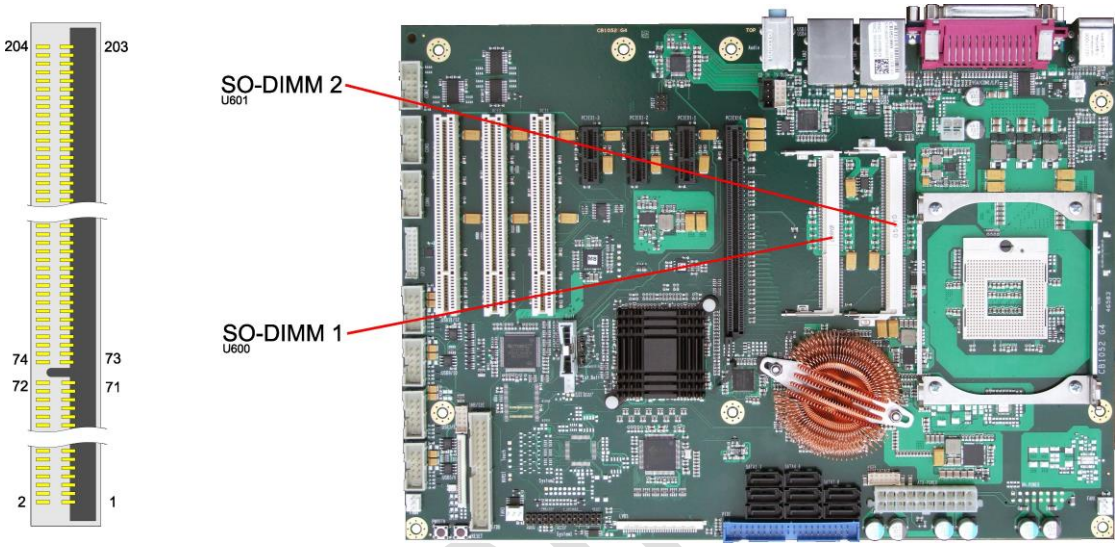


Pinout FDD 2x17 pin connector:

Description	Name	Pin		Name	Description
ground	GND	1	2	DRVDEN0	drive density sel 0
ground	GND	3	4	N/C	reserved
ground	GND	5	6	DRVDEN1	drive density sel 1
ground	GND	7	8	IDX#	index
ground	GND	9	10	MT0#	motor enable 0
ground	GND	11	12	DR1#	drive sel 1
ground	GND	13	14	DR0#	drive sel 0
ground	GND	15	16	MT1#	motor enable 1
ground	GND	17	18	DIR#	direction
ground	GND	19	20	STP#	step
ground	GND	21	22	WD#	write data
ground	GND	23	24	WE#	write enable
ground	GND	25	26	TR0#	track 0
ground	GND	27	28	WPRT#	write protect
reserved	N/C	29	30	RDATA#	read data
ground	GND	31	32	HDSL#	head select
reserved	N/C	33	34	DC#	disk change

3.3.4 Memory

The CB1052 is equipped with two SO-DIMM204 sockets for DDR3-1066-RAM. For technical and mechanical reasons it is possible that particular memory modules cannot be employed. Please ask your distributor for recommended memory modules
With currently available memory modules a memory extension up to 8 GByte is possible.
All timing parameters for different memory modules are automatically set by BIOS.



Pinout SO-DIMM204:

Description	Name	Pin		Name	Description
memory reference current	REF-DQ	1	2	GND	ground
ground	GND	3	4	DQ4	data 4
data 0	DQ0	5	6	DQ5	data 5
data 1	DQ1	7	8	GND	ground
ground	GND	9	10	DQS0#	data strobe 0 -
data mask 0	DM0	11	12	DQS0	data strobe 0 +
ground	GND	13	14	GND	ground
data 2	DQ2	15	16	DQ6	data 6
data 3	DQ3	17	18	DQ7	data 7
ground	GND	19	20	GND	ground
data 8	DQ8	21	22	DQ12	data 12
data 9	DQ9	23	24	DQ13	data 13
ground	GND	25	26	GND	ground
data strobe 1 -	DQS1#	27	28	DM1	data mask 1
data strobe 1 +	DQS1	29	30	RESET#	Reset
ground	GND	31	32	GND	ground
data 10	DQ10	33	34	DQ14	data 14
data 11	DQ11	35	36	DQ15	data 15
ground	GND	37	38	GND	ground
data 16	DQ16	39	40	DQ20	data 20
data 17	DQ17	41	42	DQ21	data 21
ground	GND	43	44	GND	ground
data strobe 2 -	DQS2#	45	46	DM2	data mask 2
data strobe 2 +	DQS2	47	48	GND	ground
ground	GND	49	50	DQ22	data 22
data 18	DQ18	51	52	DQ23	data 23

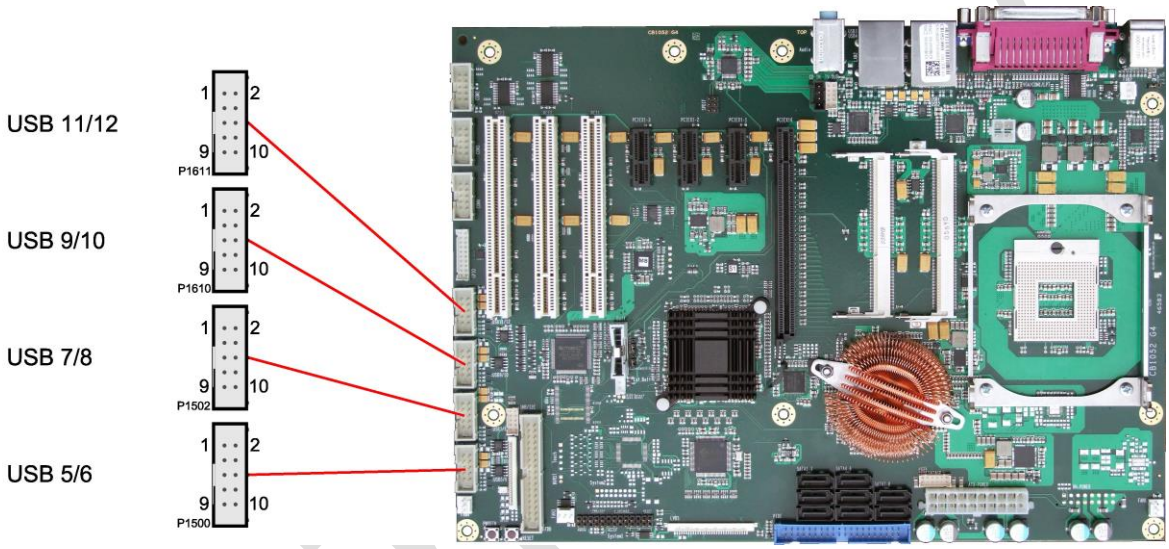
Description	Name	Pin		Name	Description
data 19	DQ19	53	54	GND	ground
ground	GND	55	56	DQ28	data 28
data 24	DQ24	57	58	DQ29	data 29
data 25	DQ25	59	60	GND	ground
ground	GND	61	62	DQS3#	data strobe 3 -
data mask 3	DQM3	63	64	DQS3	data strobe 3 +
ground	GND	65	66	GND	ground
data 26	DQ26	67	68	DQ30	data 30
data 27	DQ27	69	70	DQ31	data 31
ground	GND	71	72	GND	ground
clock enables 0	CKE0	73	74	CKE1	clock enables 1
1.5 volt supply	1.5V	75	76	1.5V	1.5 volt supply
reserved	N/C	77	78	(A15)	reserved
SDRAM bank 2	BA2	79	80	A14	address 14
1.5 volt supply	1.5V	81	82	1.5V	1.5 volt supply
address 12 (burst chop)	A12/BC#	83	84	A11	address 11
address 9	A9	85	86	A7	address 7
1.5 volt supply	1.5V	87	88	1.5V	1.5 volt supply
address 8	A8	89	90	A6	address 6
address 5	A5	91	92	A4	address 4
1.5 volt supply	1.5V	93	94	1.5V	1.5 volt supply
address 3	A3	95	96	A2	address 2
address 1	A1	97	98	A0	address 0
1.5 volt supply	1.5V	99	100	1.5V	1.5 volt supply
Clock 0 +	CK0	101	102	CK1	clock 1 +
Clock 0 -	CK0#	103	104	CK1#	clock 1 -
1.5 volt supply	1.5V	105	106	1.5V	1.5 volt supply
address 10 (auto precharge)	A10/AP	107	108	BA1	SDRAM bank 1
SDRAM Bank 0	BA0	109	110	RAS#	row address strobe
1.5 volt supply	1.5V	111	112	1.5V	1.5 volt supply
write enable	WE#	113	114	S0#	chip select 0
column address strobe	CAS#	115	116	ODT0	on die termination 0
1.5 volt supply	1.5V	117	118	1.5V	1.5 volt supply
address 13	A13	119	120	ODT1	on die termination 1
Chip Select 1	S1#	121	122	N/C	reserved
1.5 volt supply	1.5V	123	124	1.5V	1.5 volt supply
reserved	(TEST)	125	126	REF-CA	reference current
ground	GND	127	128	GND	ground
data 32	DQ32	129	130	DQ36	data 36
data 33	DQ33	131	132	DQ37	data 37
ground	GND	133	134	GND	ground
data strobe 4 -	DQS4#	135	136	DQM4	data mask 4
data strobe 4 +	DQS4	137	138	GND	ground
ground	GND	139	140	DQ38	data 38
data 34	DQ34	141	142	DQ39	data 39
data 35	DQ35	143	144	GND	ground
ground	GND	145	146	DQ44	data 44
data 40	DQ40	147	148	DQ45	data 45
data 41	DQ41	149	150	GND	ground
ground	GND	151	152	DQS5#	data strobe 5 -
data mask 5	DQM5	153	154	DQS5	data strobe 5 +
ground	GND	155	156	GND	ground
data 42	DQ42	157	158	DQ46	data 46
data 43	DQ43	159	160	DQ47	data 47
ground	GND	161	162	GND	ground

Description	Name	Pin		Name	Description
data 48	DQ48	163	164	DQ52	data 52
data 49	DQ49	165	166	DQ53	data 53
ground	GND	167	168	GND	ground
data strobe 6 -	DQS6#	169	170	DQM6	data mask 6
data strobe 6	DQS6	171	172	GND	ground
ground	GND	173	174	DQ54	data 54
data 50	DQ50	175	176	DQ55	data 55
data 51	DQ51	177	178	GND	ground
ground	GND	179	180	DQ60	data 60
data 56	DQ56	181	182	DQ61	data 61
data 57	DQ57	183	184	GND	ground
ground	GND	185	186	DQS7#	data strobe 7 -
data mask 7	DQM7	187	188	DQS7	data strobe 7 +
ground	GND	189	190	GND	ground
data 58	DQ58	191	192	DQ62	data 62
data 59	DQ59	193	194	DQ63	data 63
ground	GND	195	196	GND	ground
SPD address 0	SA0	197	198	EVENT#	Event
3.3 volt supply	3.3V	199	200	SDA	SMBus data
SPD address 1	SA1	201	202	SCL	SMBus clock
termination current	VTT	203	204	VTT	termination current

3.4 Internal Connectors

3.4.1 USB 5-12

The USB channels 5 to 12 are provided via four 2x5 pin connectors (FCI 75869-301LF, mating connector FCI 71600-610LF).
The USB channels support USB 2.0. You may note that the setting of USB keyboard or USB mouse support in the BIOS-setup is only necessary and advisable, if the OS offers no USB-support. BIOS-setup can be changed with a USB keyboard without enabling USB keyboard support. Running Windows with these features enabled may lead to significant performance or functionality limitations.
Every USB interface provides up to 500 mA current and is protected by an electronically resettable fuse.

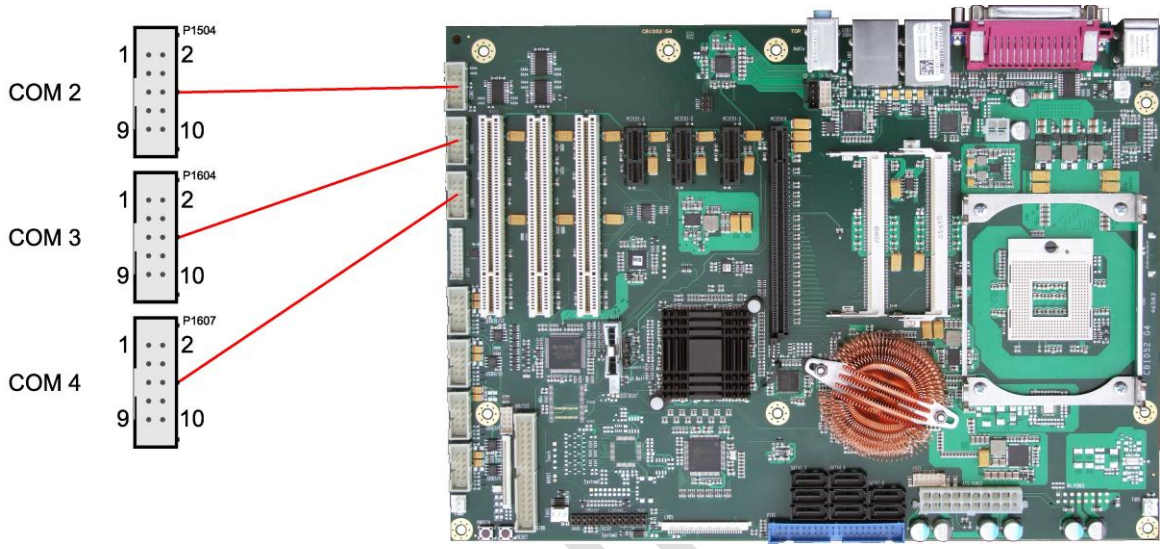


Pinout 2x5 pin connector USB x/y:

Description	Name	Pin		Name	Description
5 volt for USBx	VCC	1	2	VCC	5 volt for USBy
minus channel USBx	USBx#	3	4	USBy#	minus channel USBy
plus channel USBx	USBx	5	6	USBy	plus channel USBy
ground	GND	7	8	GND	ground
reserved	N/C	9	10	N/C	reserved

3.4.2 Serial ports COM2 to COM4

The three serial ports COM2 to COM4 are made available via a 2x5 pin connector each (FCI 75869-301LF, mating connector FCI 71600-610LF). According to the product order, TTL level signals or RS232 standard signals are provided.
The port address and the interrupt are set via the BIOS setup.

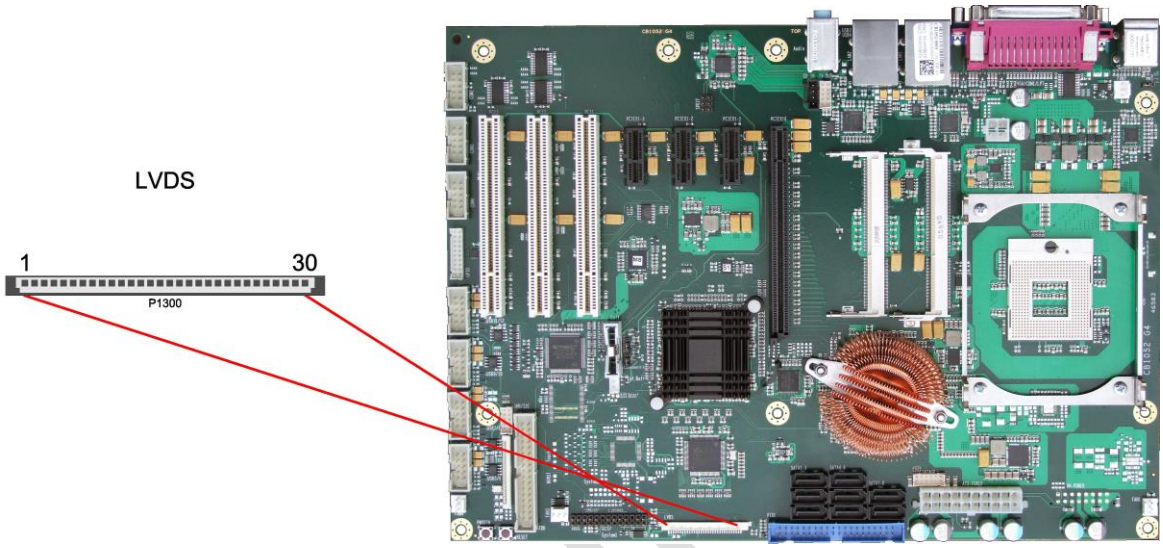


Pinout COM connector:

Description	Name	Pin		Name	Description
data carrier detect	DCD	1	2	DSR	data set ready
receive data	RXD	3	4	RTS	request to send
transmit data	TXD	5	6	CTS	clear to send
data terminal ready	DTR	7	8	RI	ring indicator
ground	GND	9	10	VCC	5 volt supply

3.4.3 LVDS

The board also offers the possibility to use displays with LVDS interface. These can be connected via a 30 pin flat-cable plug (JAE FI-X30S-HF-NPB, mating connector: FI-X30C(2)-NPB). Only shielded and twisted cables may be used. The display type is to be chosen over the BIOS setup. The connector has two additional shield pins S1 and S2 which are omitted in the pinout table below.



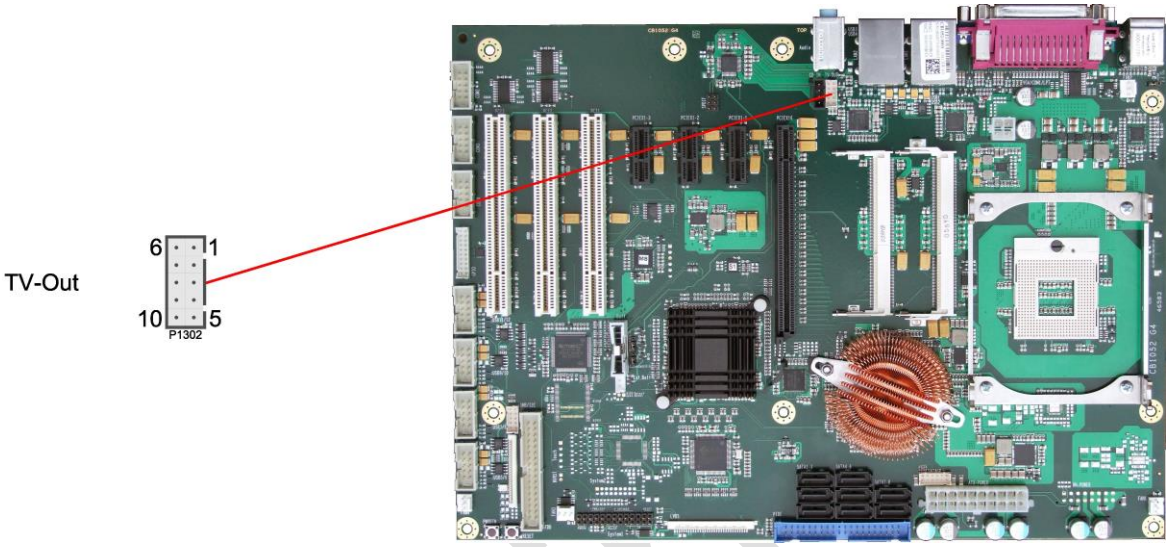
Pinout LVDS connector:

Pin	Name	Description
1	TXO00#	LVDS even data 0 -
2	TXO00	LVDS even data 0 +
3	TXO01#	LVDS even data 1 -
4	TXO01	LVDS even data 1 +
5	TXO02#	LVDS even data 2 -
6	TXO02	LVDS even data 2 +
7	GND	ground
8	TXO0C#	LVDS even clock -
9	TXO0C	LVDS even clock +
10	TXO03#	LVDS even data 3 -
11	TXO03	LVDS even data 3 +
12	TXO10#	LVDS odd data 0 -
13	TXO10	LVDS odd data 0 +
14	GND	ground
15	TXO11#	LVDS odd data 1 -
16	TXO11	LVDS odd data 1 +
17	GND	ground
18	TXO12#	LVDS odd data 2 -
19	TXO12	LVDS odd data 2 +
20	TXO1C#	LVDS odd clock -
21	TXO1C	LVDS odd clock +
22	TXO13#	LVDS odd data 3 -
23	TXO13	LVDS odd data 3 +
24	GND	ground
25	3.3V	3.3 volt supply
26	DDC_CLK	EDID clock for LCD
27	DDC_DAT	EDID data for LCD

Pin	Name	Description
28	FP_3.3V	switched 3.3 volt for display
29	FP_BL	switched 5 volt for backlight
30	VCC	5 volt supply

3.4.4 TV-Out

The CB1052 board provides TV-out signals through an 2x5 pin connector (JST B10B-PHDSSLFSN, mating connector: PHDR-10VS).

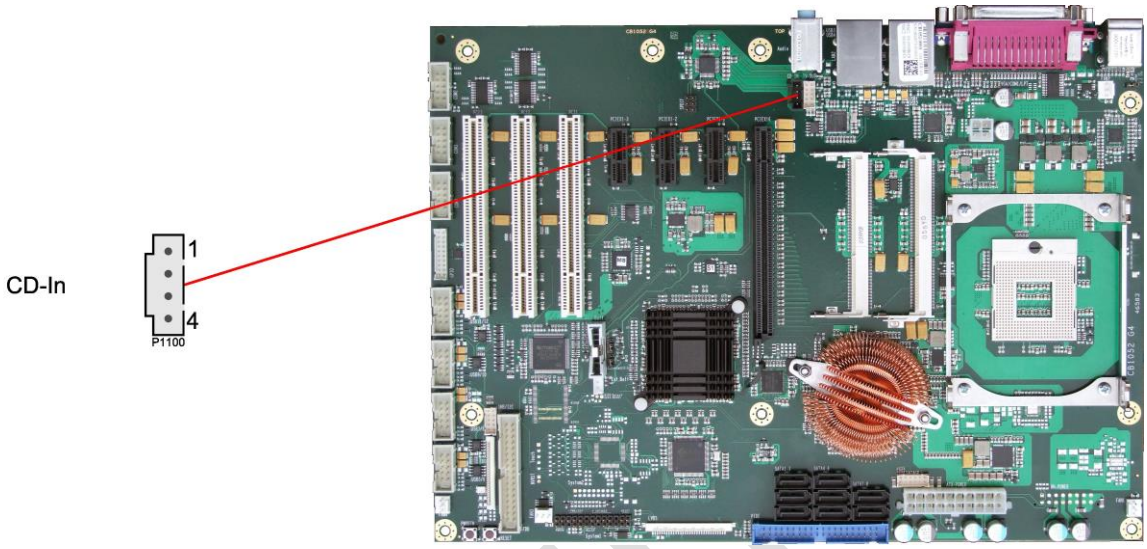


Pinout TV-out connector:

Description	Name	Pin		Name	Description
TVDAC channel A	TVDACA	1	6	3.3V	3.3 volt supply
TVDAC channel B	TVDACB	2	7	GND	ground
TVDAC channel C	TVDACC	3	8	GND	ground
TV select 0	TVSEL0	4	9	GND	ground
TV select 1	TVSEL1	5	10	VCC	5 volt supply

3.4.5 CD-In

In addition to the external TRS connectors mentioned above, the CB1052 offers an internal 4 pin connector (Foxconn HF1104E-P1), providing customers with even more possibilities to connect audio devices (analogue signals).

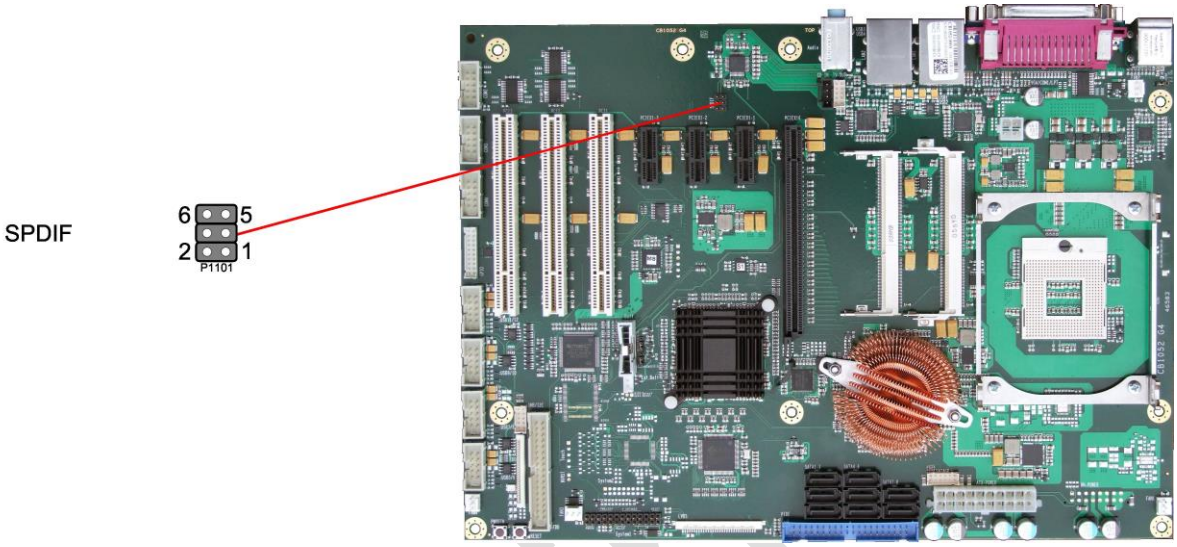


Pinout CD-in connector:

Pin	Name	Description
1	CD_L	CD left channel
2	CD_GND	CD ground
3	CD_GND	CD ground
4	CD_R	CD right channel

3.4.6 S/PDIF

For digital audio signals an SPDIF interface is available, which can be accessed using an internal 2x3 pin IDC socket connector with a spacing of 2,54mm.

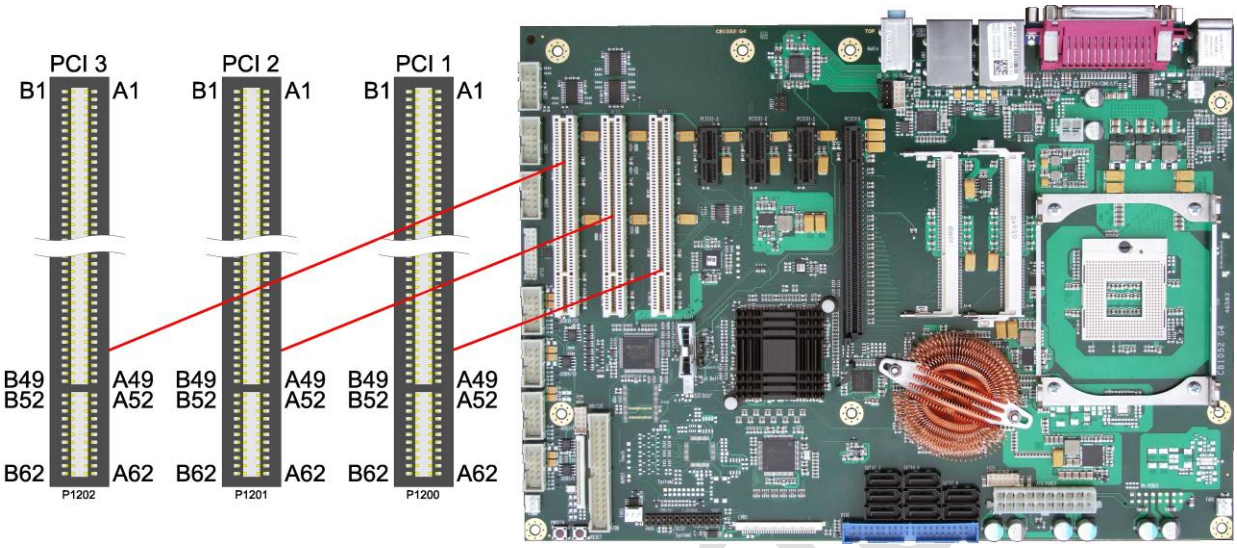


Pinout SPDIF connector:

Description	Name	Pin		Name	Description
ground	GND	1	2	SPDIFO	SPDIF out
3.3 volt supply	3,3V	3	4	VCC	5 volt supply
ground	GND	5	6	SPDIFI	SPDIF in

3.4.7 PCI interfaces

There are three standard PCI slots available on the CB1052.



NOTE

Please note that due to the nature of the PCI bus some signals in the following table are different from one PCI slot to the other. This applies to the test signals (A4, B4), the interrupt signals (A6, A7, B7, B8), the clock signal (B16), the grant signal (A17), the request signal (B18), and the ID-select signal (A26).

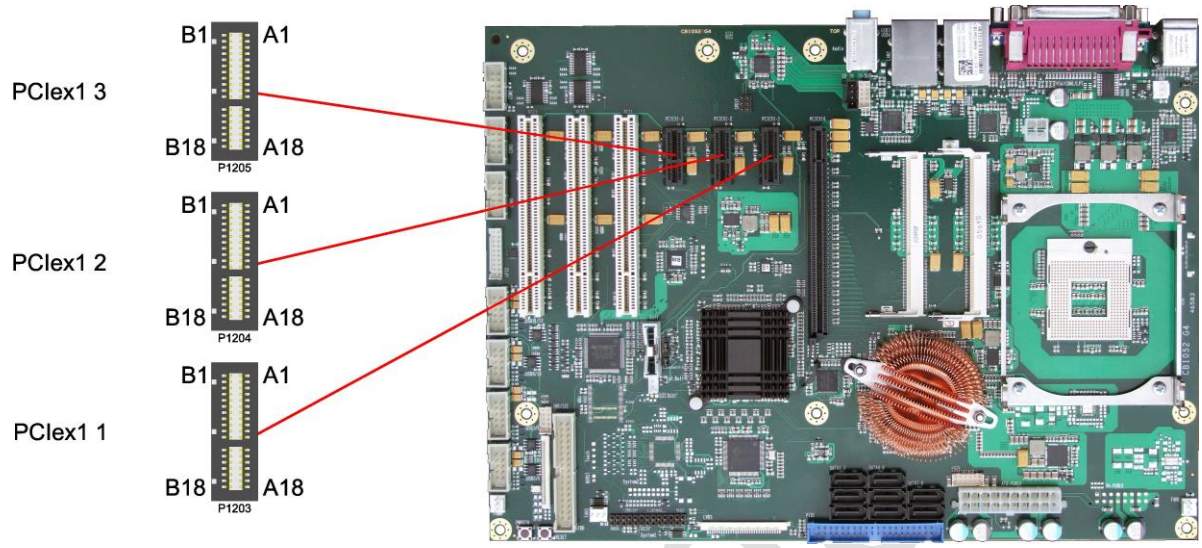
Pinout PCI slot:

Description	Name	Pin		Name	Description
test logic reset	TRST#	A1	B1	-12V	-12 volt supply
12 volt supply	12V	A2	B2	TCK	test clock
test mde select	TMS	A3	B3	GND	ground
test data input	TDI	A4	B4	TDO	test data output
5 volt supply	VCC	A5	B5	VCC	5 volt supply
interrupt A	INTA#	A6	B6	VCC	5 volt supply
interrupt C	INTC#	A7	B7	INTB#	interrupt B
5 volt supply	VCC	A8	B8	INTD#	interrupt D
reserved	N/C	A9	B9	GND	ground
5 volt supply	VCC	A10	B10	N/C	reserved
reserved	N/C	A11	B11	GND	ground
ground	GND	A12	B12	GND	ground
ground	GND	A13	B13	GND	ground
3.3 volt supply	3.3VAux	A14	B14	N/C	reserved
PCI reset	PRST#	A15	B15	GND	ground
5 volt supply	VCC	A16	B16	PCLK	clock
grant PCI use	GNT#	A17	B17	GND	ground
ground	GND	A18	B18	REQ#	request
power management event	PME#	A19	B19	VCC	5 volt supply
address/data 30	AD30	A20	B20	AD31	address/data 31
3.3 volt supply	3.3V	A21	B21	AD29	address/data 29
address/data 28	AD28	A22	B22	GND	ground
address/data 26	AD26	A23	B23	AD27	address/data 27
ground	GND	A24	B24	AD25	address/data 25

Description	Name	Pin		Name	Description
address/data 24	AD24	A25	B25	3.3V	3.3 volt supply
init device select	IDSEL	A26	B26	CBE3#	command, byte enable 3
3.3 volt supply	3.3V	A27	B27	AD23	address/data 23
address/data 22	AD22	A28	B28	GND	ground
address/data 20	AD20	A29	B29	AD21	address/data 21
ground	GND	A30	B30	AD19	address/data 19
address/data 18	AD18	A31	B31	3.3V	3.3 volt supply
address/data 16	AD16	A32	B32	AD17	address/data 17
3.3 volt supply	3.3V	A33	B33	CBE2#	command, byte enable 2
cycle frame	FRAME#	A34	B34	GND	ground
ground	GND	A35	B35	IRDY#	initiator ready
Target Ready	TRDY#	A36	B36	3.3V	3.3 volt supply
ground	GND	A37	B37	DEVSEL#	device select
stop request by target	STOP#	A38	B38	GND	ground
3.3 volt supply	3.3V	A39	B39	PLOCK#	lock bus
SMBus clock PCI	SMBCLK	A40	B40	PERR#	parity error
SMBus data PCI	SMBDAT	A41	B41	3.3V	3.3 volt supply
ground	GND	A42	B42	SERR#	system error
parity	PAR	A43	B43	3.3V	3.3 volt supply
address/data 15	AD15	A44	B44	CBE1#	command, byte enable 1
3.3 volt supply	3.3V	A45	B45	AD14	address/data 14
address/data 13	AD13	A46	B46	GND	ground
address/data 11	AD11	A47	B47	AD12	address/data 12
ground	GND	A48	B48	AD10	address/data 10
address/data 9	AD9	A49	B49	GND	ground
coded	N/C	A50	B50	N/C	coded
coded	N/C	A51	B51	N/C	coded
command, byte enable 0	CBEO#	A52	B52	AD8	address/data 8
3.3 volt supply	3.3V	A53	B53	AD7	address/data 7
address/data 6	AD6	A54	B54	3.3V	3.3 volt supply
address/data 4	AD4	A55	B55	AD5	address/data 5
ground	GND	A56	B56	AD3	address/data 3
address/data 2	AD2	A57	B57	GND	ground
address/data 0	AD0	A58	B58	AD1	address/data 1
5 volt supply	VCC	A59	B59	VCC	5 volt supply
reserved	N/C	A60	B60	VCC	5 volt supply
5 volt supply	VCC	A61	B61	VCC	5 volt supply
5 volt supply	VCC	A62	B62	VCC	5 volt supply

3.4.8 PCI-express interfaces (x1)

The CB1052 board has three slots for PCIe-x1 expansion cards.



NOTE

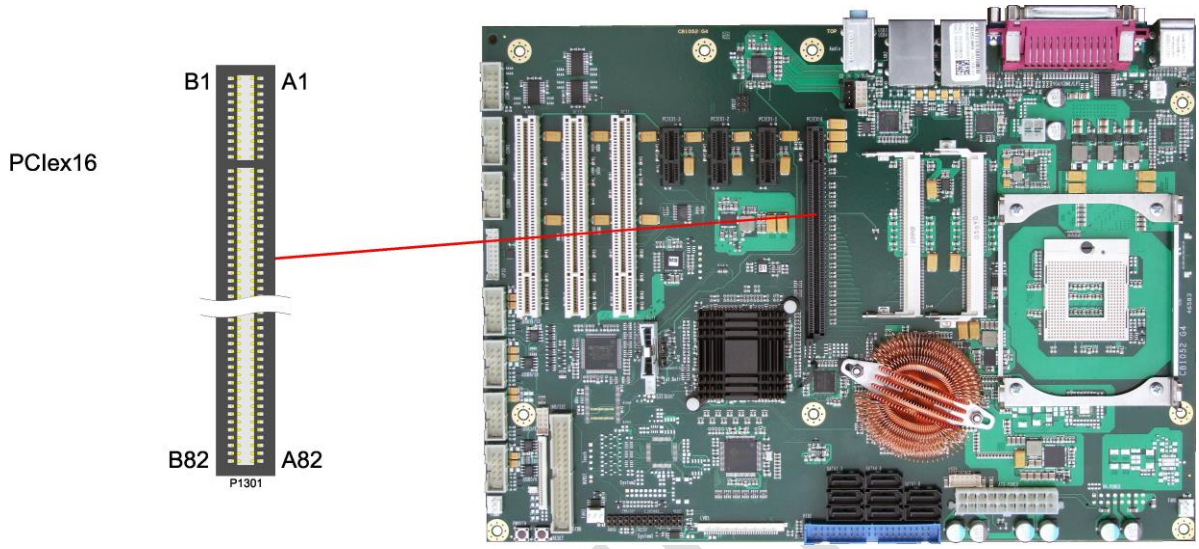
Please note that some signals in the following table are different from one PCIe slot to the other. This applies to the clock signals (A13, A14), the receive signals (A16, A17), and the transmit signals (B14, B15).

Pinout PCI-express-x1 connector:

Description	Name	Pin		Name	Description
hot plug detect 1	PRSNT1#	A1	B1	12V	12 volt supply
12 volt supply	12V	A2	B2	12V	12 volt supply
12 volt supply	12V	A3	B3	N/C	reserved
ground	GND	A4	B4	GND	ground
reserved	N/C	A5	B5	SMBCLK	SMBus clock PCIe
reserved	N/C	A6	B6	SMBDAT	SMBus data PCIe
reserved	N/C	A7	B7	GND	ground
reserved	N/C	A8	B8	3.3V	3.3 volt supply
3.3 volt supply	3.3V	A9	B9	N/C	reserved
3.3 volt supply	3.3V	A10	B10	S3.3V	3.3V standby-supply
PCIe reset	PERST#	A11	B11	PEWAKE#	link reactivation
ground	GND	A12	B12	N/C	reserved
reference clock +	REFCLK	A13	B13	GND	ground
reference clock -	REFCLK#	A14	B14	PET0	transmit lane 0 +
ground	GND	A15	B15	PET0#	transmit lane 0 -
receive lane 0 +	PER0	A16	B16	GND	ground
receive lane 0 -	PER0#	A17	B17	PRSNT2#	hot plug detect 2
ground	GND	A18	B18	GND	ground

3.4.9 PCI-express interface (x16)

One slot for PCI-express-x16-cards makes the expansion options on the CB1052 complete. You can use this slot either for PCIe-x16 graphic adapters or for ADD2 cards (SDVO). This slot also acommodates x1 or x4 expansion cards.



NOTE

SDVO signals are listed below in a table of their own.

Pinout PCI-express-x16 connector:

Description	Name	Pin		Name	Description
hot plug detect 1	PRSNT1#	A1	B1	12V	12 volt supply
12 volt supply	12V	A2	B2	12V	12 volt supply
12 volt supply	12V	A3	B3	N/C	reserved
ground	GND	A4	B4	GND	ground
reserved	N/C	A5	B5	SMBCLK	SMBus clock PCIe
reserved	N/C	A6	B6	SMBDAT	SMBus data PCIe
reserved	N/C	A7	B7	GND	ground
reserved	N/C	A8	B8	3.3V	3.3 volt supply
3.3 volt supply	3.3V	A9	B9	N/C	reserved
3.3 volt supply	3.3V	A10	B10	S3.3V	3.3V standby-supply
PCIe reset	PERST#	A11	B11	PEWAKE#	link reactivation
ground	GND	A12	B12	N/C	reserved
reference clock +	REFCLK	A13	B13	GND	ground
reference clock -	REFCLK#	A14	B14	PET0	transmit lane 0 +
ground	GND	A15	B15	PET0#	transmit lane 0 -
receive lane 0 +	PER0	A16	B16	GND	ground
receive lane 0 -	PER0#	A17	B17	PRSNT2#	hot plug detect 2
ground	GND	A18	B18	GND	ground
reserved	N/C	A19	B19	PET1	transmit lane 1 +
ground	GND	A20	B20	PET1#	transmit lane 1 -
receive lane 1 +	PER1	A21	B21	GND	ground
receive lane 1 -	PER1#	A22	B22	GND	ground
ground	GND	A23	B23	PET2	transmit lane 2 +
ground	GND	A24	B24	PET2#	transmit lane 2 -

Description	Name	Pin		Name	Description
receive lane 2 +	PER2	A25	B25	GND	ground
receive lane 2 -	PER2#	A26	B26	GND	ground
ground	GND	A27	B27	PET3	transmit lane 3 +
ground	GND	A28	B28	PET3#	transmit lane 3 -
receive lane 3 +	PER3	A29	B29	GND	ground
receive lane 3 -	PER3#	A30	B30	N/C	reserved
ground	GND	A31	B31	PRSNT2#	hot plug detect 2
reserved	N/C	A32	B32	GND	ground
reserved	N/C	A33	B33	PET4	transmit lane 4 +
ground	GND	A34	B34	PET4#	transmit lane 4 -
receive lane 4 +	PER4	A35	B35	GND	ground
receive lane 4 -	PER4#	A36	B36	GND	ground
ground	GND	A37	B37	PET5	transmit lane 5 +
ground	GND	A38	B38	PET5#	transmit lane 5 -
receive lane 5 +	PER5	A39	B39	GND	ground
receive lane 5 -	PER5#	A40	B40	GND	ground
ground	GND	A41	B41	PET6	transmit lane 6 +
ground	GND	A42	B42	PET6#	transmit lane 6 -
receive lane 6 +	PER6	A43	B43	GND	ground
receive lane 6 -	PER6#	A44	B44	GND	ground
ground	GND	A45	B45	PET7	transmit lane 7 +
ground	GND	A46	B46	PET7#	transmit lane 7 -
receive lane 7 +	PER7	A47	B47	GND	ground
receive lane 7 -	PER7#	A48	B48	PRSNT2#	hot plug detect 2
ground	GND	A49	B49	GND	ground
reserved	N/C	A50	B50	PET8	transmit lane 8 +
ground	GND	A51	B51	PET8#	transmit lane 8 -
receive lane 8 +	PER8	A52	B52	GND	ground
receive lane 8 -	PER8#	A53	B53	GND	ground
ground	GND	A54	B54	PET9	transmit lane 9 +
ground	GND	A55	B55	PET9#	transmit lane 9 -
receive lane 9 +	PER9	A56	B56	GND	ground
receive lane 9 -	PER9#	A57	B57	GND	ground
ground	GND	A58	B58	PET10	transmit lane 10 +
ground	GND	A59	B59	PET10#	transmit lane 10 -
receive lane 10 +	PER10	A60	B60	GND	ground
receive lane 10 -	PER10#	A61	B61	GND	ground
ground	GND	A62	B62	PET11	transmit lane 11 +
ground	GND	A63	B63	PET11#	transmit lane 11 -
receive lane 11 +	PER11	A64	B64	GND	ground
receive lane 11 -	PER11#	A65	B65	GND	ground
ground	GND	A66	B66	PET12	transmit lane 12 +
ground	GND	A67	B67	PET12#	transmit lane 12 -
receive lane 12 +	PER12	A68	B68	GND	ground
receive lane 12 -	PER12#	A69	B69	GND	ground
ground	GND	A70	B70	PET13	transmit lane 13 +
ground	GND	A71	B71	PET13#	transmit lane 13 -
receive lane 13+	PER13	A72	B72	GND	ground
receive lane 13-	PER13#	A73	B73	GND	ground
ground	GND	A74	B74	PET14	transmit lane 14 +
ground	GND	A75	B75	PET14#	transmit lane 14 -
receive lane 14 +	PER14	A76	B76	GND	ground
receive lane 14 -	PER14#	A77	B77	GND	ground
ground	GND	A78	B78	PET15	transmit lane 15 +
ground	GND	A79	B79	PET15#	transmit lane 15 -

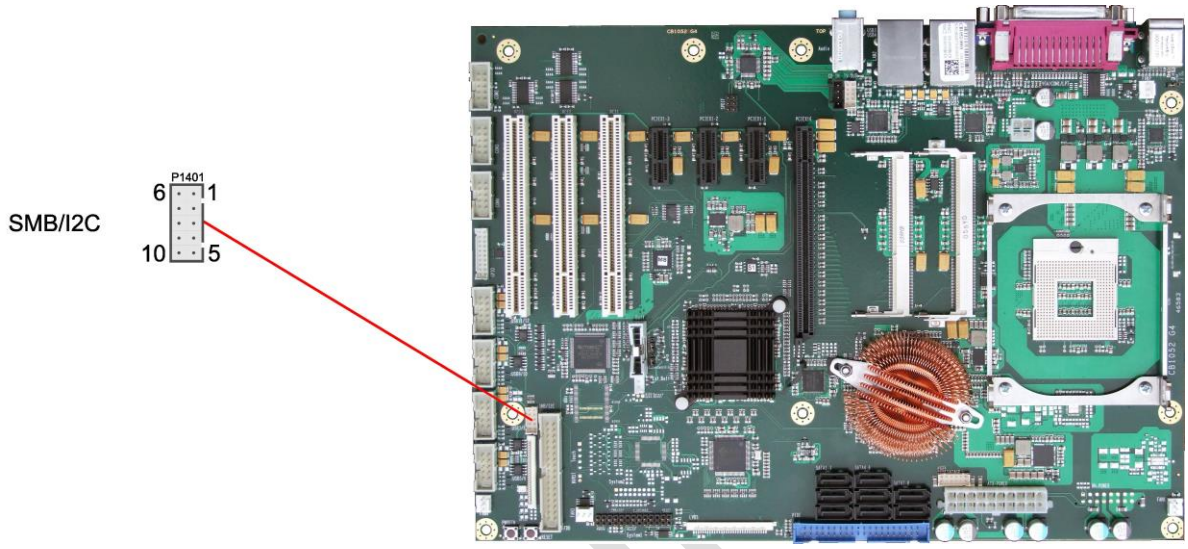
Description	Name	Pin		Name	Description
receive lane 15 +	PER15	A80	B80	GND	ground
receive lane 15 -	PER15#	A81	B81	N/C	reserved
ground	GND	A82	B82	N/C	reserved

Pinout PCI-express-x16 connector, translation SDVO signals (pins not used for this purpose are omitted):

Description	Name	Pin		Name	Description
DDPC-CLK	PRSNT1#	A1	B1		
		A14	B14	PET0	SDVOB-RED
		A15	B15	PET0#	SDVOB-RED#
SDVO_TVCLKI	PER0	A16	B16		
SDVO_TVCLKI#	PER0#	A17	B17	PRSNT2#	SDVO-CLK
		A19	B19	PET1	SDVOB-GREEN
		A20	B20	PET1#	SDVOB-GREEN#
SDVOB_INT	PER1	A21	B21		
SDVOB_INT#	PER1#	A22	B22		
		A23	B23	PET2	SDVOB-BLUE
		A24	B24	PET2#	SDVOB-BLUE#
SDVO_FLDSTALL	PER2	A25	B25		
SDVO_FLDSTALL#	PER2#	A26	B26		
		A27	B27	PET3	SDVOB-CLK
		A28	B28	PET3#	SDVOB-CLK#
		A31	B31	PRSNT2#	SDVO-DAT
		A33	B33	PET4	SDVOC-RED
		A34	B34	PET4#	SDVOC-RED#
		A37	B37	PET5	SDVOC-GREEN
		A38	B38	PET5#	SDVOC-GREEN#
SDVOC_INT	PER5	A39	B39		
SDVOC_INT#	PER5#	A40	B40		
		A41	B41	PET6	SDVOC_BLUE
		A42	B42	PET6#	SDVOC_BLUE#
		A45	B45	PET7	SDVOC_CLK
		A46	B46	PET7#	SDVOC_CLK#
		A48	B48	PRSNT2#	SDVO+PCIe
		A81	B81	PRSNT2#	DDPC-DAT

3.4.10 SMB/I2C

The CB1052 can communicate with external devices via the SMBus protocol or the I2C protocol. The signals for these protocols are available through a 2x5 pin connector (JST B10B-PHDSSLFSN, mating connector: PHDR-10VS). The SMBus signals are processed by the chipset, the I2C signals are processed by the SIO unit.

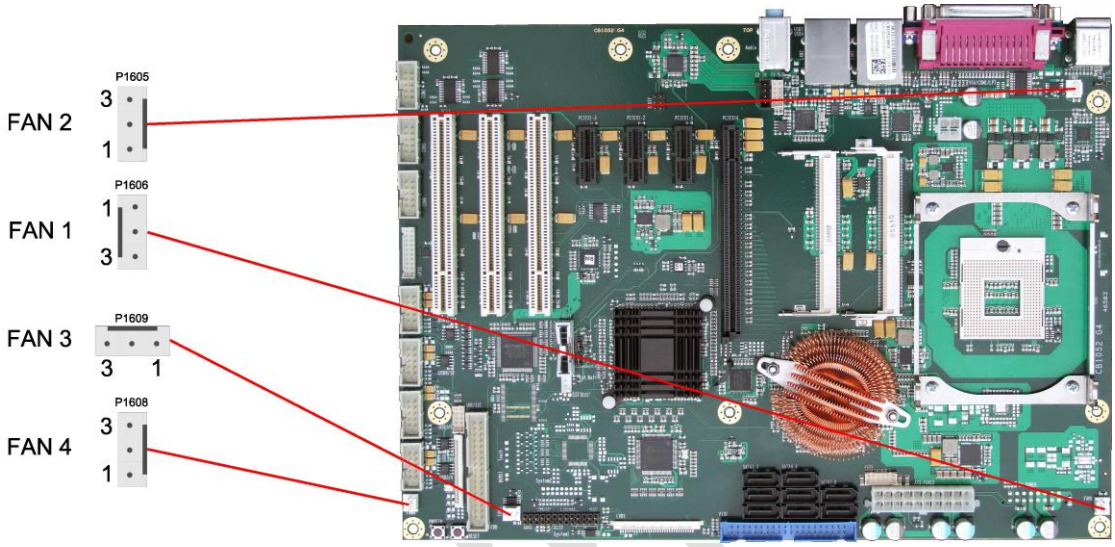


Pinout SMBus/I2C connector:

Description	Name	Pin		Name	Description
3.3 volt supply	3.3V	1	6	GND	ground
SMBus clock	SMBCLK	2	7	SMBDAT	SMBus data
SMBus alarm	SMBALRT#	3	8	SVCC	standby supply 5V
I2C bus clock	I2CLK	4	9	I2DAT	I2C bus data
5 volt supply	VCC	5	10	GND	ground

3.4.11 Fan Connectors

Four 3 pin connectors are available for controlling and monitoring external fans (12 volt). For the monitoring the fans must provide a corresponding speed signal.



Pinout fan connector:

Pin	Name	Description
1	GND	ground
2	12V	12 volt supply regulated
3	TACHO	fan monitoring signal

NOTE

The FAN4 connector doesn't have pin 3 connected (N/C).

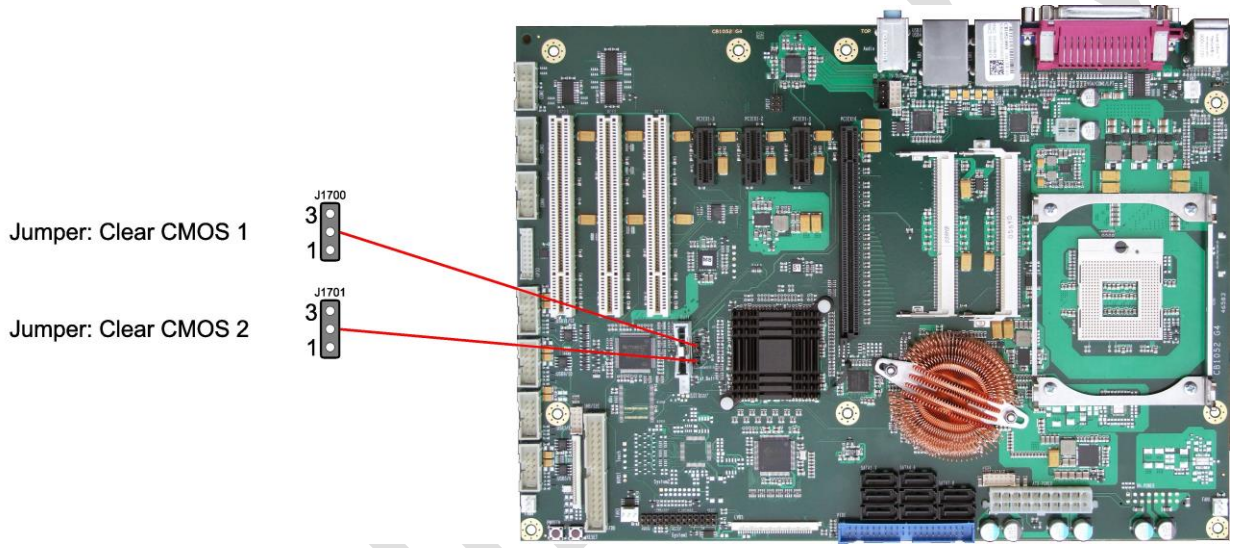
3.5 Jumper Settings

3.5.1 Clear CMOS

In case the board doesn't start up anymore and BIOS setup is inaccessible there is a "last resort": You can use the "Clear CMOS" jumpers to reset all CMOS settings to factory defaults. In order to do so you need to shut down the computer, change the jumper setting from normal (pins 1 & 2 short) to "Clear CMOS" (pins 2 & 3 short) for both jumpers, wait a few seconds, put the jumpers back into normal position and reboot.

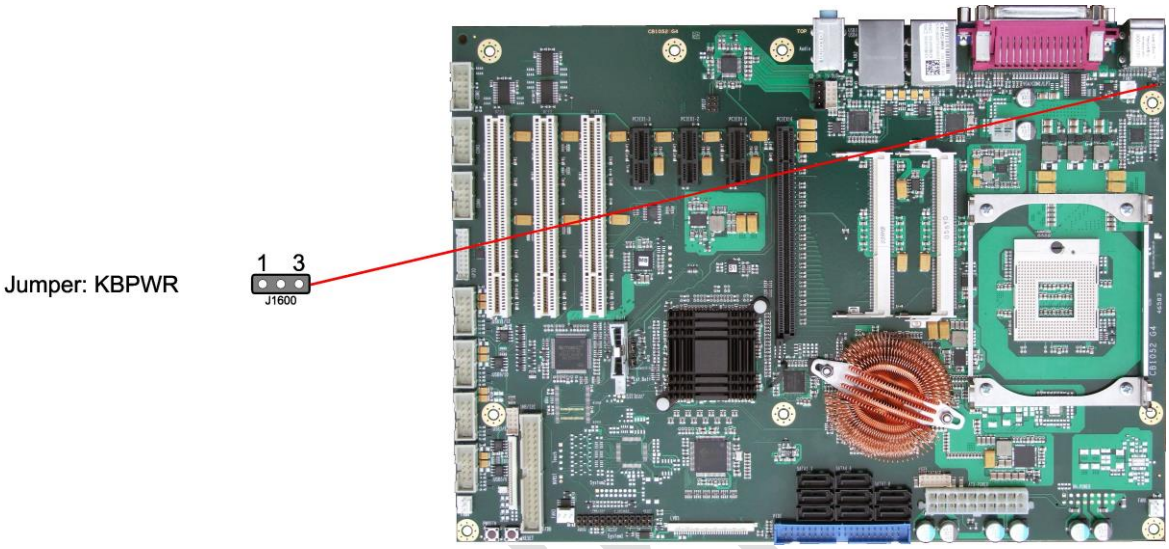
CAUTION

If you reset the CMOS this does not only bring all settings made in BIOS setup back to default values, it also clears the date and time information stored in CMOS. So don't forget that, after the Clear CMOS procedure, you will have to set the clock again.



3.5.2 Jumper: Keyboard Power (KBPWR)

Power supply for keyboard and mouse can be provided in two different ways, either using normal power supply VCC or standby power supply SVCC. You can switch between the two by using the KBPWR jumper. For VCC you need to short pins 1 and 2, for SVCC please short pins 2 and 3.



4 BIOS Settings

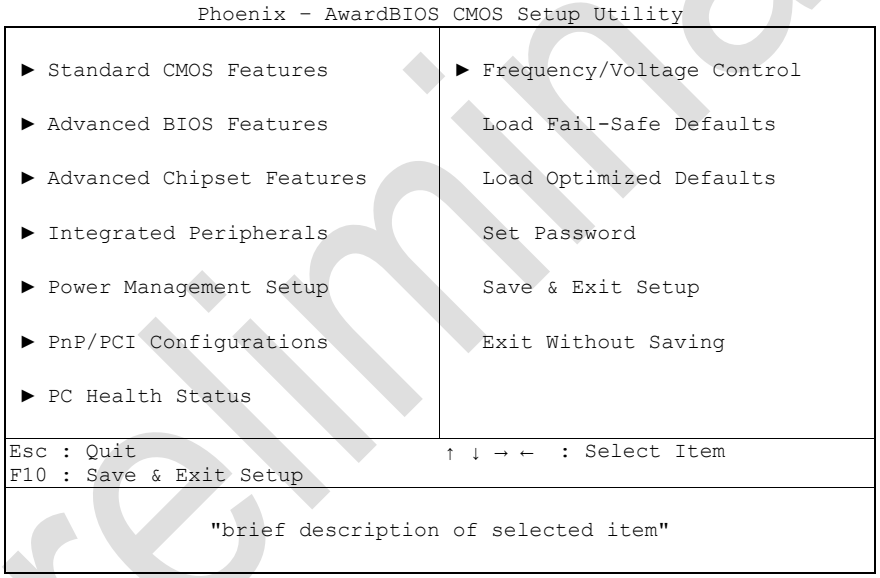
4.1 Remarks for Setup Use

In a setup page, standard values for its setup entries can be loaded. Fail-safe defaults are loaded with F6 and optimized defaults are loaded with F7. These standard values are independent of the fact that a board has successfully booted with a setup setting before.
This is different if these defaults are called from the Top Menu. Once a setup setting was saved, which subsequently leads to a successful boot process, those values are loaded as default for all setup items afterwards.
See also the chapters “Load Fail-Safe Defaults" (5.10) and “Load Optimized Defaults” (5.11).

NOTE

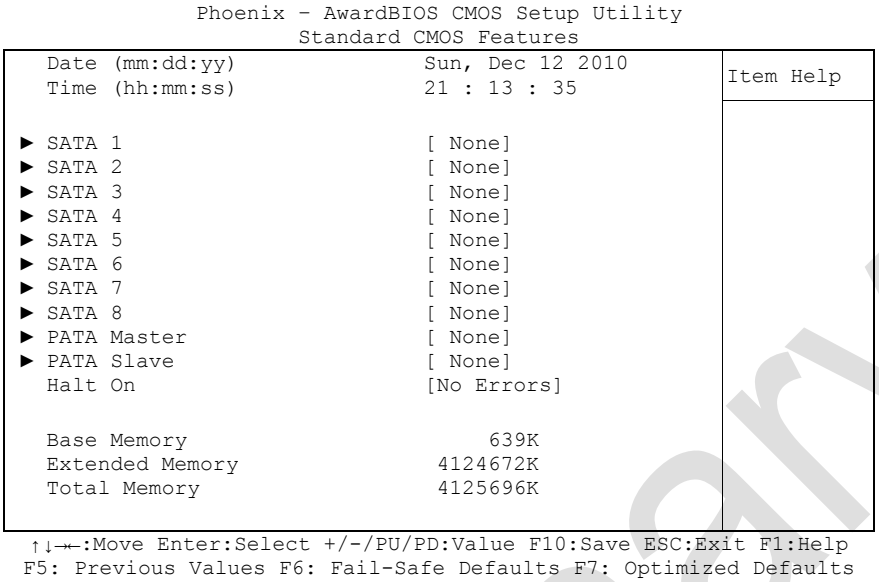
BIOS features and setup options are subject to change without notice. The settings displayed in the screenshots on the following pages are meant to be examples only. They do not represent the recommended settings or the default settings. Determination of the appropriate settings is dependent upon the particular application scenario in which the board is used.

4.2 Top Level Menu



The sign „►“ in front of an item means that there is a sub menu.
The „x“ sign in front of an item means, that the item is disabled but can be enabled by changing or selecting some other item (usually somewhere above the disabled item on the same screen).
Use the arrow buttons to navigate from one item to another. For selecting an item press Enter which will open either a sub menu or a dialog screen.

4.3 Standard CMOS Features



- ✓ **Date (mm:dd:yy)**
  Options: mm: month
  dd: day
  yy: year

- ✓ **Time (hh:mm:ss)**
  Options: hh: hours
  mm: minutes
  ss: seconds

- ✓ **PATA Master**
  Sub menu: see "PATA channel" (page 54)

- ✓ **PATA Slave**
  Sub menu: see "PATA channel" (page 54)

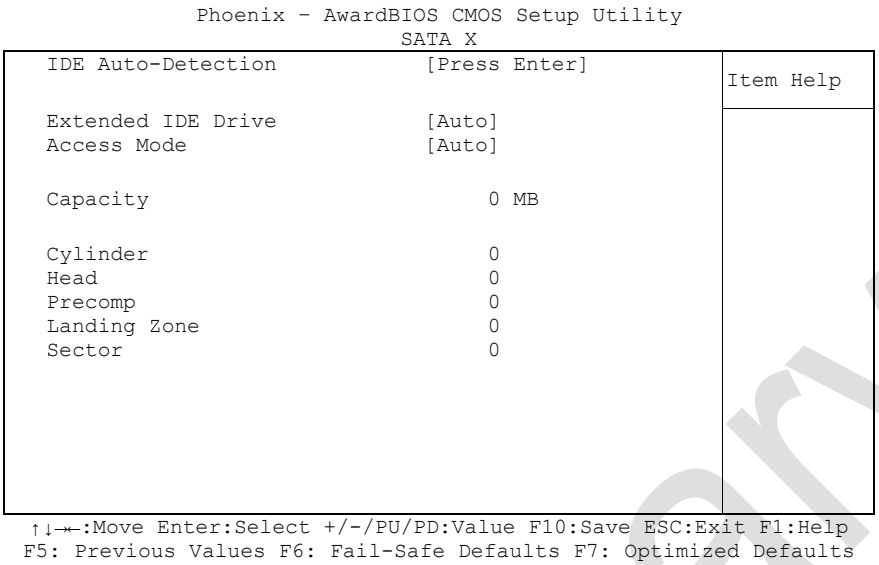
- ✓ **Halt On**
  Options: All Errors / No Errors / All, But Keyboard

- ✓ **Base Memory**
  Options: none

- ✓ **Extended Memory**
  Options: none

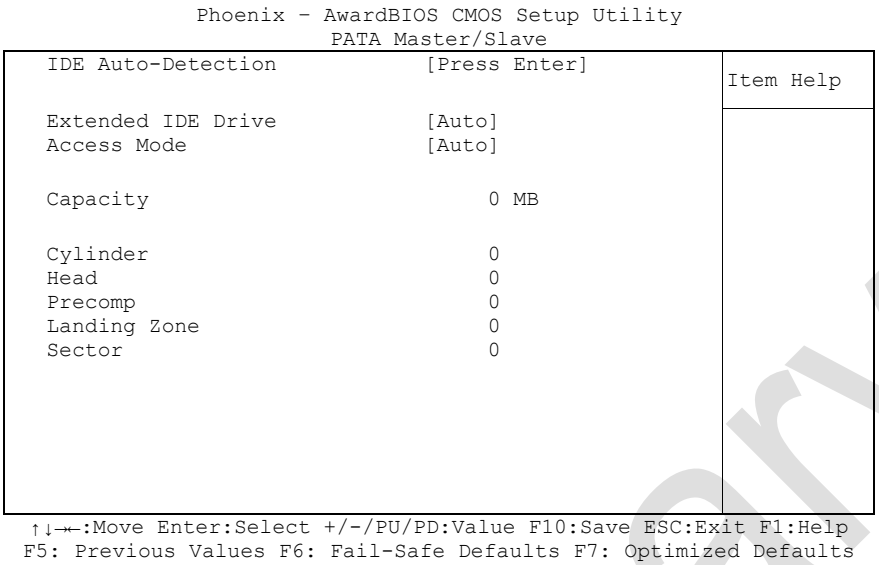
- ✓ **Total Memory**
  Options: none

4.3.1 SATA channels



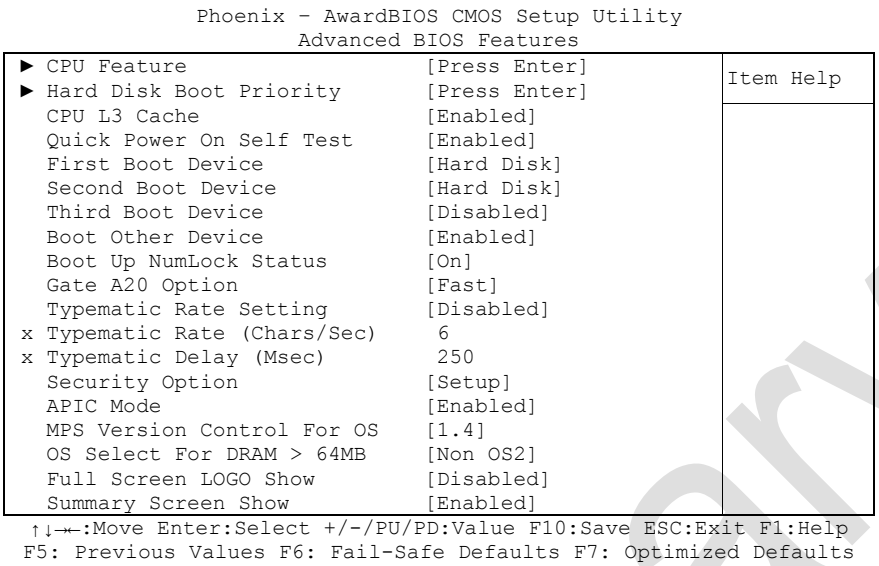
- ✓ **IDE HDD Auto-Detection**
  Options: none
- ✓ **Extended IDE Drive**
  Options: None / Auto
- ✓ **Access Mode**
  Options: Large / Auto
- ✓ **Capacity**
  Options: none
- ✓ **Cylinder**
  Options: none
- ✓ **Head**
  Options: none
- ✓ **Precomp**
  Options: none
- ✓ **Landing Zone**
  Options: none
- ✓ **Sector**
  Options: none

4.3.2 PATA channel



- ✓ **IDE HDD Auto-Detection**
  Options: none
- ✓ **Extended IDE Drive**
  Options: None / Auto
- ✓ **Access Mode**
  Options: Large / Auto
- ✓ **Capacity**
  Options: none
- ✓ **Cylinder**
  Options: none
- ✓ **Head**
  Options: none
- ✓ **Precomp**
  Options: none
- ✓ **Landing Zone**
  Options: none
- ✓ **Sector**
  Options: none

4.4 Advanced BIOS Features



- ✓ **CPU Feature**
  Sub menu: see "CPU Feature" (page 57)

- ✓ **Hard Disk Boot Priority**
  Sub menu: see "Hard Disk Boot Priority" (page 58)

- ✓ **CPU L3 Cache**
  Options: Enabled / Disabled

- ✓ **Quick Power On Self Test**
  Options: Enabled / Disabled

- ✓ **First Boot Device**
  Options: LS120 / Hard Disk / CDROM / USB Device / ZIP100 / USB-FDD / USB-ZIP / Legacy LAN / IBA GE Slot 00C8 / Disabled

- ✓ **Second Boot Device**
  Options: LS120 / Hard Disk / CDROM / USB Device / ZIP100 / USB-FDD / USB-ZIP / Legacy LAN / IBA GE Slot 00C8 / Disabled

- ✓ **Third Boot Device**
  Options: LS120 / Hard Disk / CDROM / USB Device / ZIP100 / USB-FDD / USB-ZIP / Legacy LAN / IBA GE Slot 00C8 / Disabled

- ✓ **Boot Other Device**
  Options: Enabled / Disabled

- ✓ **Boot Up NumLock Status**
  Options: Off / On

- ✓ **Gate A20 Option**
  Options: Normal / Fast

- ✓ **Typematic Rate Setting**
  Options: Enabled / Disabled

- ✓ **Typematic Rate (Chars/Sec)**
  Options: 6 / 8 / 10 / 12 / 15 / 20 / 24 / 30

- ✓ **Typematic Delay (Msec)**
  Options: 250 / 500 / 750 / 1000

- ✓ **Security Option**
  Options: Setup / System

- ✓ **APIC Mode**
  Options: Enabled / Disabled

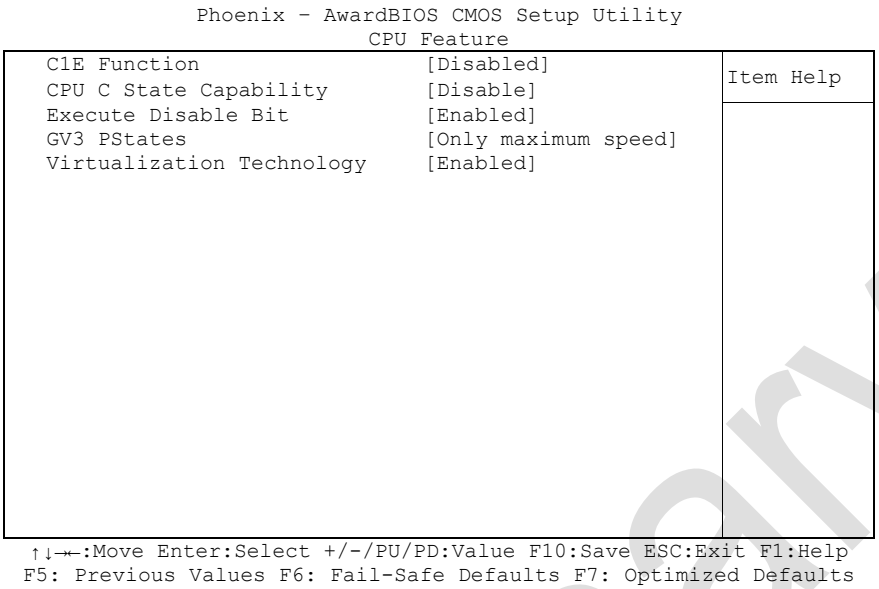
- ✓ **MPS Version Control For OS**
  Options: 1.1 / 1.4

- ✓ **OS Select For DRAM > 64MB**
  Options: Non-OS2 / OS2

- ✓ **Full Screen LOGO Show**
  Options: Enabled / Disabled

- ✓ **Summary Screen Show**
  Options: Enabled / Disabled

4.4.1 CPU Feature



- ✓ **C1E Function**
  Options: Auto / Disabled

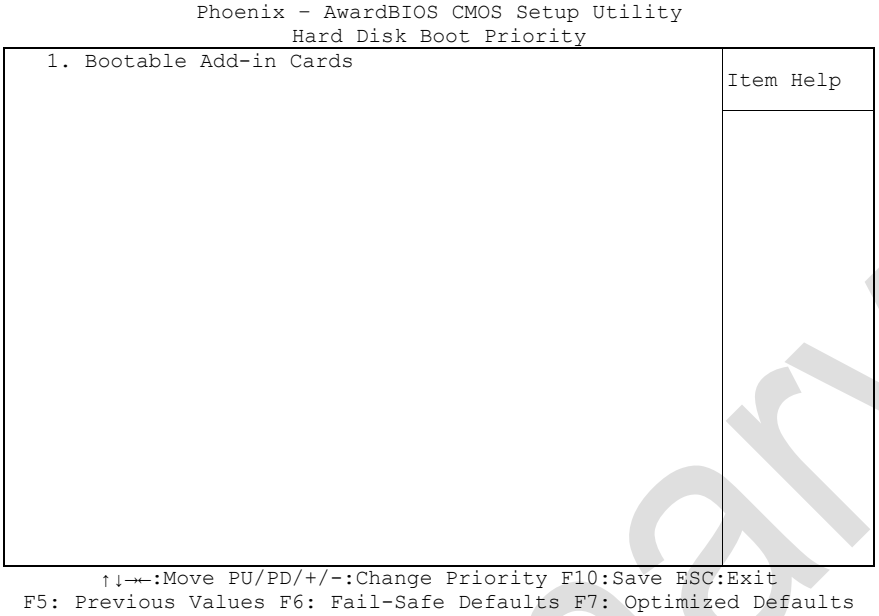
- ✓ **CPU C State Capability**
  Options: Disable / C2 / C3 / C4 / Deep C4 / C6

- ✓ **Execute Disable Bit**
  Options: Enabled / Disabled

- ✓ **GV3 PStates**
  Options: Only maximum speed / All PStates

- ✓ **Virtualization Technology**
  Options: Enabled / Disabled

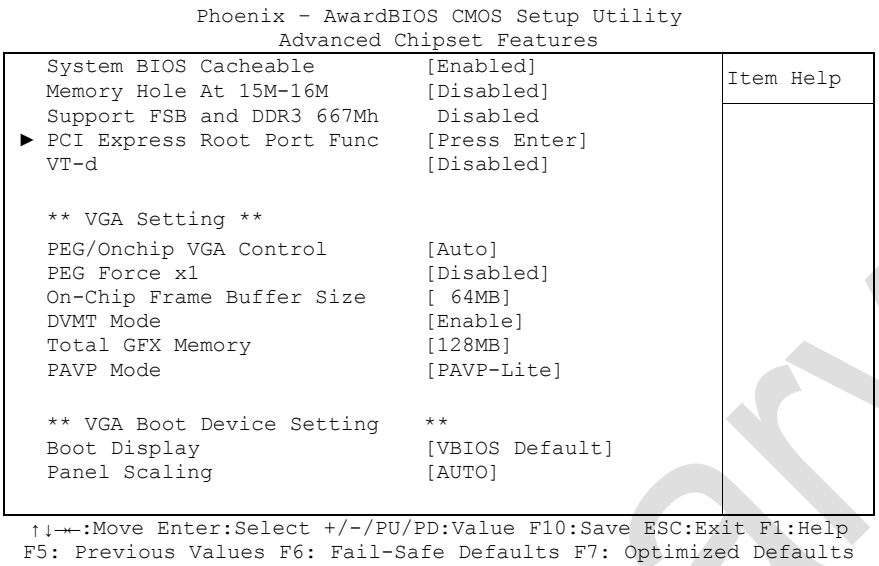
4.4.2 Hard Disk Boot Priority



✓ **[list of available devices]**
Options: this dialog allows you to set the order in which the available bootable devices shall be accessed for an attempt to boot.

✓ **Attention!**
in this sub menu the buttons <Page Up>, <Page Down>, <+> and <-> have a different function than in the rest of the setup: They serve to move the items of the list up or down.

4.5 Advanced Chipset Features



- ✓ **System BIOS Cacheable**
  Options: Enabled / Disabled

- ✓ **Memory Hole At 15M-16M**
  Options: Enabled / Disabled

- ✓ **Support FSB and DDR3 667Mhz**
  Options: none

- ✓ **PCI Express Root Port Func**
  Sub menu: see "PCI Express Root Port Function" (page 61)

- ✓ **VT-d**
  Options: Enabled / Disabled

- ✓ **PEG/Onchip VGA Control**
  Options: Onchip VGA / PEG Port / Auto

- ✓ **PEG Force X1**
  Options: Enabled / Disabled

- ✓ **On-Chip Frame Buffer Size**
  Options: 32MB / 64MB / 128MB

- ✓ **DVMT Mode**
  Options: Disable / Enable

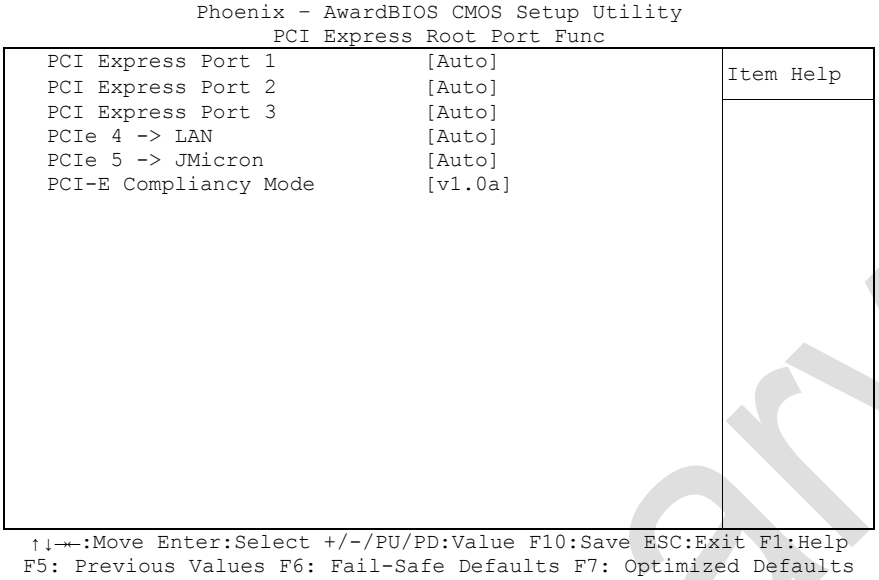
- ✓ **Total GFX Memory**
  Options: 128MB / 256MB / MAX.

- ✓ **PAVP Mode**
  Options: Disable / PAVP-Lite / PAVP-High

- ✓ **Boot Display**
  Options: VBIOS Default / CRT

✓ **Panel Scaling**
Options: Auto / Force / Off / Maintain Aspect Ratio

4.5.1 PCI Express Root Port Function



- ✓ **PCI Express Port 1**
  Options: Auto / Enabled / Disabled

- ✓ **PCI Express Port 2**
  Options: Auto / Enabled / Disabled

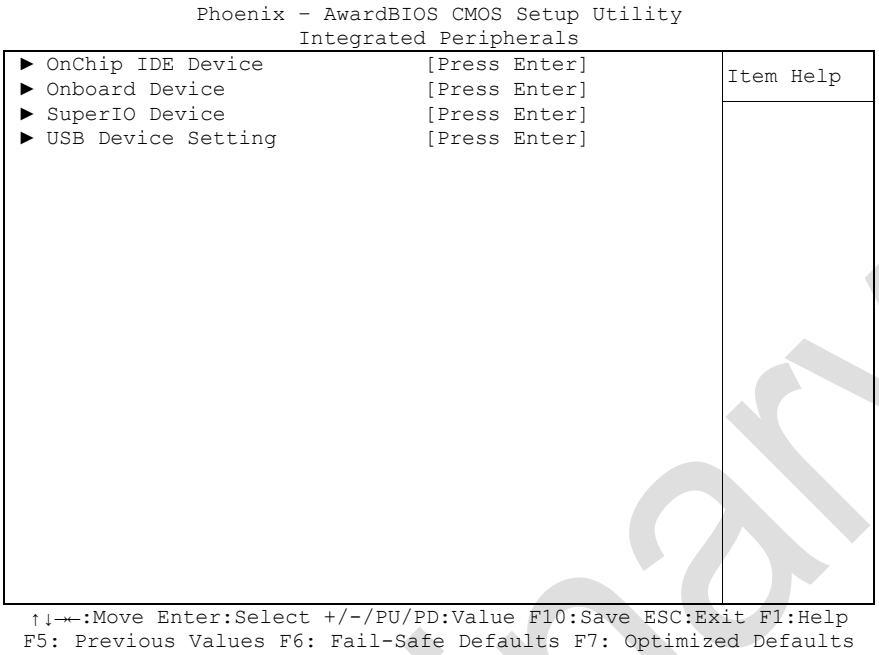
- ✓ **PCI Express Port 3**
  Options: Auto / Enabled / Disabled

- ✓ **PCIe 4 -> LAN**
  Options: Auto / Enabled / Disabled

- ✓ **PCIe 5 -> JMicron**
  Options: Auto / Enabled / Disabled

- ✓ **PCI-E Compliancy Mode**
  Options: v1.0a / v1.0

4.6 Integrated Peripherals



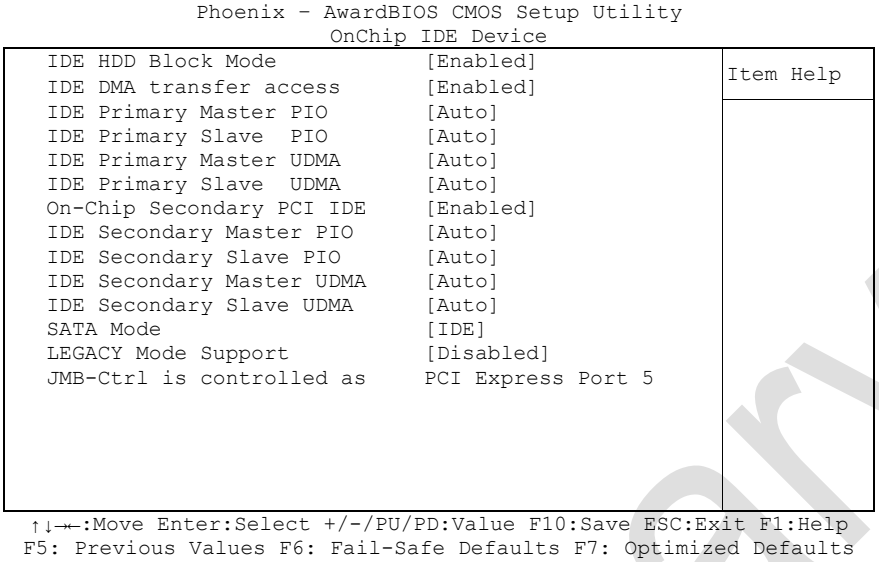
- ✓ **OnChip IDE Device**
  Sub menu: see "OnChip IDE Devices" (page 63)

- ✓ **Onboard Device**
  Sub menu: see "Onboard Devices" (page 65)

- ✓ **SuperIO Device**
  Sub menu: see "SuperIO Devices" (page 66)

- ✓ **USB Device Setting**
  Sub menu: see "USB Device Setting" (page 67)

4.6.1 OnChip IDE Devices



- ✓ **IDE HDD Block Mode**
  Options: Enabled / Disabled

- ✓ **IDE DMA transfer access**
  Options: Enabled / Disabled

- ✓ **IDE Primary Master PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

- ✓ **IDE Primary Slave PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

- ✓ **IDE Primary Master UDMA**
  Options: Disabled / Auto

- ✓ **IDE Primary Slave UDMA**
  Options: Disabled / Auto

- ✓ **On-Chip Secondary PCI IDE**
  Options: Enabled / Disabled

- ✓ **IDE Secondary Master PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

- ✓ **IDE Secondary Slave PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

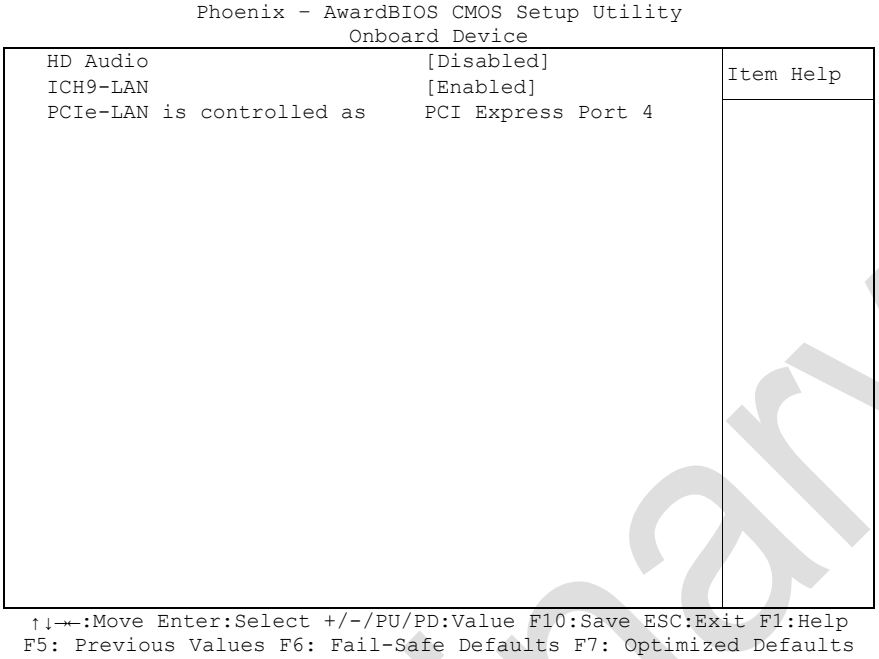
- ✓ **IDE Secondary Master UDMA**
  Options: Disabled / Auto

- ✓ **IDE Secondary Slave UDMA**
  Options: Disabled / Auto

- ✓ **SATA Mode**
  Options: IDE / RAID / AHCI

✓ **LEGACY Mode Support**
Options: Enabled / Disabled

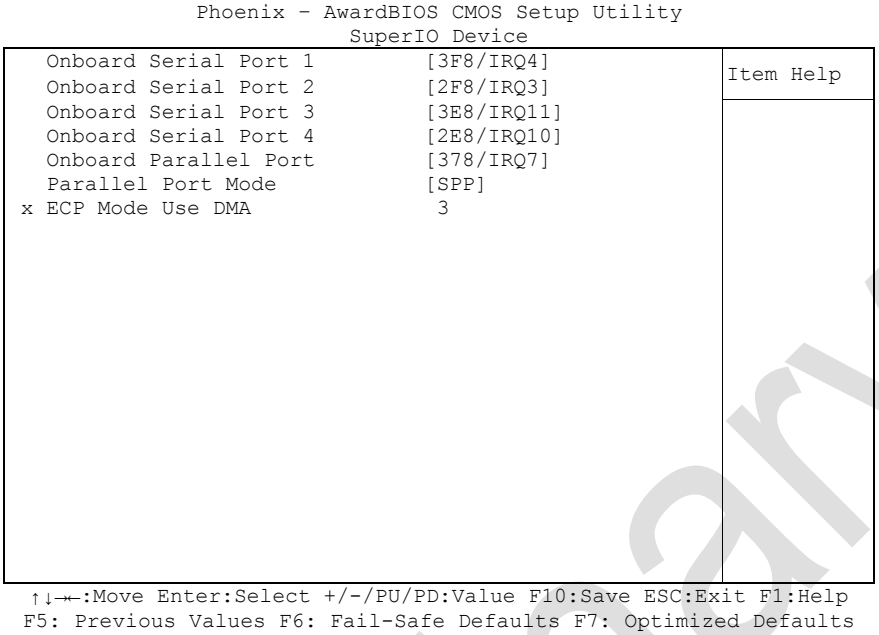
4.6.2 Onboard Devices



- ✓ **HD Audio**
  Options: Auto / Disabled

- ✓ **ICH9-LAN**
  Options: Enabled / Disabled

4.6.3 SuperIO Devices



- ✓ **Onboard Serial Port 1**
  Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3

- ✓ **Onboard Serial Port 2**
  Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3

- ✓ **Onboard Serial Port 3**
  Options: Disabled / 3F8/IRQ11 / 2F8/IRQ11 / 3E8/IRQ11 / 2E8/IRQ11

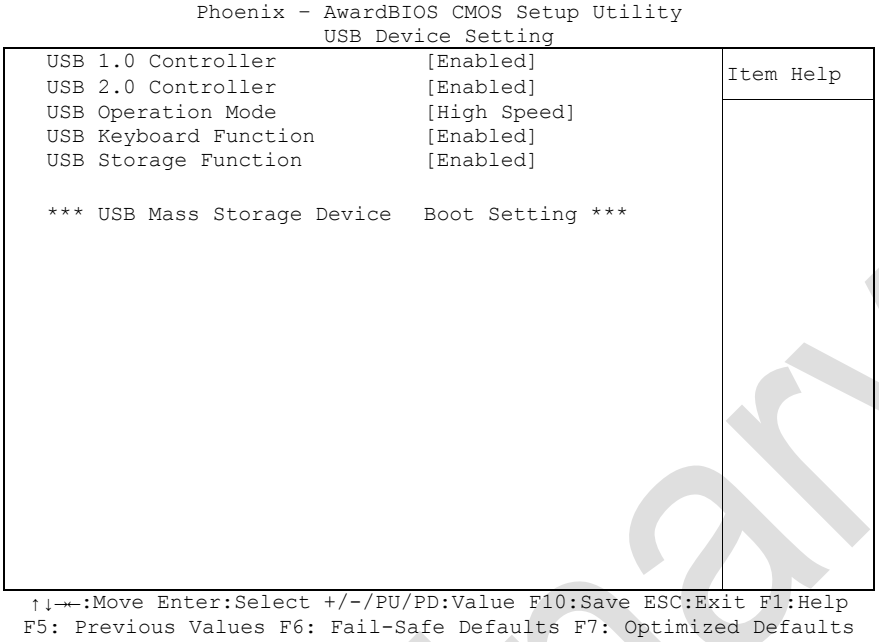
- ✓ **Onboard Serial Port 4**
  Options: Disabled / 3F8/IRQ10 / 2F8/IRQ10 / 3E8/IRQ10 / 2E8/IRQ10

- ✓ **Onboard Parallel Port**
  Options: Disabled / 378/IRQ7 / 278/IRQ5 / 3BC/IRQ7

- ✓ **Parallel Port Mode**
  Options: SPP / EPP1.9 + SPP / ECP / EPP1.9 + ECP / PRINTER / EPP1.7 + SPP / EPP1.7 + ECP

- ✓ **ECP Mode Use DMA**
  Options: 1 / 3

4.6.4 USB Device Setting



- ✓ **USB 1.0 Controller**
  Options: Enabled / Disabled

- ✓ **USB 2.0 Controller**
  Options: Enabled / Disabled

- ✓ **USB Operation Mode**
  Options: Full/Low Speed / High Speed

- ✓ **USB Keyboard Function**
  Options: Enabled / Disabled

- ✓ **USB Storage Function**
  Options: Enabled / Disabled

4.7 Power Management Setup

```
                Phoenix – AwardBIOS CMOS Setup Utility
                      Power Management Setup
 ► PCI Express PM Function       [Press Enter]    Item Help
   ACPI Function                 [Enabled]
   ACPI Suspend Type             [S1(POS)]
 x Run VGABIOS if S3 Resume       Auto
   Power Management              [User Define]
   Video Off Method              [DPMS]
   Video Off in Suspend          [Yes]
   Suspend Type                  [Stop Grant]
   Modem Use IRQ                 [3]
   Suspend Mode                  [Disabled]
   HDD Power Down                [Disabled]
   Soft-Off by PWR-BTTN          [Instant-Off]
   PWRON After PWR-Fail          [On]
   Wake-Up by PCI card           [Disabled]
   Power On by Ring              [Disabled]
 x USB KB Wake-Up From S3       Disabled
   Resume by Alarm               [Disabled]
 x  Date(of Month) Alarm          0
 x  Time(hh:mm:ss)                0 : 0 : 0

   ** Reload Global Timer        Events **
   Primary IDE 0                 [Disabled]
   Primary IDE 1                 [Disabled]
   Secondary IDE 0               [Disabled]
   Secondary IDE 1               [Disabled]
   FDD,COM,LPT Port              [Disabled]
   PCI PIRQ[A-D]#                [Disabled]
   HPET Support                  [Enabled]
   HPET Mode                     [32-bit mode]
 ► Intel DTS Feature             [Press Enter]
   ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
  F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- ✓ **PCI Express PM Function**
  Sub menu: see "PCI Express PM Function" (page 70)

- ✓ **ACPI function**
  Options: Enabled / Disabled

- ✓ **ACPI Suspend Type**
  Options: S1(POS) / S3(STR) / S1&S3

- ✓ **Run VGABIOS if S3 Resume**
  Options: Auto / Yes / No

- ✓ **Power Management**
  Options: User Define / Min Saving / Max Saving

- ✓ **Video Off Method**
  Options: Blank Screen / V/H SYNC+Blank / DPMS

- ✓ **Video Off In Suspend**
  Options: No / Yes

- ✓ **Suspend Type**
  Options: Stop Grant / PwrOn Suspend

- ✓ **MODEM Use IRQ**
  Options: NA / 3 / 4 / 5 / 7 / 9 / 10 / 11

- ✓ **Suspend Mode**
  Options: Disabled / 1 Min / 2 Min / 4 Min / 8 Min / 12 Min / 20 Min / 30 Min / 40 Min / 1 Hour

- ✓ **HDD Power Down**
  Options: Disabled / 1 Min ... 15 Min

- ✓ **Soft-Off by PWR-BTTN**
  Options: Instant-Off / Delay 4 Sec

- ✓ **PWRON After PWR-Fail**
  Options: Former Sts / On / Off

- ✓ **Wake Up by PCI Card**
  Options: Enabled / Disabled

- ✓ **Power-On by Ring**
  Options: Enabled / Disabled

- ✓ **USB KB Wake Up From S3**
  Options: Enabled / Disabled

- ✓ **Resume by Alarm**
  Options: Enabled / Disabled

- ✓ **Date(of Month) Alarm**
  Options: 1 / ... / 31

- ✓ **Time (hh:mm:ss) Alarm**
  Options: insert [hh], [mm] and [ss]

- ✓ **Primary IDE 0**
  Options: Enabled / Disabled

- ✓ **Primary IDE 1**
  Options: Enabled / Disabled

- ✓ **Secondary IDE 0**
  Options: Enabled / Disabled

- ✓ **Secondary IDE 1**
  Options: Enabled / Disabled

- ✓ **FDD,COM,LPT Port**
  Options: Enabled / Disabled

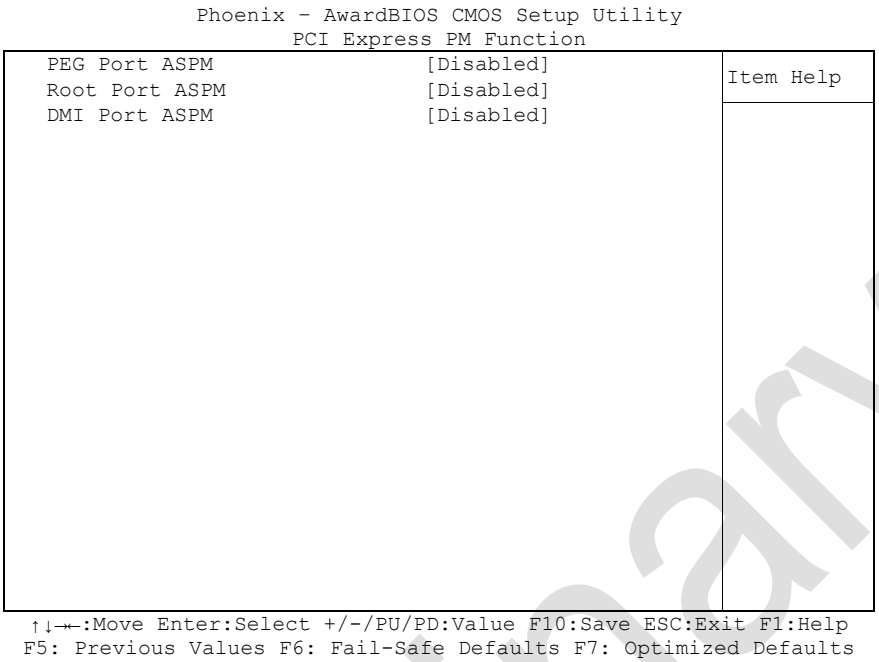
- ✓ **PCI PIRQ[A-D]#**
  Options: Enabled / Disabled

- ✓ **HPET Support**
  Options: Enabled / Disabled

- ✓ **HPET Mode**
  Options: 32-bit mode / 64-bit mode

- ✓ **Intel DTS Feature**
  Sub menu: see "Intel DTS Feature" (page 71)

4.7.1 PCI Express PM Function

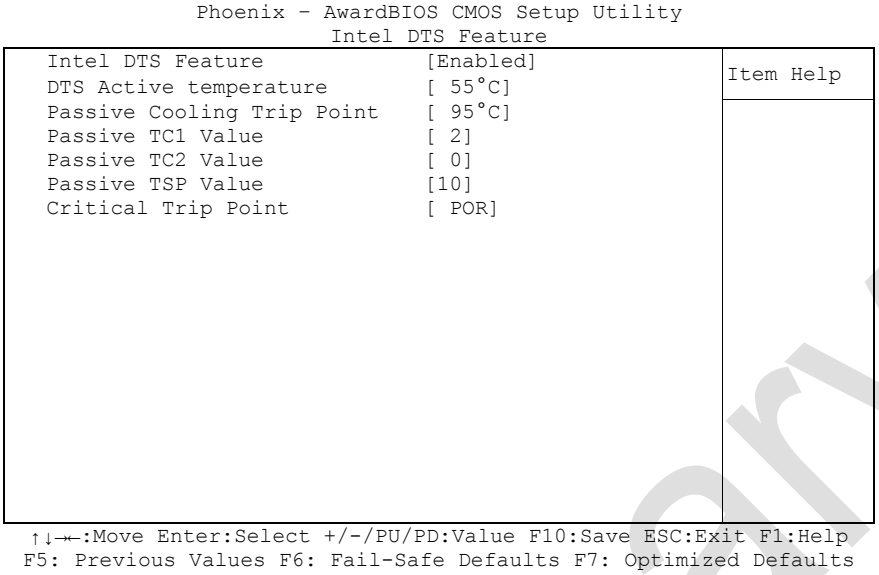


- ✓ **PEG Port ASPM**
  Options: Disabled / L0s / L1/L0s

- ✓ **Root Port ASPM**
  Options: Disabled / L0s / L1 / L1/L0s

- ✓ **DMI Port ASPM**
  Options: Enabled / Disabled

4.7.2 Intel DTS Feature



- ✓ **Intel DTS Function**
  Options: Enabled / Disabled

- ✓ **DTS Active temperature**
  Options: 15°C / 23°C / 31°C / 39°C / 47°C / 55°C / 63°C / 71°C / 79°C / 87°C / 95°C / 103°C / 111°C / 119°C

- ✓ **Passive Cooling Trip Point**
  Options: 15°C / 23°C / 31°C / 39°C / 47°C / 55°C / 63°C / 71°C / 79°C / 87°C / 95°C / 103°C / 111°C / 119°C

- ✓ **Passive TC1 Value**
  Options: 0 / 1 / ... / 14 / 15

- ✓ **Passive TC2 Value**
  Options: 0 / 1 / ... / 14 / 15

- ✓ **Passive TSP Value**
  Options: 0 / 1 / ... / 14 / 15

- ✓ **Critical Trip Point**
  Options: POR / 15°C / 23°C / 31°C / 39°C / 47°C / 55°C / 63°C / 71°C / 79°C / 87°C / 95°C / 103°C / 111°C / 119°C / 127°C

4.8 PnP/PCI Configuration

```
                Phoenix – AwardBIOS CMOS Setup Utility
                      PNP/PCI Configurations
  Init Display First            [PCI Slot]          | Item Help
  Reset Configuration Data      [Disabled]          |
                                                    |
  Resources Controlled By       [Manual]            |
► IRQ Resources                 [Press Enter]       |
                                                    |
  PCI/VGA Palette Snoop         [Disabled]          |
  INT Pin 1 Assignment          [Auto]              |
  INT Pin 2 Assignment          [Auto]              |
  INT Pin 3 Assignment          [Auto]              |
  INT Pin 4 Assignment          [Auto]              |
  INT Pin 5 Assignment          [Auto]              |
  INT Pin 6 Assignment          [Auto]              |
  INT Pin 7 Assignment          [Auto]              |
  INT Pin 8 Assignment          [Auto]              |
                                                    |
  ** PCI Express relative       items **            |
  Maximum Payload Size          [128]               |
                                                    |
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- ✓ **Init Display First**
  Options: PCI Slot / Onboard

- ✓ **Reset Configuration Data**
  Options: Enabled / Disabled

- ✓ **Resources Controlled By**
  Options: Auto(ESCD) / Manual

- ✓ **IRQ Resources**
  Sub menu: see "IRQ Resources" (page 74)

- ✓ **PCI/VGA Palette Snoop**
  Options: Enabled / Disabled

- ✓ **INT Pin 1 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- ✓ **INT Pin 2 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- ✓ **INT Pin 3 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- ✓ **INT Pin 4 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- ✓ **INT Pin 5 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

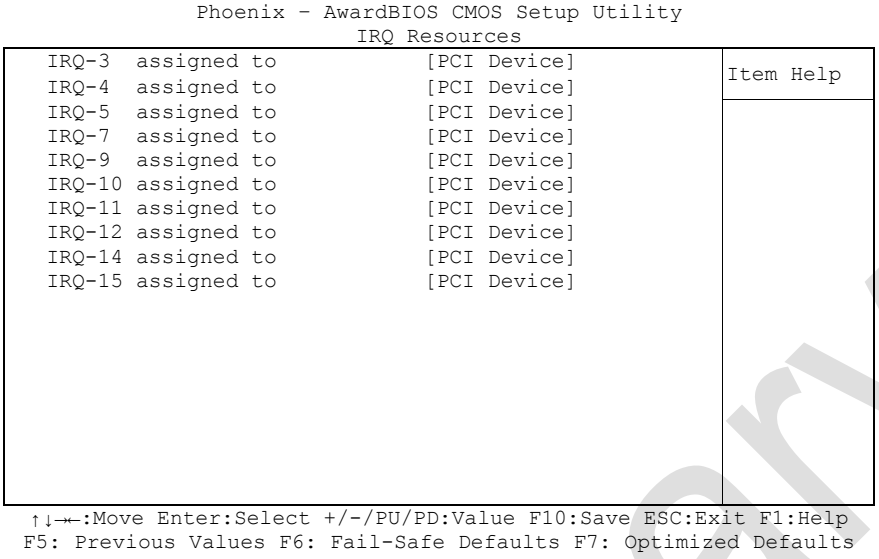
- ✓ **INT Pin 6 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- ✓ **INT Pin 7 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- ✓ **INT Pin 8 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

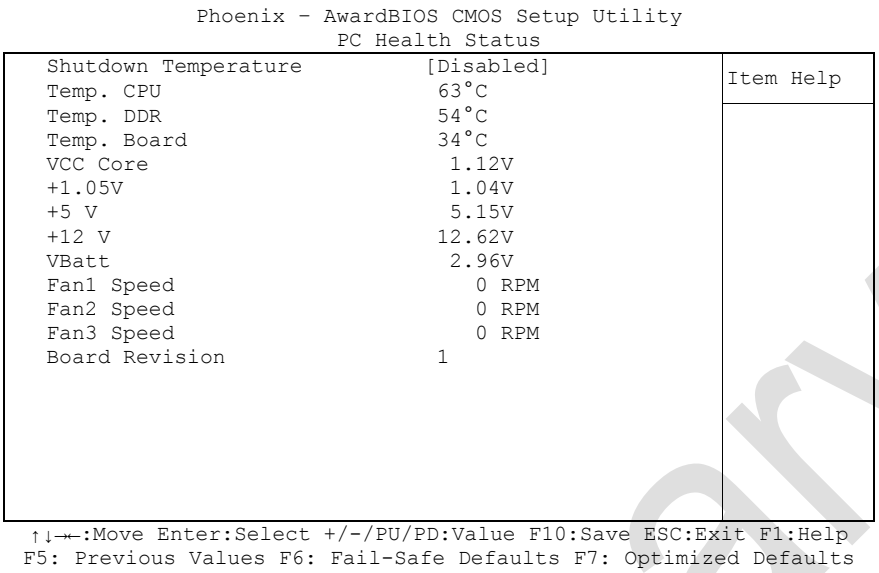
- ✓ **Maximum Payload Size**
  Options: none

4.8.1 IRQ Resources



- ✓ **IRQ-3 assigned to**
  Options: PCI Device / Reserved
- ✓ **IRQ-4 assigned to**
  Options: PCI Device / Reserved
- ✓ **IRQ-5 assigned to**
  Options: PCI Device / Reserved
- ✓ **IRQ-7 assigned to**
  Options: PCI Device / Reserved
- ✓ **IRQ-9 assigned to**
  Options: PCI Device / Reserved
- ✓ **IRQ-10 assigned to**
  Options: PCI Device / Reserved
- ✓ **IRQ-11 assigned to**
  Options: PCI Device / Reserved
- ✓ **IRQ-12 assigned to**
  Options: PCI Device / Reserved
- ✓ **IRQ-14 assigned to**
  Options: PCI Device / Reserved
- ✓ **IRQ-15 assigned to**
  Options: PCI Device / Reserved

4.9 PC Health Status



- ✓ **Temp. CPU**
  Options: none
- ✓ **Temp. DDR**
  Options: none
- ✓ **Temp. Board**
  Options: none
- ✓ **VCC Core**
  Options: none
- ✓ **+1.05 V**
  Options: none
- ✓ **+5 V**
  Options: none
- ✓ **+12 V**
  Options: none
- ✓ **VBatt**
  Options: none
- ✓ **Fan1 Speed**
  Options: none
- ✓ **Fan2 Speed**
  Options: none
- ✓ **Fan3 Speed**
  Options: none
- ✓ **Board Revision**
  Options: none

4.10 Frequency/Voltage Control

- ✓ **Spread Spectrum**
  Options: Enabled / Disabled

4.11 Load Fail-Safe Defaults

If this option is chosen, the last working setup is loaded from flash. Working means that the setup setting has already led to a successful boot process.
At the first setting of the BIOS setup, safe values are loaded which lets the board boot. This status is reached again, if the board is reprogrammed with the corresponding flash-program and the required parameters.

4.12 Load Optimized Defaults

This option applies like described under “Remarks for Setup Use” (5.1).
At first start of the BIOS, optimized values are loaded from the setup, which are supposed to make the board boot. This status is achieved again, if the board is reprogrammed using the flash program with the required parameters.

4.13 Set Password

Here you can enter a password to protect the BIOS settings against unauthorized changes. Use this option with care! Forgotten or lost passwords are a frequent problem.

4.14 Save & Exit Setup

Settings are saved and the board is restarted.

4.15 Exit Without Saving

This option leaves the setup without saving any changes.

5 BIOS update

If a BIOS update becomes necessary, the program “AWDFLASH.EXE” from Phoenix Technologies is used for this. It is important, that the program is started from a DOS environment without a virtual memory manager such as for example “EMM386.EXE”. In case such a memory manager is loaded, the program will stop with an error message.
The system must not be interrupted during the flash process, otherwise the update is stopped and the BIOS is destroyed afterwards.
The program should be started as follows:

```
awdflash [biosfilename] /sn /cc /cp
```

/sn	Do not save the current BIOS
/cc	Clear the CMOS
/cp	Clear the PnP information

The erasure of CMOS and PnP is strongly recommended. This ensures, that the new BIOS works correctly and that all chipset registers, which were saved in the setup, are reinitialized through the BIOS. DMI should only be erased (option /cd) if the BIOS supplier advises to do so.
A complete description of all valid parameters is shown with the parameter “/?”.
In order to make the updating process run automatically, the parameter “/py” must be added. This parameter bypasses all security checks during programming.

CAUTION

Updating the BIOS in an improper way can render the board unusable. Therefore, you should only update the BIOS if you really need the changes/corrections which come with the new BIOS version.

CAUTION

Before you proceed to update the BIOS you need to make absolutely sure that you have the right BIOS file which was issued for the exact board and exact board revision that you wish to update. If you try to update the BIOS using the wrong file the board will not start up again.

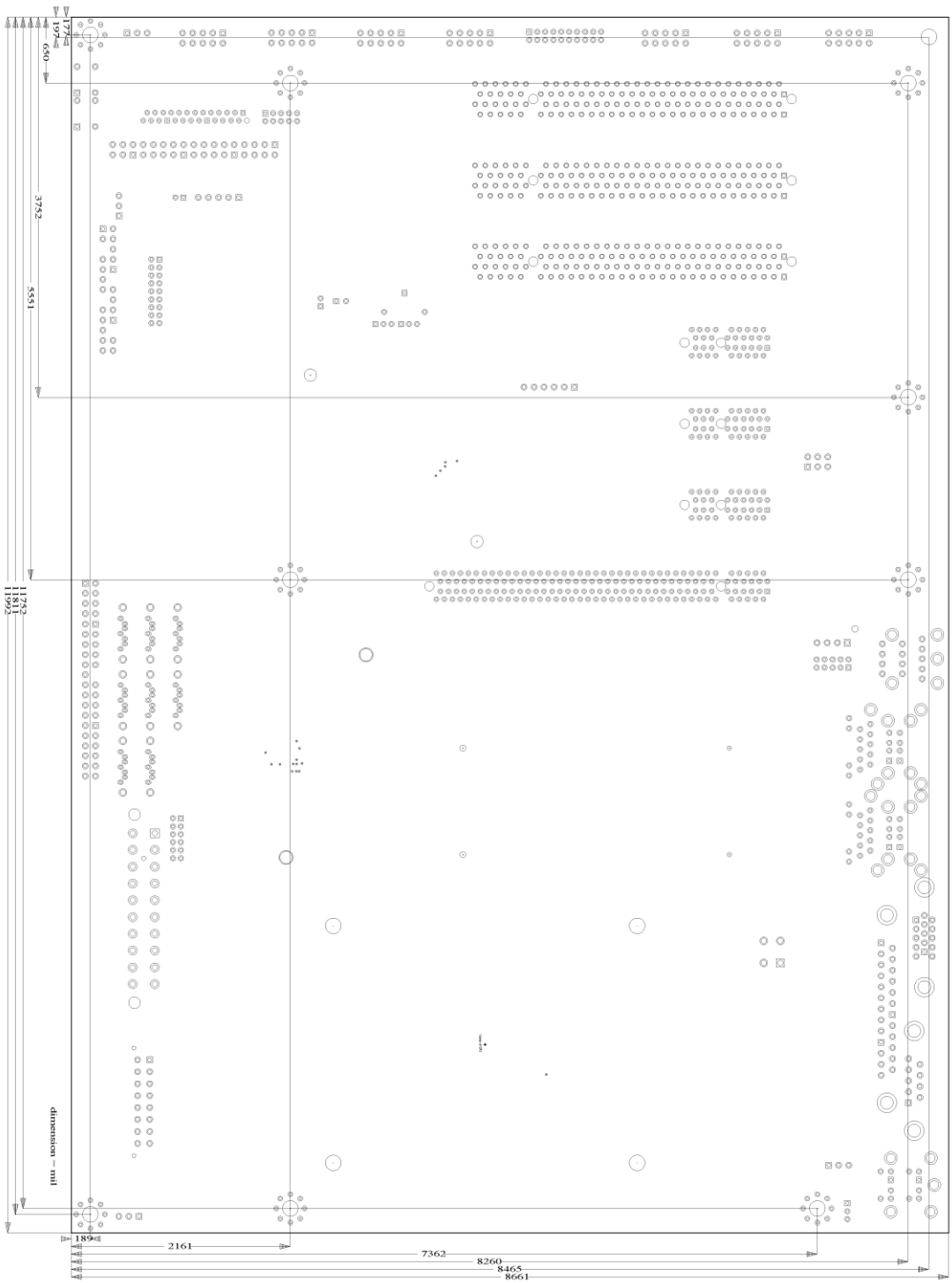
6 Mechanical Drawings

6.1 PCB: Mounting Holes

A true dimensioned drawing can be found in the PC/104 specification.

NOTE

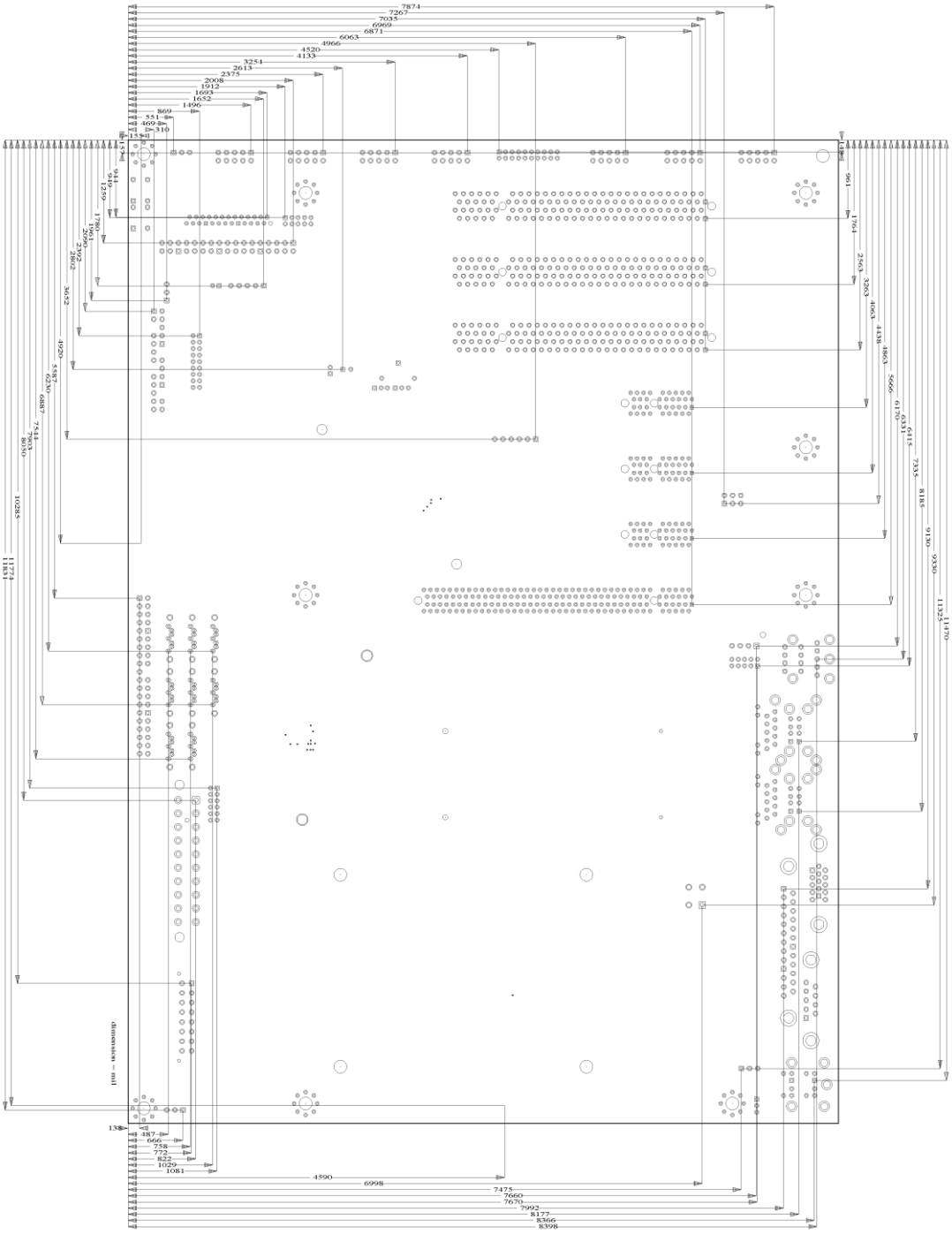
All dimensions are in mil (1 mil = 0,0254 mm)



6.2 PCB: Pin 1 Dimensions

NOTE

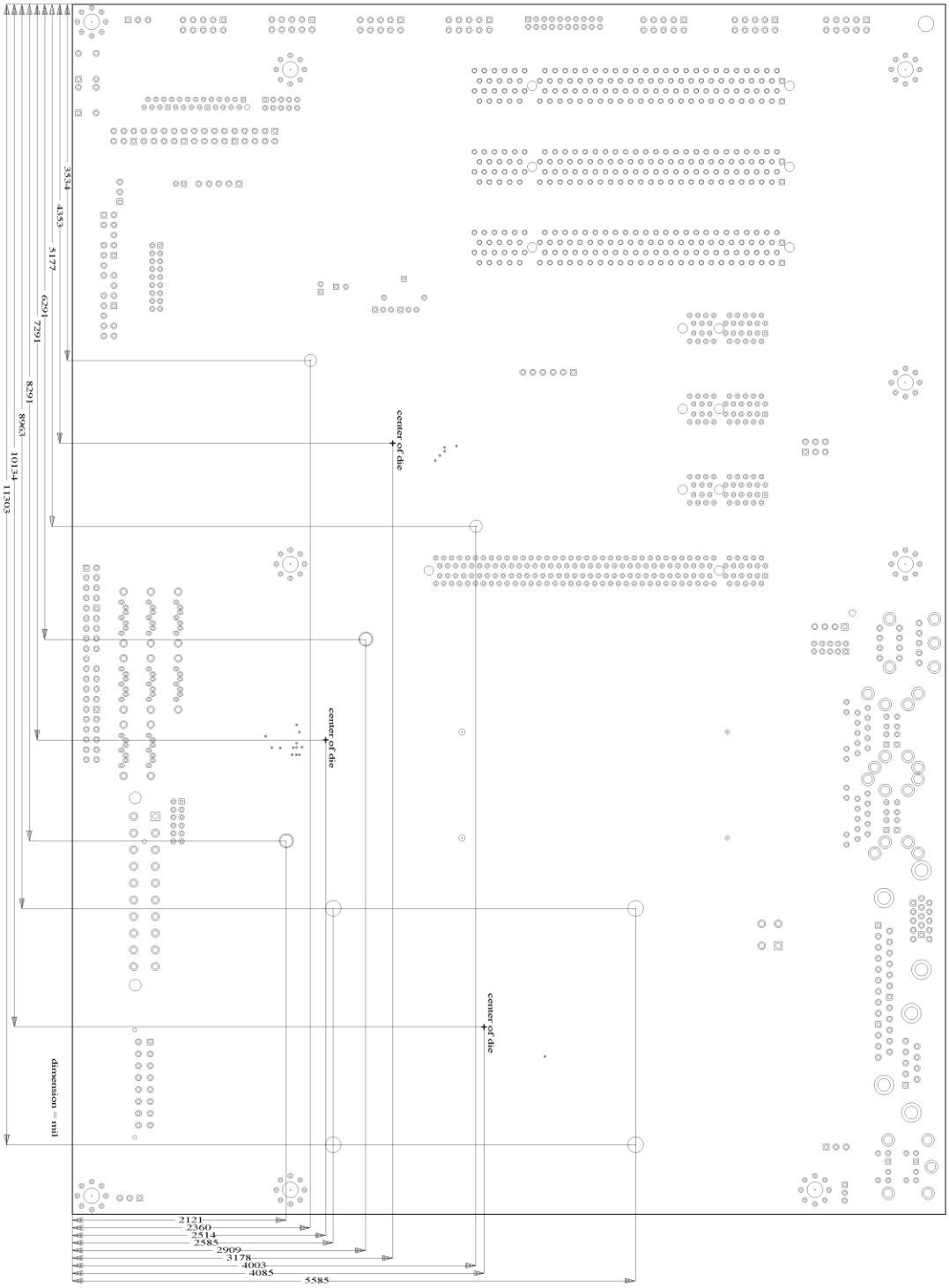
All dimensions are in mil (1 mil = 0,0254 mm)



6.3 PCB: Die Center

NOTE

All dimensions are in mil (1 mil = 0,0254 mm)



7 Technical Data

7.1 Electrical Data

Power Supply:

Board:	ATX, including 2x2pin 12V connector
RTC:	>= 3 Volt

Electric Power Consumption:

Board:	typically 10VA (CPU and expansion cards excluded)
RTC:	<= 10µA

7.2 Environmental Conditions

Temperature Range:

Operating:	0°C to +60°C (extended temperature on request)
Storage:	-25°C up to +85°C
Shipping:	-25°C up to +85°C, for packaged boards

Temperature Changes:

Operating:	0.5°C per minute, 7.5°C per 30 minutes
Storage:	1.0°C per minute
Shipping:	1.0°C per minute, for packaged boards

Relative Humidity:

Operating:	5% up to 85% (non condensing)
Storage:	5% up to 95% (non condensing)
Shipping:	5% up to 100% (non condensing), for packaged boards

Shock:

Operating:	150m/s^2, 6ms
Storage:	400m/s^2, 6ms
Shipping:	400m/s^2, 6ms, for packaged boards

Vibration:

Operating:	10 up to 58Hz, 0.075mm amplitude
	58 up to 500Hz, 10m/s^2
Storage:	5 up to 9Hz, 3.5mm amplitude
	9 up to 500Hz, 10m/s^2
Shipping:	5 up to 9Hz, 3.5mm amplitude
	9 up to 500Hz, 10m/s^2, for packaged boards

CAUTION

Shock and vibration figures pertain to the motherboard alone and do not include additional components such as heat sinks, memory modules, cables etc.

7.3 Thermal Specifications

The board is specified to operate in an environmental temperature range from 0°C to +60°C (extended temperature on request). Maximum die temperature is 100°C. To keep the processor under this threshold an appropriate cooling solution needs to be applied. This solution has to take typical and maximum power consumption into account. The maximum power consumption may be twice as high and should be used as a basis for the cooling concept. Additional controllers may also affect the cooling concept. The power consumption of such components may be comparable to the consumption of the processor.
The board design includes thermal solution mounting points that will provide the best possible thermal interface between die and solution. Since we take thermal solutions seriously we have several advanced, aggressive cooling solutions in our product portfolio. Please contact your sales representative to order or discuss your thermal solution needs.

CAUTION

The end customer has the responsibility to ensure that the die temperature of the processor does not exceed 100°C. Permanent overheating may destroy the board!
In case the temperature exceeds 100°C the environmental temperature must be reduced. Under certain circumstances sufficient air circulation must be provided.

8 Support and Service

Beckhoff and their partners around the world offer comprehensive support and service, making available fast and competent assistance with all questions related to Beckhoff products and system solutions.

8.1 Beckhoff's Branch Offices and Representatives

Please contact your Beckhoff branch office or representative for local support and service on Beckhoff products.
The addresses of Beckhoff's branch offices and representatives around the world can be found on her internet pages: http://www.beckhoff.com
You will also find further documentation for Beckhoff components there.

8.2 Beckhoff Headquarters

Beckhoff Automation GmbH
Eiserstr. 5
33415 Verl
Germany

phone:	+49(0)5246/963-0
fax:	+49(0)5246/963-198
e-mail:	info@beckhoff.com
web:	www.beckhoff.com

8.2.1 Beckhoff Support

Support offers you comprehensive technical assistance, helping you not only with the application of individual Beckhoff products, but also with other, wide-ranging services:

- support
- design, programming and commissioning of complex automation systems
- and extensive training programs for Beckhoff system components

hotline:	+49(0)5246/963-157
fax:	+49(0)5246/963-9157
e-mail:	support@beckhoff.com

8.2.2 Beckhoff Service

The Beckhoff Service Center supports you in all matters of after-sales service:

- on-site service
- repair service
- spare parts service
- hotline service

hotline:	+49(0)5246/963-460
fax:	+49(0)5246/963-479
e-mail:	service@beckhoff.com

I Annex: Post-Codes

Code	Description
01h	The Xgroup-program code is written in the random access memory from address 1000:0 onwards.
03h	Initialise Variable/Routine "Superio_Early_Init".
05h	1. Cancel display 2. Cancel CMOS error flag
07h	1. Cancel 8042 (keyboard controller) Interface Register 2. Initialising and self testing of 8042 (keyboard controller)
08h	1. Test of special keyboard controllers (Winbond 977 super I/O Chip-series). 2. Enabling of the keyboard-interface register
0Ah	1. Disabling of the PS/2 mouse interface (optional). 2. Auto-detection of the connectors for Keyboard and mouse, optional: swap of PS/2 mouse ports and PS/2 interfaces.
0Eh	Test of the F000h-memory segment (Read/Write ability). In case of an error a signal will come out of the loud speakers.
10h	Auto-detection of the flash-rom-type and loading of the suitable Read/Write program into the run time memory segment F000 (it is required for ESCD-data & the DMI-pool-support).
12h	Interface-test of the CMOS RAM-logic (walking 1's"-algorithm). Setting of the power status of the real-time-clock (RTC), afterwards test of register overflow.
14h	Initialising of the chip-set with default values. They can be modified through a software (MODBIN) by the OEM-customer.
16h	Initialise Variable/Routine "Early_Init_Onboard_Generator".
18h	CPU auto-detection (manufacturer, SMI type (Cyrix or Intel), CPU-class (586 or 686).
1Bh	Initialising if the interrupt pointer table. If nothing else is pretended, the hardware interrupts will point on "SPURIOUS_INT_HDLR and the software interrupts will point on SPURIOUS_soft_HDLR.
1Dh	Initialise Variable/Routine EARLY_PM_INIT.
1Fh	Load the keyboard table (Notebooks)
21h	Initialising of the hardware power management (HPM) (Notebooks)
23h	1. Test the validity of the RTC-values (Example: "5Ah" is an invalid value for an RTC-minute). 2. Load the CMOS-values into the BIOS Stack. Default-values are loaded if CMOS-checksum errors occur. 3. Preparing of the BIOS 'resource map' for the PCI & plug and play configuration. If ESCD is valid, take into consideration the ESCD's legacy information. 4. Initialise the onboard clock generator. Clock circuit at non-used PCI- and DIMM slots. 5. First initialising of PCI-devices: assign PCI-bus numbers - alot memory- & I/O resources - search for functional VGA-controllers and VGA-BIOS and copy the latter into memory segment C000:0 (Video ROM Shadow).
27h	Initialise cache memory for INT 09
29h	1. Program the CPU (internal MTRR at P6 and PII) for the first memory address range (0-640K). 2. Initialising of the APIC at CPUs of the Pentium-class. 3. Program the chip-set according to the settings of the CMOS-set-up (Example: Onboard IDE-controller). 4. Measuring of the CPU clock speed. 5. Initialise the video BIOS.
2Dh	1. Initialise the "Multi-Language"-function of the BIOS 2. Soft copy, e.g. Award-Logo, CPU-type and CPU clock speed…
33h	Keyboard-reset (except super I/O chips of the Winbond 977 series)
3Ch	Test the 8254 (timer device)
3Eh	Test the interrupt Mask bits of IRQ-channel 1 of the interrupt controller 8259.
40h	Test the interrupt Mask bits of IRQ-channel 2 of the interrupt controller 8259
43h	Testing the function of the interrupt controller (8259).
47h	Initialise EISA slot (if existent).

Code	Description
49h	1. Determination of the entire memory size by revising the last 32-Bit double word of each 64k memory segment. 2. Program “write allocation” at AMD K5-CPUs.
4Eh	1. Program MTRR at M1 CPUs 2. Initialise level 2-cache at CPUs of the class P6 and set the “cacheable range” of the random access memory. 3. Initialise APIC at CPUs of the class P6. 4. Only for multiprocessor systems (MP platform): Setting of the “cacheable range” on the respective smallest value (for the case of non-identical values).
50h	Initialise USB interface
52h	Testing of the entire random access memory and deleting of the extended memory (put on “0”)
55h	Only for multi processor systems (MP platform): Indicate the number of CPUs.
57h	1. Indicate the plug and play logo 2. First ISA plug and play initialising – CSN-assignment for each identified ISA plug and play device.
59h	Initialise TrendMicro anti virus program code.
5Bh	(Optional:) Indication of the possibility to start AWDFLASH.EXE (Flash ROM programming) from the hard disk.
5Dh	1. Initialise Variable/Routine Init_Onboard_Super_IO. 2. Initialise Variable/Routine Init_Onbaord_AUDIO.
60h	Release for starting the CMOS set-up (this means that before this step of POST, users are not able to access the BIOS set-up).
65h	Initialising of the PS/2 mouse.
67h	Information concerning the size of random access memory for function call (INT 15h with AX-Reg. = E820h).
69h	Enable level 2 cache
6Bh	Programming of the chip set register according to the BIOS set-up and auto-detection table.
6Dh	1. Assignment of resources for all ISA plug and play devices. 2. Assignment of the port address for onboard COM-ports (only if an automatic junction has been defined in the setup).
6Fh	1. Initialising of the floppy controller 2. Programming of all relevant registers and variables (floppy and floppy controller).
73h	Optional feature: Call of AWDFLASH.EXE if: - the AWDFLASH program was found on a disk in the floppy drive. - the shortcut ALT+F2 was pressed.
75h	Detection and installation of the IDE drives: HDD, LS120, ZIP, CDROM…
77h	Detection of parallel and serial ports.
7Ah	Co-processor is detected and enabled.
7Fh	1. Switch over to the text mode, the logo output is supported. - Indication of possibly emerged errors. Waiting for keyboard entry. - No errors emerged, respective F1 key was pressed (continue): Deleting of the EPA- or own logo.
82h	1. Call the pointer to the “chip set power management”. 2. Load the text font of the EPA-logo (not if a complete picture is displayed) 3. If a password is set, it is asked here.
83h	Saving of the data in the stack, back to CMOS.
84h	Initialising of ISA plug and play boot drives (also Boot-ROMs)
85h	1. Final initialising of the USB-host. 2. At network PCs (Boot-ROM): Construction of a SYSID structure table 3. Backspace the scope presentation into the text mode 4. Initialise the ACPI table (top of memory). 5. Initialise and link ROMs on ISA cards 6. Assignment of PCI-IRQs 7. Initialising of the advanced power management (APM) 8. Set back the IRQ-register.

Code	Description
93h	Reading in of the hard disk boot sector for the inspection through the internal anti virus program (trend anti virus code)
94h	1. Enabling of level 2 cache 2. Setting of the clock speed during the boot process 3. Final initialising of the chip set. 4. Final initialising of the power management. 5. Erase the onscreen and display the overview table (rectangular box). 6. Program “write allocation” at K6 CPUs (AMD) 7. Program “write combining” at P6 CPUs (INTEL)
95h	1. Program the changeover of summer-and winter-time 2. Update settings of keyboard-LED and keyboard repeat rates
96h	1. Multi processor system: generate MP-table 2. Generate and update ESCD-table 3. Correct century settings in the CMOS (20xx or 19xx) 4. Synchronise the DOS-system timer with CMOS-time 5. Generate an MSIRQ-Routing table..
C0h	Chip set initialising: - Cut off shadow RAM - Cut off L2 cache (apron 7 or older) - Initialise chip set register
C1h	Memory detection: Auto detection of DRAM size, type and error correction (ECC or none) Auto detection of L2 cache size (apron 7 or older)
C3h	Unpacking of the packed BIOS program codes into the random access memory.
C5h	Copying of the BIOS program code into the shadow RAM (segments E000 & F000) via chipset hook.
CFh	Testing of the CMOS read/write functionality
FFh	Boot trial over boot-loader-routine (software-interrupt INT 19h)

II Annex: Resources

IO Range

The used resources depend on setup settings.
The given values are ranges, which are fixed by AT compatibility. Other IO ranges are used, which are dynamically adjusted by Plug & Play BIOS while booting.

Address	Function
0-FF	Reserved IO area of the board
170-17F	
1F0-1F7	IDE1
278-27F	
2E8-2EF	COM4
2F8-2FF	COM2
370-377	
378-37F	LPT1
3BC-3BF	
3E8-3EF	COM3
3F0-3F7	FDC1
3F8-3FF	COM1

Memory Range

The used resources depend on setup settings.
If the entire range is clogged through option ROMs, these functions do not work anymore.

Address	Function
A0000-BFFFF	VGA RAM
C0000-CFFFF	VGA BIOS
D0000-DFFFF	AHCI BIOS / RAID / PXE (if available)
E0000-EFFFF	System BIOS while booting
F0000-FFFFF	System BIOS

Interrupt

The used resources depend on setup settings.
The listed interrupts and their use are given through AT compatibility.
If interrupts must exclusively be available on the ISA side, they have to be reserved through the BIOS setup.
The exclusivity is not given and not possible on the PCI side.

Address	Function
IRQ0	Timer
IRQ1	PS/2 Keyboard
IRQ2 (9)	COM3
IRQ3	COM1
IRQ4	COM2
IRQ5	COM4
IRQ6	FDC
IRQ7	LPT1
IRQ8	RTC
IRQ9	
IRQ10	
IRQ11	
IRQ12	PS/2 Mouse

Address	Function
IRQ13	FPU
IRQ14	IDE Primary
IRQ15	

PCI Devices

All listed PCI devices exist on the board. Some PCI devices or functions of devices may be disabled in the BIOS setup. Once a device is disabled other devices may get PCI bus numbers different from the ones listed in the table.

AD	INTA	REQ	Bus	Dev.	Fct.	Controller / Slot
	-	-	0	0	0	Host Bridge ID2A40h
	A	-	0	2	0	VGA Graphics ID2A42h
	A	-	0	25	0	LAN ICH9 ID10E5h
	A	-	0	26	0	USB UHCI Controller #4 ID2937h
	B	-	0	26	1	USB UHCI Controller #5 ID2938h
	D	-	0	26	2	USB UHCI Controller #6 ID2939h
	C	-	0	26	7	USB 2.0 EHCI Controller #2 ID293Ch
	A	-	0	27	0	HDA Controller ID293Eh
	A	-	0	28	0	PCI Express Port 1 ICH9 ID2940h
	B	-	0	28	1	[PCI Express Port 2 ICH9 ID2942h]
	C	-	0	28	2	[PCI Express Port 3 ICH9 ID2944h]
	D	-	0	28	3	PCI Express Port 4 ICH9 ID2946h
	A	-	0	28	4	PCI Express Port 5 ICH9 ID2948h
	A	-	0	29	0	USB UHCI Controller #1 ID2934h
	B	-	0	29	1	USB UHCI Controller #2 ID2935h
	C	-	0	29	2	USB UHCI Controller #3 ID2936h
	A	-	0	29	7	USB 2.0 EHCI Controller #1 ID293Ah
	-	-	0	30	0	DMI-to-PCI Bridge ID244Eh
	-	-	0	31	0	LPC Interface ID2916h
	B	-	0	31	2	SATA Interface #1 ID2920h
	B	-	0	31	3	SMBus Interface ID2930h
	B	-	0	31	5	SATA Interface #2 ID2926h
	A	-	m	0	0	LAN 82547L ID10D3h
	A	-	n	0	0	ATA JMB363 ID2363h
18	A	0	o			PCI Slot 1
19	B	1	o			PCI Slot 2
20	C	2	o			PCI Slot 3

SMB Devices

Address	Function
10-11	Standard slave address
60-61	Reserved by BIOS
88-89	BIOS defined slave address
A0-A1	DIMM 1
A2-A3	DIMM 2
A4-AF	Reserved by BIOS
D2-D3	ICS9LPRS501