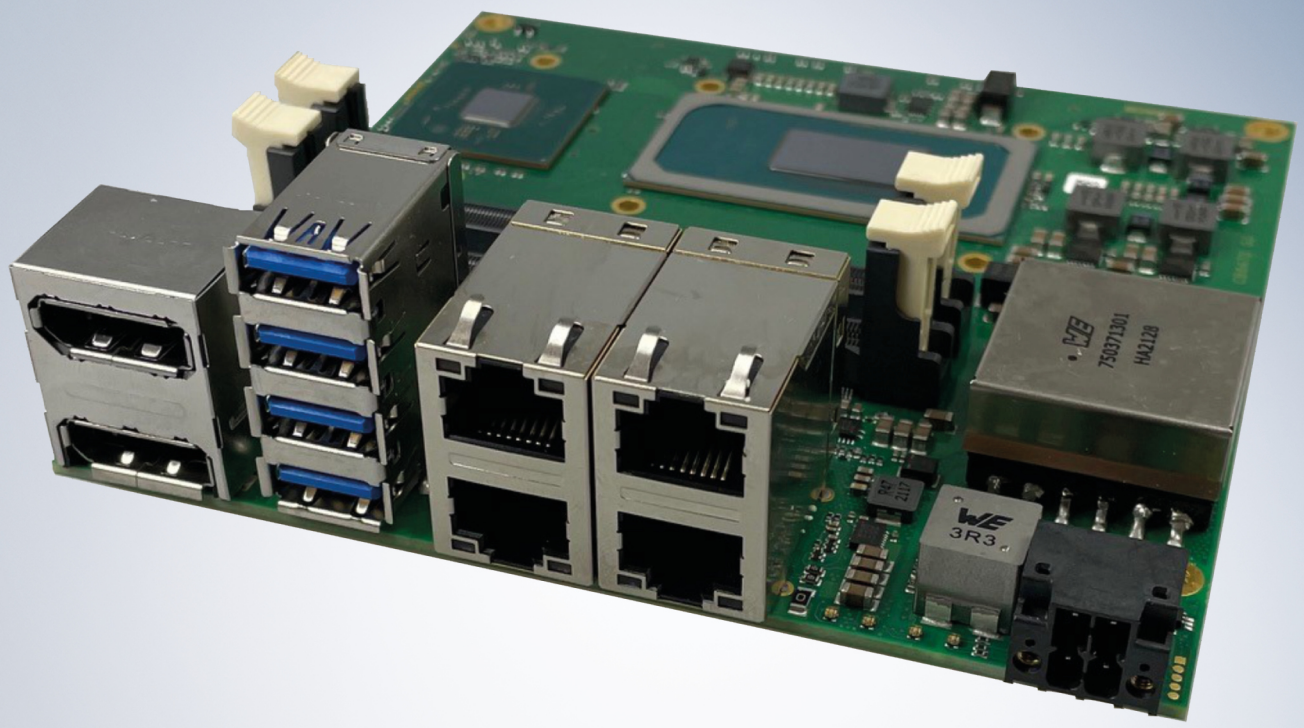
BECKHOFF New Automation Technology

Manual for | EN

CB6472

Computerboard



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1 Documentation issue status

Version	Modifications
0.1	Preliminary version, mechanical only
0.2	Preliminary version, BIOS 0.15 added
0.3	BIOS version 0.28 added
0.4	Support and service page updated
1.0	Release version with BIOS version 0.56

2 Notes on the documentation

This description is intended exclusively for trained specialists in control and automation technology who are familiar with the applicable national standards.
For installation and commissioning of the components, it is absolutely necessary to comply with the documentation and the following notes and explanations.
It is the duty of the responsible staff to use the documentation published at the respective time of each installation and commissioning.

The responsible staff must ensure that the application or use of the products described satisfies all safety requirements, including all the relevant laws, regulations, guidelines, and standards.

Origin of the document

This documentation was originally written in German. All other languages are derived from the German original.

Disclaimer

The documentation has been prepared with care. The products described are, however, constantly under development.
We reserve the right to revise and change the documentation at any time and without notice.
No claims to modify products that have already been supplied may be made on the basis of the data, diagrams, and descriptions in this documentation.

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EP1590927, EP1789857, EP1456722, EP2137893, DE102015105702
and similar applications and registrations in several other countries.

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3 Safety instructions

Safety regulations

Please observe the following safety instructions and explanations!
Product-specific safety instructions can be found on following pages or in the mounting, wiring, commissioning areas, etc.

Exclusion of liability

All of the components are supplied in specific hardware and software configurations depending on the application requirements. Modifications to hardware or software configurations other than those described in the documentation are not permitted, and nullify the liability of Beckhoff Automation GmbH & Co. KG.

Personnel qualification

This description is only intended for trained specialists in control, automation, and drive technology who are familiar with the applicable national standards.

Description of symbols

In this documentation the following symbols are used with an accompanying safety instruction or note. The safety instructions must be read carefully and followed without fail!

⚠ DANGER

Serious risk of injury!

Failure to follow the safety instructions associated with this symbol directly endangers human life and health!

⚠ WARNING

Risk of injury!

Failure to follow the safety instructions associated with this symbol endangers human life and health!

⚠ CAUTION

Personal injuries!

Failure to follow the safety instructions associated with this symbol can lead to physical injuries!

NOTICE

Damage to the environment or devices

Failure to follow the instructions associated with this symbol can lead to damage to the environment or equipment.

Tip or pointer

This symbol indicates information that contributes to better understanding.

This symbol indicates important information regarding UL approval.

Intended use

The CB6472 Computer Board was designed and developed exclusively for configuration in automation processes. To that end the board is equipped with external interfaces in order to acquire or output digital or analog signals or forward them to higher-level components.

Any other use is regarded as inappropriate.

The specified limits for electrical and technical data must be adhered to.

4 Notes on information security

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5 Overview

5.1 Properties

The CB6472 is a high-performance compact board, based on Intel®'s Tigerlake-H processor. The chipset is a Q580. State-of-the-art DDR4 technology enables a memory extension up to 64 GB using SO-DIMM260.

Two DisplayPort connectors, 4 Gigabit-LAN connectors and 4 USB 3.2 ports are available as standard interfaces on the front panel. *The two DisplayPorts++ enable the connection of an HDMI adapter for an HDMI signal. The connection of an HDMI display with adapter is possible.*

Internally, the CB6472 has two M.2 (M) sockets (2280), one of which has multiplexers for PCIe or SATA signals and a BeaCon140 connector. Depending on the chipset in use, various signals are fed out via the internal connectors. These signals are listed in the respective chapter.

Power is supplied via a 4-pin isolated connector on the front panel.

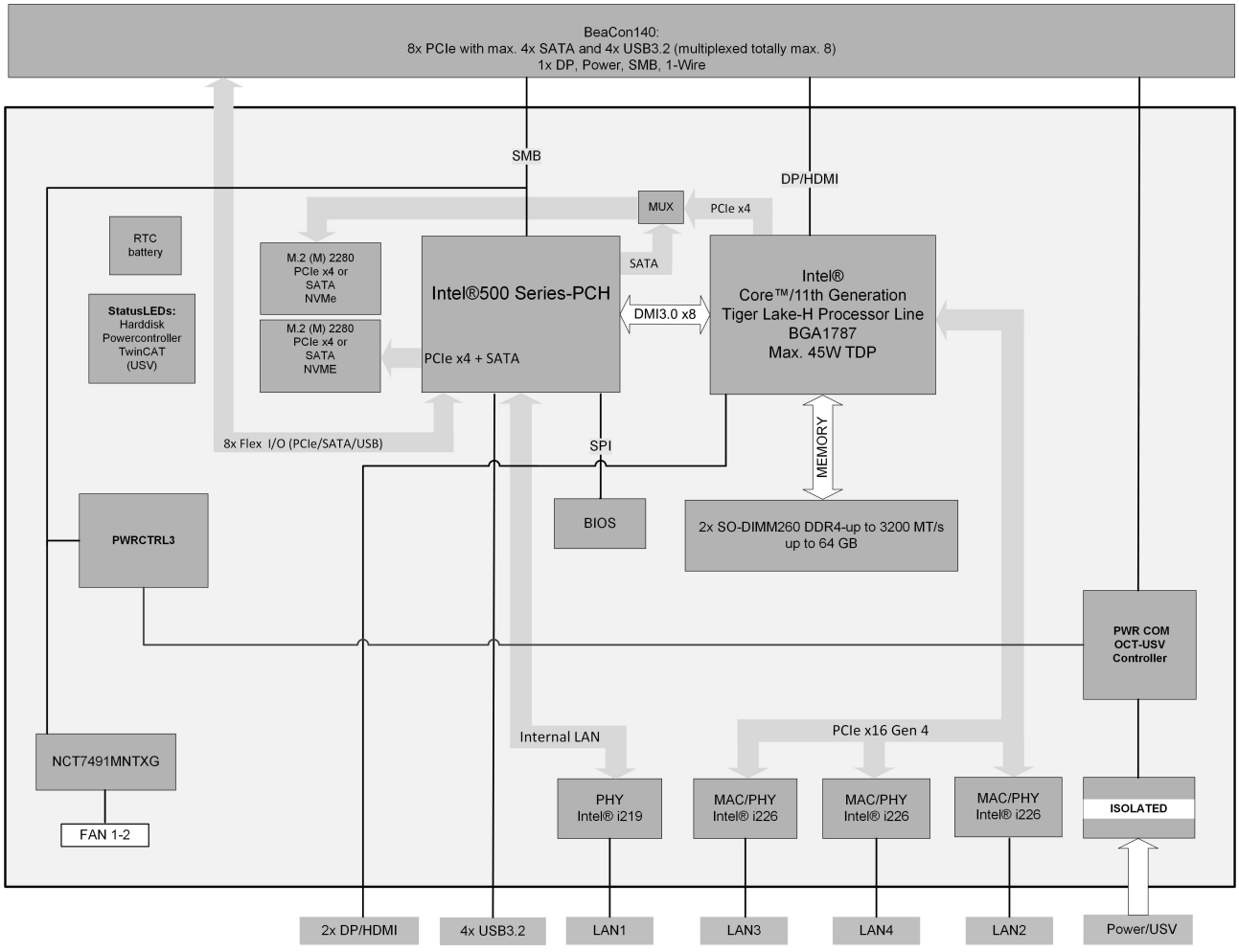


Fig. 1: Block diagram CB6472-TGL-H

5.2 List of features

List of features	
CB6472	
CPU Intel®	Celeron® 6600HE (2C/8M/2.6 GHz), TDP 35 W) Core™ i3-11100HE (4C/8M/2.4 GHz), TDP 45 W Core™ i5-11500HE (6C/12M/2.6 GHz), TDP 45 W Core™ i7-11850HE (8C/24M/2.6 GHz), TDP 45 W
Socket	FCBGA1787
Memory	2x SO-DIMM260 1.2 V DDR4-3200 Maximum memory capacity 64 GB
I/O front panel	1 x power 2x DisplayPort (connection of an HDMI adapter for an HDMI signal is possible.) 4x LAN 10/100/1000/2500 4x USB 3.2 GEN2
I/O internal	2x M.2 (M) sockets, signals dependent on chipset (see: Internal: M.2 Key-M (P1201 and P1202) [▶ 26]) 1x BeaCon140, signals (see: Internal: BeaCon140 (P1200) [▶ 29])
Graphic resolution	Max. resolution 4096x2304@60Hz (HDMI 2.0b, 4K) Max. resolution 7068x4320@60Hz (DP1.4) Max. resolution 4096x2304@60Hz (eDP1.4b – integrated flat screen)
RTC	Exchangeable, horizontal on-board battery Optional: horizontal battery on expansion card
BIOS	AMI® Aptio V
Power supply	24 V_{DC} power supply unit (+20 % / - 15 %) Overvoltage and undervoltage protection Reverse polarity protection, UPS-OCT possible
Format	120 x 120 mm, electrically isolated

Availability of the processors

The list of features lists all the processors that can be ordered. Their actual availability depends on the manufacturer.

5.3 Specifications and documents

The following documents, specifications or webpages were used for the preparation of this manual or as further technical documentation respectively.

- **PCI specification**
- Version 2.3 or 3.0
- www.pcisig.com
- **PCI Express® Base Specification**
- Version 5.0
- www.pcisig.com
- **ACPI specification**
- Version 5.0
- www.acpi.info
- **ATA/ATAPI specification**
- Version 7 Rev. 1
- www.t13.org
- **USB specifications**
- www.usb.org
- **SM-Bus specification**
- Version 2.0
- www.smbus.org
- **Intel® chip descriptions**
- Intel® Core™ Processor Product Family datasheet
- www.intel.com
- **Intel® chip description**
- I219 Datasheet
- I226 Datasheet
- www.intel.com
- **SMSC® chip description**
- SCH3114 datasheet (NDA required)
- www.smsc.com
- **American Megatrends®**
- Aptio™ Text Setup Environment (TSE) User Manual
- www.ami.com
- **American Megatrends®**
- Aptio™ 5.x Status Codes
- www.ami.com

6 Detailed description

6.1 Power supply

The board is supplied with an isolated input voltage with a nominal rating of 24 V. In normal operation the DC/DC power rail is supplied with this voltage. A UPS can also be implemented via an OCT signal (OCT = One Cable Technology).

UPS-OCT

The UPS OCT can only be implemented with the Beckhoff CU81XX-xxxx UPS.

6.2 CPU

The processors used are 11th generation Intel® Celeron and Core processors (Tigerlake-H). The processors of 11th generation are characterized by very low power consumption and offer contemporary performance with clock rates of currently up to 4.4 GHz (max. turbo clock frequency).

6.3 Memory

SO-DIMM260 memory modules (DDR4-3200), as commonly used in notebooks, are used on the CB6472 board. For technical and mechanical reasons, it is possible that certain memory modules cannot be used. Information regarding the recommended memory modules can be obtained from your distributor.

Depending on the product version, a memory extension up to 64 GB is possible with the currently available SO-DIMM260 modules.

NOTICE

Same memory modules

When populating both memory slots, make sure that you use identical memory modules.

6.4 M.2 Key M

Expansion cards that fulfill the M.2 specification are characterized by an extremely small format and – depending on the card type – flexible dimensions.

M.2 cards can easily and simply be inserted by plugging them into the slot and fixing them with a screw.

These M.2 sockets (2280) of the CB6472 support Key M. With a multiplexer, you can feed either PCIe or SATA signals out of a socket.

Different signals are supported, depending on the chipset used. The table in chapter M.2 lists all the interfaces supported, depending on the chipset in use.

Driver compatibility

For optimum driver compatibility, we recommend the use of a Microsoft® Windows 10 operating system.

7 Interfaces

7.1 Note on the use of cables

Requirement for the cabling!

The cables used must meet certain requirements for most interfaces. For example, twisted and shielded cables are necessary for a reliable USB 2.0 connection. Limitations in the maximum cable length are also no rarity. All of these interface-specific requirements are to be taken from the respective specifications and observed accordingly.

7.2 Interface overview

The following figure shows the interfaces of the CB6472 board. The table below shows the function of the respective interface, as well as the manual page where you can find further information on this connection.

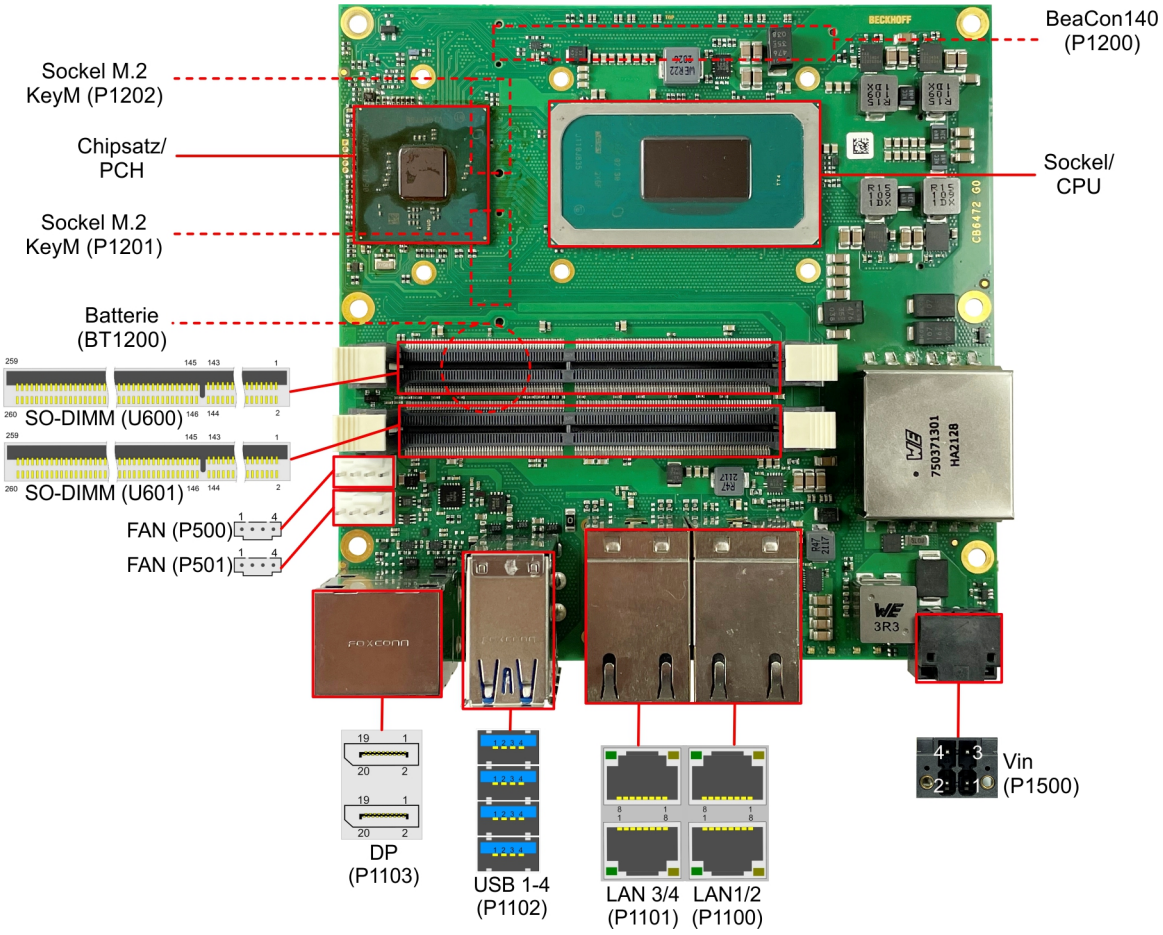


Fig. 2: CB6472 interface overview

7.3 List of interfaces

The listing is clockwise, starting with the power supply (P1500).

Number	Function (designation)	Page
P1500	Vin	Front panel: power supply P1500 [▶ 16]
P1100/1101	LAN 1 - 4	Front panel: LAN 1 – 4 (P1100, P1101) [▶ 17]
P1102	USB3.2 A - D	Front panel: USB3.2 Gen2 A - D (P1102) [▶ 18]
P1103	DisplayPorts	Front panel: DisplayPort A and B (P1103) [▶ 19]
P500/501	FAN	Internal: FAN (P500, P501) [▶ 20]
U601/600	SODIMM	Internal: Memory (U600, U601) [▶ 21]
BT1200*	Battery	Internal: Battery (BT1200) [▶ 26]
P1201*	M.2 (Key M) 2280	Internal: M.2 Key-M (P1201 and P1202) [▶ 26]
P1200*	BeaCon140	Internal: BeaCon140 (P1200) [▶ 29]

*not shown (see underside of the board)

8 External interfaces

8.1 Front panel: power supply P1500

P1500

Fig. 3: CB6472 Power

The connection for the power supply is implemented as a 2x2 pin housing connector (P20THR-1818504). The main power supply (24 V) for the module is on pin 3. This can also be implemented as UPS-OCT (One Cable Technology), i.e. the signal for the UPS is also transmitted to the board via this cable.

Pin assignment of the power plug:					
Description	**Signal**	**Pin**		**Signal**	**Description**
PC_On: Input for starting and shutting down the PC. Low (0 V or open contact): PC starts. High (>3 V): PC shuts down.	PC_On	1	3	Vin	Supply voltage 24 V UPS-OCT is supported.
Power Status: Output of the Power Status. The voltage corresponds to the positive supply voltage and can be loaded up to 500 mA. Low (0 V): PC is off. High (Vin): PC is on.	PowerStatus	2	4	GND	Ground

Function restrictions PC_Start switch

Please note that there are system states in which the activation of a connected PC_Start switch is ignored by the system, e.g. during booting of a Windows operating system. In this case, repeat the operation of the switch after a few seconds. The same applies to connected PC_Start push buttons.

8.2 Front panel: LAN 1 – 4 (P1100, P1101)

The board has four Gigabit-LAN connections. 10BaseT-, 100BaseT-. 1000BaseT and 2500BaseT - compatible network components can be connected. The required speed is selected automatically. Auto-Cross and Auto-Negotiate are available as well as PXE and RPL functionality. Controller is Intel®'s i219 for LAN1 and i226 for LAN2, 3 and LAN4.

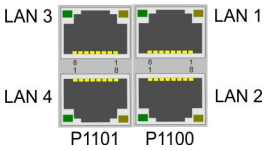


Fig. 4: CB6472 LAN (P1100-1101)

Pin assignment of LAN connector		
Pin	**Name**	**Description**
1	LAN-3#	LAN line 3 -
2	LAN-3	LAN line 3 +
3	LAN-2#	LAN line 2 #
4	LAN-2	LAN line 2 +
5	LAN-1#	LAN line 1 -
6	LAN-1	LAN line 1 +
7	LAN-0#	LAN line 0 -
8	LAN-0	LAN line 0 +

The LEDs of the LAN interfaces indicate the activity and speed of the data transmission (Mbit/s). The left-hand LED lights up when there is a connection and activity, and the right-hand LED during data transmission:

Left-hand LED **Steadily lit when there is a connection,** **Flashing during data transmission**	**Right-hand LED** **Steadily lit during data transmission**	**Mbit/s**
Green	Green	2500
Green	Orange	1000
Green	Off	100/10

Real-time applications

The Ethernet port connected via PCIe is usually suitable for cycle times <= 1 ms and for distributed clock applications with EtherCAT.
The Ethernet port integrated in the chipset is usually suitable for real-time Ethernet applications with cycle times > 1 ms (without distributed clocks).

8.3 Front panel: USB3.2 Gen2 A - D (P1102)

The CB6472 provides four USB3.2 ports in a combination connector.

The USB channels support the USB specification 3.2. All necessary settings for USB can be made by the BIOS.

Note that the "USB Mouse and Keyboard" functionality of the BIOS setup is only required if the operating system does not provide USB support.

Do not select this function for settings in the setup and for booting Windows with a connected USB mouse and keyboard, because this would result in significant performance limitations.

The individual USB interfaces can supply a current of up to 900 mA and are electronically protected.

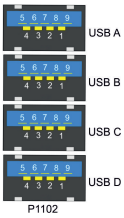


Fig. 5: CB6472 USB (P1102)

Pin assignment USB3.2 Gen2 connector:		
Pin	**Signal**	**Description**
1	VCC	Supply voltage 5 V
2	D-	Data - (USB 2.0)
3	D+	Data + (USB 2.0)
4	GND	Ground
5	RX-	Receive line - (USB 3.2)
6	RX+	Receive line + (USB 3.2)
7	GND	Ground
8	TX-	Transmit line - (USB 3.2)
9	TX+	Transmit line + (USB 3.2)

Switch-off of the USB ports by overcurrent protection

USB ports A and B and USB ports C and D are each protected by a common overcurrent detection. In the event of overcurrent occurring on one of the ports, therefore, both commonly protected USB ports will be switched off.

8.4 Front panel: DisplayPort A and B (P1103)

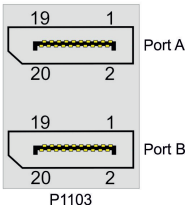


Fig. 6: CB6472 Display Port (P1103)

For devices with a DisplayPort connection a corresponding standard connector (Foxconn 3VD11203-DPA1-4H) with two DisplayPort connections is available.

The interface additionally provides HDMI/DVI signals that can be used with aid of an adapter. Please consult your distributor with regard to a suitable adapter.

Pin assignment DisplayPort A and B:					
Description	**Signal**	**Pin**		**Signal**	**Description**
Display Port Lane 0 +	L0	1	2	GND	Ground
Display Port Lane 0 -	L#0	3	4	L1	Display Port Lane 1 +
Ground	GND	5	6	L#1	Display Port Lane 1 -
Display Port Lane 2 +	L2	7	8	GND	Ground
Display Port Lane 2 -	L#2	9	10	L3	Display Port Lane 3 +
Ground	GND	11	12	L#3	Display Port Lane 3 -
DP / HDMI	HDMI#	13	14	GND	Ground
Auxiliary plus	AUX	15	16	GND	Ground
Auxiliary minus	AUX#	17	18	HPD	Hot Plug Detect
Ground	GND	19	20	3.3 V	Supply voltage 3.3 V

Switching to HDMI

DisplayPort signals are led out via the interface by default. With the use of a level shifter cable the board switches the DisplayPort specification 1.1 automatically to HDMI signals.

9 Internal interfaces

9.1 Internal: FAN (P500, P501)

The computer board has two 4-pin fan connectors. Here you can connect fans with a supply voltage of 12 V directly to the computer board. A signal for monitoring the fan speed is also available.

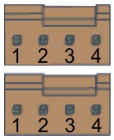


Fig. 7: CB6472 FAN P500-501

Pin assignment fan connector:		
Pin	**Signal**	**Description**
1	GND	Ground
2	12 V	Supply voltage 12 V regulated
3	TACH	Speed monitoring
4	PWM	Speed control

9.2 Internal: Memory (U600, U601)

On the CB6472 board there are two SO-DIMM260 memory slots for DDR4-3200 RAM. For technical and mechanical reasons, it is possible that certain memory modules cannot be used. Information regarding the recommended memory modules can be obtained from your distributor.

With two sockets, a memory extension up to 64 GB is possible with currently available modules. Identical memory modules should be inserted in the two memory sockets.

All timing parameters for the different makes and versions are automatically set by the BIOS.

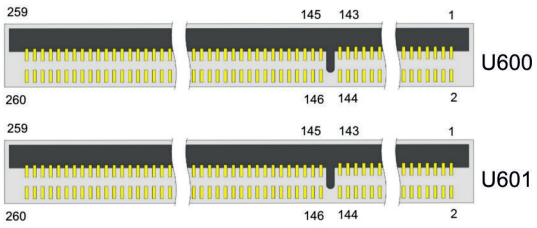


Fig. 8: CB6472 SODIMM

Pin assignment memory socket:					
Description	**Signal**	**Pin1**		**Signal**	**Description**
Ground	GND	1	2	GND	Ground
Data line 5	DQ5	3	4	DQ4	Data line 4
Ground	GND	5	6	GND	Ground
Data line 1	DQ1	7	8	DQ0	Data line 0
Ground	GND	9	10	GND	Ground
Data Strobe 0 -	DQS0_c	11	12	NC	Reserved
Data Strobe 0 +	DQS0_t	13	14	GND	Ground
Ground	GND	15	16	DQ6	Data line 6
Data line 7	DQ7	17	18	GND	Ground
Ground	GND	19	20	DQ2	Data line 2
Data line 3	DQ3	21	22	GND	Ground
Ground	GND	23	24	DQ12	Data line 12
Data line 13	DQ13	25	26	GND	Ground
Ground	GND	27	28	DQ8	Data line 8
Data line 9	DQ9	29	30	GND	Ground
Ground	GND	31	32	DQS1_c	Data Strobe 1 -
Reserved	NC	33	34	DQS1_t	Data Strobe 1 +
Ground	GND	35	36	GND	Ground
Data line 15	DQ15	37	38	DQ14	Data line 14
Ground	GND	39	40	GND	Ground
Data line 10	DQ10	41	42	DQ11	Data line 11
Ground	GND	43	44	GND	Ground
Data line 21	DQ21	45	46	DQ20	Data line 20
Ground	GND	47	48	GND	Ground
Data line 17	DQ17	49	50	DQ16	Data line 16
Ground	GND	51	52	GND	Ground
Data Strobe 2 -	DQS2_c	53	54	NC	Reserved
Data Strobe 2 +	DQS2_t	55	56	GND	Ground
Ground	GND	57	58	DQ22	Data line 22
Data line 23	DQ23	59	60	GND	Ground
Ground	GND	61	62	DQ18	Data line 18
Data line 19	DQ19	63	64	GND	Ground
Ground	GND	65	66	DQ28	Data line 28
Data line 29	DQ29	67	68	GND	Ground
Ground	GND	69	70	DQ24	Data line 24
Data line 25	DQ25	71	72	GND	Ground
Ground	GND	73	74	DQS3_c	Data Strobe 3 -
Reserved	NC	75	76	DQS3_t	Data Strobe 3 +
Ground	GND	77	78	GND	Ground
Data line 30	DQ30	79	80	DQ31	Data line 31
Ground	GND	81	82	GND	Ground
Data line 26	DQ26	83	84	DQ27	Data line 27
Ground	GND	85	86	GND	Ground
Reserved	NC	87	88	NC	Reserved
Ground	GND	89	90	GND	Ground
Reserved	NC	91	92	NC	Reserved
Ground	GND	93	94	GND	Ground

Pin assignment memory socket:					
Description	**Signal**	**Pin1**		**Signal**	**Description**
Data Strobe 8 -	DQS8_c	95	96	NC	Reserved
Data Strobe 8 +	DQS8_t	97	98	GND	Ground
Ground	GND	99	100	NC	Reserved
Reserved	NC	101	102	GND	Ground
Ground	GND	103	104	N C	Reserved
Reserved	NC	105	106	GND	Ground
Ground	GND	107	108	RESET_n	Reset
Clock Enable 0	CKE0	109	110	CKE1	Clock Enable 1
Supply voltage 1.2 V	VCC	111	112	VCC	Supply voltage 1.2 V
Bank Group Input 1	BG1	113	114	ACT_n	Activation Command Input
Bank Group Input 0	BG0	115	116	ALERT_n	Alert
Supply voltage 1.2 V	VCC	117	118	VCC	Supply voltage 1.2 V
Address line 12	A12	119	120	A11	Address line 11
Address line 9	A9	121	122	A7	Address line 7
Supply voltage 1.2 V	VCC	123	124	VCC	Supply voltage 1.2 V
Address line 8	A8	125	126	A5	Address line 5
Address line 6	A6	127	128	A4	Address line 4
Supply voltage 1.2 V	VCC	129	130	VCC	Supply voltage 1.2 V
Address line 3	A3	131	132	A2	Address line 2
Address line 1	A1	133	134	EVENT_n	Event
Supply voltage 1.2 V	VCC	135	136	VCC	Supply voltage 1.2 V
Clock-Signal 0 +	CK0_t	137	138	CK1_t	Clock 1 +
Clock-Signal 0 -	CK0_c	139	140	CK1_c	Clock 1 -
Supply voltage 1.2 V	VCC	141	142	VCC	Supply voltage 1.2 V
Even parity check	Parity	143	144	A0	Address line 0
SDRAM Bank 2	BA1	145	146	A10/AP	Address line 10/Autoprecharge
Supply voltage 1.2 V	VCC	147	148	VCC	Supply voltage 1.2 V
Chip Select 0	CS0_n	149	150	BA0	Bank Adress 0
Address line 14/Write Enable	A14/WE_n	151	152	A16/RAS_n	Address line 16/ Row Adress Strobe
Supply voltage 1.2 V	VCC	153	154	VCC	Supply voltage 1.2 V
On Die Termination 0	ODT0	155	156	A15/CAS_n	Address line 15/ Column Adress Strobe
Chip Select 1	CS1_n	157	158	A13	Address line 13
1.2 V	VCC	159	160	VCC	Supply voltage 1.2 V
On Die Termination 1	ODT1	161	162	NC	Reserved
Supply voltage 1.2 V	VCC	163	164	VREFCA	Reference voltage
Reserved	NC	165	166	SA2	SPD Address 2

Pin assignment memory socket:					
Description	**Signal**	**Pin1**		**Signal**	**Description**
Ground	GND	167	168	GND	Ground
Data line 37	DQ37	169	170	DQ36	Data line 36
Ground	GND	171	172	GND	Ground
Data line 33	DQ33	173	174	DQ32	Data line 32
Ground	GND	175	176	GND	Ground
Data Strobe 4 -	DQS4_c	177	178	NC	Reserved
Data Strobe 4 +	DQS4_t	179	180	GND	Ground
Ground	GND	181	182	DQ39	Data line 39
Data line 38	DQ38	183	184	GND	Ground
Ground	GND	185	186	DQ35	Data line 35
Data line 34	DQ34	187	188	GND	Ground
Ground	GND	189	190	DQ45	Data line 45
Data line 44	DQ44	191	192	GND	Ground
Ground	GND	193	194	DQ41	Data line 41
Data line 40	DQ40	195	196	GND	Ground
Ground	GND	197	198	DQS5_c	Data Strobe 5 -
Reserved	NC	199	200	DQS5_t	Data Strobe 5 +
Ground	GND	201	202	GND	Ground
Data line 46	DQ46	203	204	DQ47	Data line 47
Ground	GND	205	206	GND	Ground
Data line 42	DQ42	207	208	DQ43	Data line 43
Ground	GND	209	210	GND	Ground
Data line 52	DQ52	211	212	DQ53	Data line 53
Ground	GND	213	214	GND	Ground
Data line 49	DQ49	215	216	DQ48	Data line 48
Ground	GND	217	218	GND	Ground
Data Strobe 6 -	DQS6_c	219	220	NC	Reserved
Data Strobe 6 +	DQS6_t	221	222	GND	Ground
Ground	GND	223	224	DQ54	Data line 54
Data line 55	DQ55	225	226	GND	Ground
Ground	GND	227	228	DQ50	Data line 50
Data line 51	DQ51	229	230	GND	Ground
Ground	GND	231	232	DQ60	Data line 60
Data line 61	DQ61	233	234	GND	Ground
Ground	GND	235	236	DQ57	Data line 57
Data line 56	DQ56	237	238	GND	Ground
Ground	GND	239	240	DQS7_c	Data Strobe 7 -
Reserved	NC	241	242	DQS7_t	Data Strobe 7 +
Ground	GND	243	244	GND	Ground
Data line 62	DQ62	245	246	DQ63	Data line 63
Ground	GND	247	248	GND	Ground
Data line 58	DQ58	249	250	DQ59	Data line 59
Ground	GND	251	252	GND	Ground
SMBus Clock	SCL	253	254	SDA	SMBus Data
I²C Power for SPD EEProm	VCCSPD	255	256	SA0	SPD Address 0

Pin assignment memory socket:					
Description	**Signal**	**Pin1**		**Signal**	**Description**
DRAM Activating Power	VPP	257	258	VTT	Termination voltage
DRAM Activating Power	VPP	259	260	SA1	SPD Address 1

9.3 Internal: Battery (BT1200)

The board is delivered with a CR2032 battery holder (Renata VBH2032-1) including a 3 V battery.

UL conformity

All technical measures for UL conformity are already integrated on the board.

Accordingly, no additional actions are necessary for the connection of an RTC battery. The battery must be connected directly.

BT1200

Fig. 9: CB6472 BAT

Synchronism of the RTC

The quartz of the RTC reacts to temperature fluctuations. Therefore, correct synchronism of the RTC is possible only with suitable and sufficient cooling!

9.4 Internal: M.2 Key-M (P1201 and P1202)

The CB6472 is equipped with two M.2 Key-M sockets, one of which has a multiplexer for leading out SATA or PCIe signals. You can plug an M.2-2280 card (Key M, P1201 and P1202) into this. Adapter cards with standard plug connectors are available as accessories. Please contact your distributor for this.

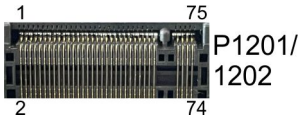


Fig. 10: CB6472 M.2M P1201-1202

Pin assignment M.2 (Key M) P1201:					
Description	**Signal**	**Pin**		**Signal**	**Description**
Ground	GND	1	2	3.3 V1	Standby supply voltage S3.3 V
Ground	GND	3	4	3.3 V2	Standby supply voltage S3.3 V
PCIe Lane 3 Receive -	PER3#	5	6	N/C	(not led out)
PCIe Lane 3 Receive +	PER3	7	8	N/C	(not led out)
Ground	GND	9	10	GPIO9 DAS DDS LED1	NVMELED#
PCIe Lane 3 Transmit -	PET3#	11	12	3.3 V3	Standby supply voltage S3.3 V
Pcie Lane 3 Transmit +	PET3	13	14	3.3 V4	Standby supply voltage S3.3 V
Ground	GND	15	16	3.3 V5	Standby supply voltage S3.3 V
PCIe Lane 2 Receive -	PER2#	17	18	3.3 V6	Standby supply voltage S3.3 V
PCIe Lane 2 Receive +	PER2	19	20	N/C	(not led out)
Ground	GND	21	22	N/C	(not led out)
PCIe Lane 2 Transmit -	PET2#	23	24	N/C	(not led out)
PCIe Lane 2 Transmit +	PET2	25	26	N/C	(not led out)
Ground	GND	27	28	N/C	(not led out)
PCIe Lane 1 Receive -	PER1#	29	30	N/C	(not led out)
PCIe Lane 1 Receive +	PER1	31	32	N/C	(not led out)
Ground	GND	33	34	N/C	(not led out)
PCIe Lane 1 Transmit -	PET1#	35	36	N/C	(not led out)
PCIe Lane 1 Transmit +	PET1	37	38	DEVSLP	DeviceSleep
Ground	GND	39	40	N/C	(not led out)
PCIe Lane 0 Receive +	PER0# SATAB	41	42	N/C	(not led out)
PCIe Lane 0 Receive -	PER0 SATAB#	43	44	N/C	(not led out)
Ground	GND	45	46	N/C	(not led out)
PCIe Lane 0 Transmit -	PET0# SATAA#	47	48	N/C	(not led out)
PCIe Lane 0 Transmit +	PET0 SATAA	49	50	PRST#	PCIe Reset active low
Ground	GND	51	52	CLKREQ#	PCIe Clock Enable active low
PCIe Lane 1 Reference Clock -	REFCLK#	53	54	PEWAKE#	Link Reactivation active low
PCIe Lane 1 Reference Clock +	REFCLK	55	56	N/C	(not led out)

Pin assignment M.2 (Key M) P1201:					
Description	**Signal**	**Pin**		**Signal**	**Description**
Ground	GND	57	58	N/C	(not led out)
(not led out)	N/C	59	60	N/C	(not led out)
(not led out)	N/C	61	62	N/C	(not led out)
(not led out)	N/C	63	64	N/C	(not led out)
(not led out)	N/C	65	66	N/C	(not led out)
(not led out)	N/C	67	68	SUSCLK	System clock
Configuration pin	CFG_PCIe/ SATA	69	70	3.3 V	Standby supply voltage S3.3 V
Ground	GND	71	72	3.3 V	Standby supply voltage S3.3 V
Ground	GND	73	74	3.3 V	Standby supply voltage S3.3 V
Ground	GND	75			

9.5 Internal: BeaCon140 (P1200)

In conjunction with the chipset, the BeaCon140 connector allows flexible extension of the CB6472's I/O functions. It provides up to 8 PCIe lanes, of which a maximum of 4 can be multiplexed with SATA3.0 (6G) and a maximum of 4 with PCIe lines, as well as a maximum of 3 PCIe lines with a maximum of 3 USB3.1-GEN2 lines (see table). DisplayPort, SSIC, SMBus and 1-Wire signals can be fed out via the BeaCon140 connector. The extension board takes care of the configuration of the IO functions. A PIC on the expansion card contains the configuration data, which are communicated to the board upon connection and thus enable an uncomplicated and self-configuring extension of the I/O options.

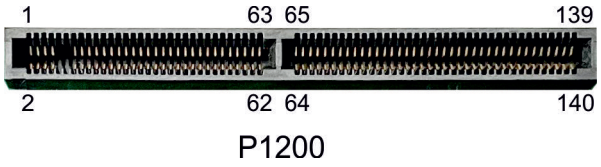


Fig. 11: CB6472 BeaCon140 P1200

Pin assignment of BeaCon140 connector:					
Description	**Signal**	**Pin**		**Signal**	**Description**
P_VLoad 24 V S UPS output	VOLOAD/ P_VOLOAD1	2	1	P_VIN1/VIN1	P_Vin S UPS input
P_VLoad 24 V S UPS output	VOLOAD/ P_VOLOAD2	4	3	P_VIN2/VIN2	P_Vin S UPS input
(not led out)	5V/NC	6	5	P_GND/GND	Ground
(not led out)	5V/NC	8	7	P_GND/GND	Ground
	INSULATION				
Standby 5 Volt	S5V	14	13	S3.3 V	Standby 3.3 V
Ground	GND	16	15	GND	Ground
PCIe Lane 1 Transmit +	PE1/SATA4-TX	18	17	RX-SATA4/ PE1	PCIe Lane 1 Receive +
PCIe Lane 1 Transmit -	PE1/SATA4-TX#	20	19	RX-SATA4/ PE1#	PCIe Lane 1 Receive -
Ground	GND	22	21	GND	Ground
PCIe Clock Lane 1 +	PECLK1	24	23	PECLK2	PCIe Clock Lane 2 +
PCIe Clock Lane 1 -	PECLK1#	26	25	PECLK2#	PCIe Clock Lane 2 -
Ground	GND	28	27	GND	Ground
PCI Lane 2 Transmit +	PE2/SATA3-TX	30	29	RX-SATA3/ PE2	PCIe Lane 2 Receive +
PCI Lane 2 Transmit -	PE2/SATA3-TX#	32	31	RX-SATA3/ PE2#	PCIe Lane 2 Receive -
Ground	GND	34	33	GND	Ground
PCIe Lane 3 Transmit +	PE3/SATA2-TX	36	35	RX-SATA2/ PE3	PCIe Lane 3 Receive +
PCIe Lane 3 Transmit -	PE3/SATA2-TX#	38	37	RX-SATA2/ PE3#	PCIe Lane 3 Receive -
Ground	GND	40	39	GND	Ground
PCIe Clock Lane 3 +	PECLK3	42	41	PECLK4	PCIe Clock Lane 4 +
PCIe Clock Lane 3 -	PECLK3#	44	43	PECLK4#	PCIe Clock Lane 4 -
Ground	GND	46	45	GND	Ground
PCIe Lane 4 Transmit +	PE4/SATA1-TX	48	47	RX-SATA1/ PE4	PCIe Lane 4 Receive +
PCIe Lane 4 Transmit -	PE4/SATA1-TX#	50	49	RX-SATA1/ PE4#	PCIe Lane 4 Receive -
Ground	GND	52	51	GND	Ground
PCIe Clock Lane 1 Enable active low	PCKE1/ DEVSLP4#	54	53	DVSLP3/ PCKE2#	PCIe Clock Lane 2 Enable active low
PCIe Clock Lane 3 Enable -	PCKE3/ DEVSLP2#	56	55	DEVSLP1/ PCKE4#	PCIe Clock Lane 4 Enable -
PCIe Reset active low	PERST#	58	57	PEWAKE#	PCIe Wake active low
SMBus Clock	SMBCLK	60	59	SMBDAT	SMBus Data
		KEY			
SMBus Alert active low	SMB-Alert#	62	61	1Wire	1Wire

Pin assignment of BeaCon140 connector:					
Description	**Signal**	**Pin**		**Signal**	**Description**
PCIe Clock Lane 5 Enable	PCKE5/ OC4#	64	63	OC3/PCKE6#	PCIe Clock Lane 6 Enable -
KEY					
PCIe Clock Lane 7 Enable -	PCKE7/ OC2#	66	65	OC1/PCKE8#	PCIe Clock Lane 8 Enable -
Ground	GND	68	67	GND	Ground
PCIe Lane 5 Transmit +	PE5/USB3-4/ USBC1-TX	70	69	RX-USBC1/ USB3-4/PE5	PCIe Lane 5 Receive +
PCIe Lane 5 Transmit -	PE5/USB3-4/ USBC1-TX#	72	71	RX-USBC1/ USB3-4/PE5#	PCIe Lane 5 Receive -
USB 4.D +	USB2-4#/ (GND)	74	73	USB2-3/ (GND)	USB 3.D +
PCIe Clock Lane 5 +	PECLK5/ (GND)	76	75	PECLK6/ (GND)	PCIe Clock Lane 6 +
PCIe Clock Lane 5 -	PECLK5/ (GND)	78	77	PECLK6#/ (GND)	PCIe Clock Lane 6 -
USB 4.D -	USB2-4#/(GND)	80	79	USB2-3 D#/(GND)	USB 3.D -
PCIe Lane 6 Transmit +	PE6/USB3-3/ USBC2-TX	82	81	RX-USBC2/ USB3-3/PE6	PCIe Lane 6 Receive +
PCIe Lane 6 Transmit -	PE6/USB3-3-TX/ USBC2-TX#	84	83	RX-USBC2/ USB3-3/PE6#	PCIe Lane 6 Receive -
Ground	GND	86	85	GND	Ground
PCIe Lane 7 Transmit +	PE7/USB3-2-TX/TCPTX1	88	87	TCPTXRX1/ RX- USB3-2/ PE7	PCIe Lane 7 Receive +
PCIe Lane 7 Transmit -	PE7/USB3-2-TX/TCPTX1#	90	89	TCPTXRX/ RX-USB3-2/ PE7#	PCIe Lane 7 Receive -
USB 2.D +	USB2-2 (GND)	92	91	USB2-1/ (GND)	USB 1.D +
PCIe Clock Lane 7 +	PECLK7/ (GND)	94	93	PECLK8/ (GND)	PCIe Clock Lane 8 +
PCIe Clock Lane 7 -	PECLK7#/ (GND)	96	95	PECLK8#/ (GND)	PCIe Clock Lane 8-
USB 2.D -	USB2-2#/ (GND)	98	97	USB2-1#/ (GND)	USB 1.D -
PCIe Lane 8 Transmit +	PE8/ USB3-1-TX/ TCPTX0	100	99	TCPTXRX0/ RX- USB3-1/ PE8	PCIe Lane 8 Receive +
PCIe Lane 8 Transmit -	PE8/ USB3-1-TX/ TCPTX0#	102	101	TCPTXRX/ RX-USB3-1/ PE8#	PCIe Lane 8 Receive -
Ground	GND	104	103	GND	Ground
KEY					
SATA GP 1	SATAGP1	106	105	SATAGP2	SATA GP 2
SATA GP 3	SATAGP3	108	107	SATAGP4	SATA GP 4
TwinCAT LED Red	TCLEDR	110	109	TCLEDG	TwinCAT LED Green
TwinCAT LED Blue	TCLEDB	112	111	RES2	LAN-Sync
HDLED active low	SATALED	114	113	USBPWREN	USB Power Enable
BATTe	BATT	116	115	PWRFAIL	S UPS
(not led out)	RES1	118	117	PWRGOOD	Power good

Pin assignment of BeaCon140 connector:					
Description	**Signal**	**Pin**		**Signal**	**Description**
Powerbutton active low	PWRBTN#	120	119	MRST#	Resetbutton active low
PSON	PSON	122	121	ATXPWRGD	ATX Power good
Ground	GND	124	123	GND	Ground
DisplayPort -/ HDMID	DP/DVI	126	125	DDCC/ DPAUX	DDC Clock/ DisplayPort Aux +
DisplayPort Hot Plug Detect	DPHPD	128	127	DDCD/ DPAUX#	DDC Daten/ DisplayPort Aux -
Ground	GND	130	129	GND	Ground
DisplayPort Lane 0 +	DPL0/ TMDSD2	132	131	TMDSD1/DPL1	DisplayPort Lane 1+
DisplayPort Lane 0 -	DPL0/ TMDSD2#	134	133	TMDSD1/ DPL1#	DisplayPort Lane 1 -
Ground	GND	136	135	GND	Ground
DisplayPort Lane 2+	DPL2/ TMDS0	138	137	TMDSD3/ DPL3	DisplayPort Lane 3 +
DisplayPort Lane 2 -	DPL2/ FMDS0#	140	139	TMDSD3/ DPL3#	DisplayPort Lane 3 -

Observe the current limits!

In order to avoid damaging the device, it is essential to observe the following current limits:

A maximum load of 2.8 A per pin must not be exceeded. On account of the different current consumptions of the usable processors the actual current consumption may be lower. The respective maximum values can be obtained from your distributor on inquiry.

Irrespective of the CPU in use, a maximum total load of 100 W must not be exceeded.

NOTICE

Signal mirroring with BeaCon Stack Up connector

With the Stack Up version of the BeaCon connector (connector at the top of the board), a stack is used for signal transfer to the mating connector. The signals are mirrored on this mating connector (Stack Down). There is no reflection on the stack.

10 BIOS

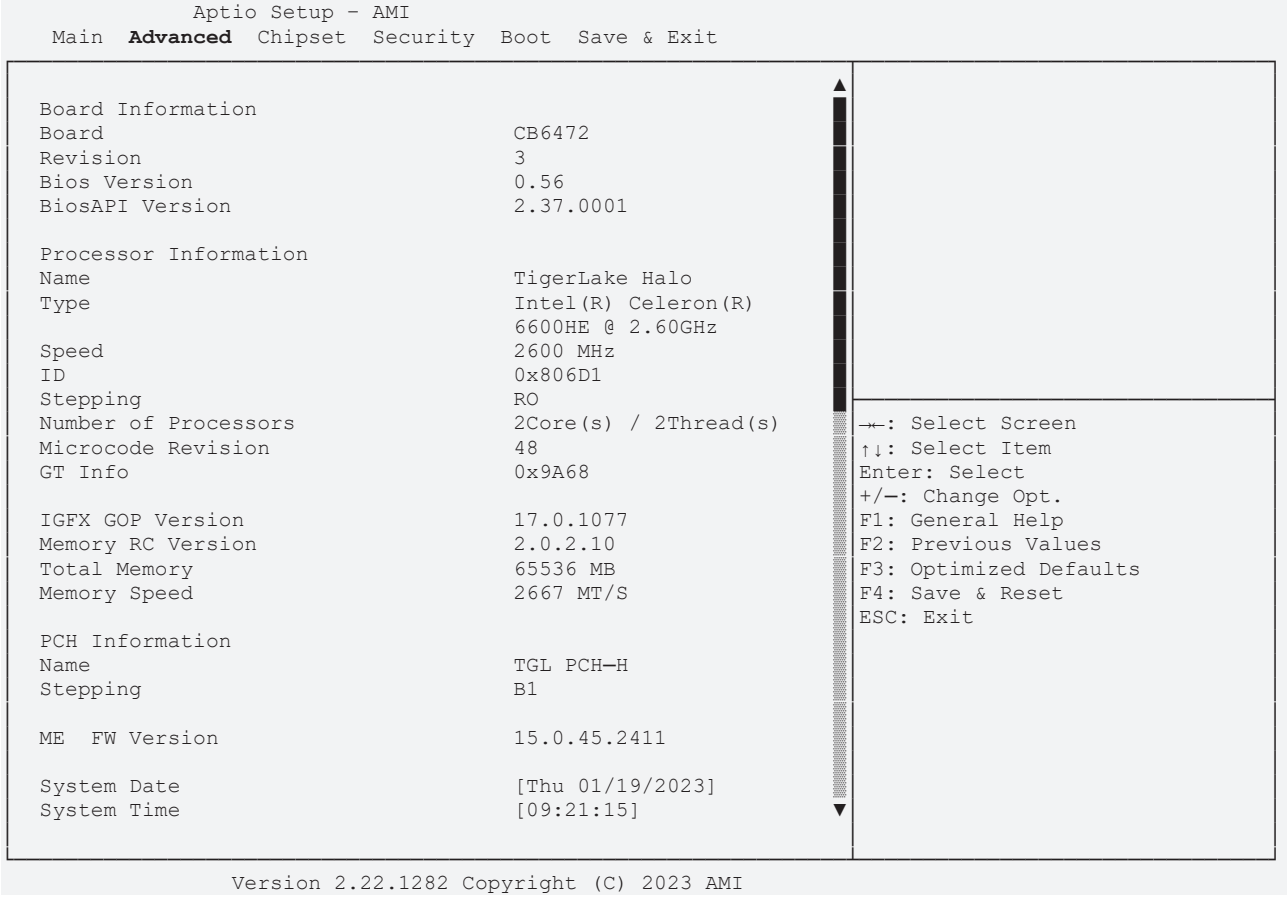
10.1 Using the setup

Within the individual setup pages the last saved settings can be restored can at any time with F2 ("Previous Values"). Use F3 ("Optimized Defaults") to load the factory defaults. Use F2/F3 to load the complete set of settings and F4 to save them (“Save & Reset”).

A "►" sign in front of the menu item indicates that a submenu is available. Use the arrow keys to navigate between menu items. Use the Enter key to select menu items and call submenus or selection dialogs.

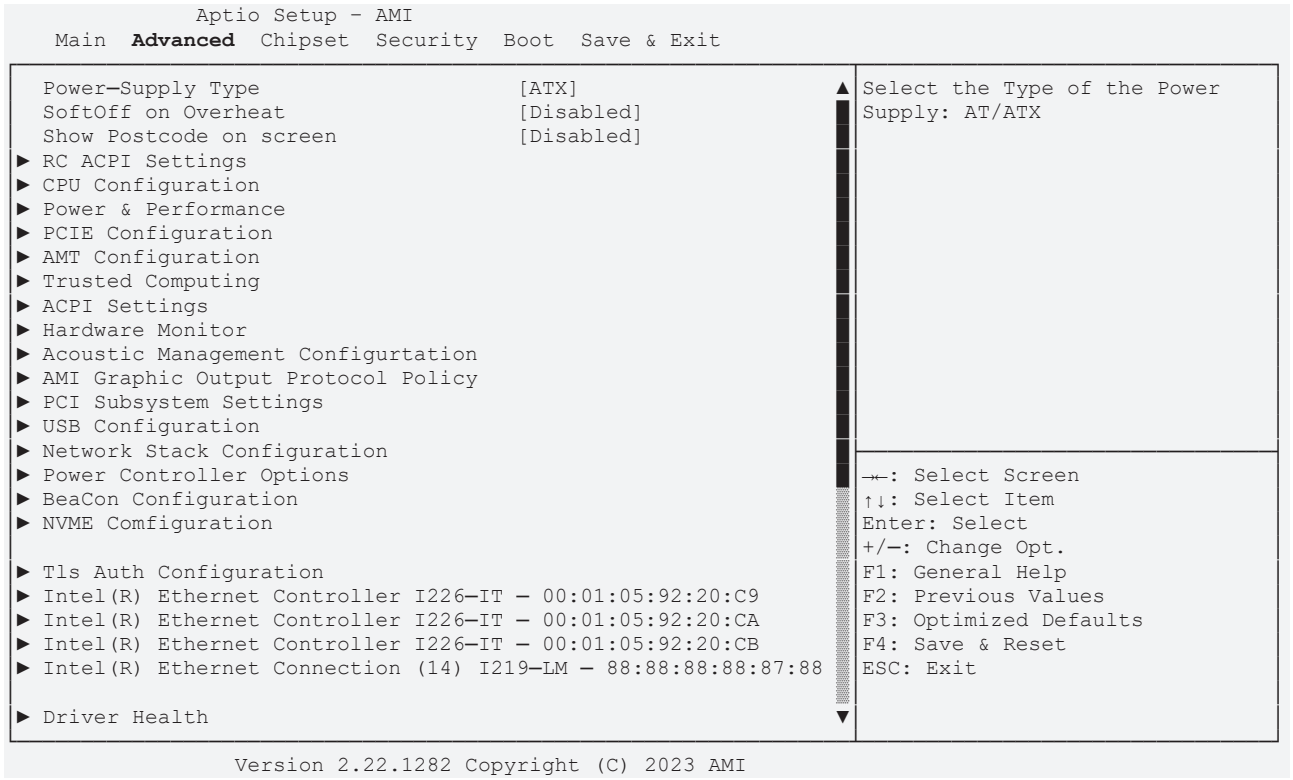
For each setup option a help text is displayed at the top right, which in many cases contains useful information about the option and permitted values, etc.

10.2 Main CB6472



BIOS entry	Options
Board	None
Revision	None
Bios version	None
Platform information	
TigerLake Halo, Intel® Celeron®T 6600HE @ 2.60GHz	
Speed	None
ID	None
Stepping	None
Number of Processors	None
Microcode Revision	None
GT Info	None
IGFX GOP Version	None
Memory RC version	None
Total Memory	None
Memory Speed	None
PCH information	None
Name	None
Stepping	None
ME FW version	None
System Date	Set the system date here.
System Time	Set the system time here.

10.3 Advanced CB6472

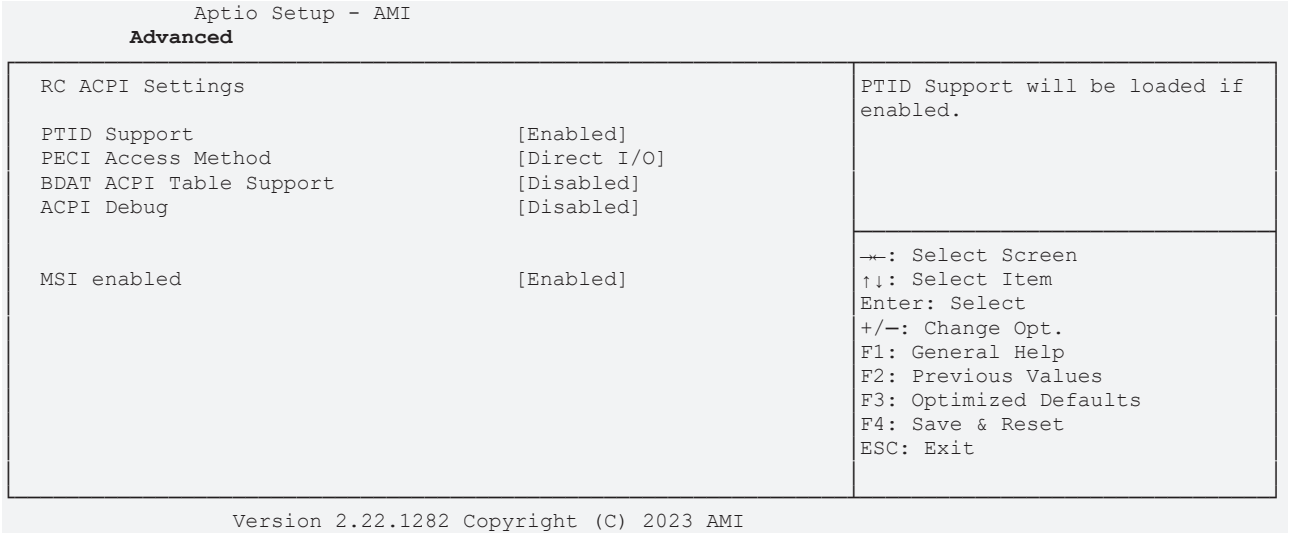


BIOS entry	Options
Power - Supply Type [ATX]	ATX / AT
SoftOff on Overheat	Disabled / Enabled
Show postcode on screen	Disabled / Enabled
▶RC ACPI Settings	Submenu see: RC ACPI Settings [▶ 38]
▶CPU Configuration	Submenu see: CPU Configuration [▶ 39]
▶PCIE Configuration	Submenu see: PCIE Configuration [▶ 43]
▶AMT Configuration	Submenu see: AMT Configuration [▶ 44]
▶Trusted Computing	Submenu see: Trusted Computing [▶ 48]
▶ACPI Settings	Submenu see: ACPI Settings [▶ 49]
▶Hardware Monitor	Submenu see: Hardware Monitor [▶ 49]
▶Acoustic Management Configuration	Submenu see: Acoustic Management Configuration [▶ 50]
▶AMI Graphic Output Protocol Policy	Submenu see: AMI Graphic Output Protocol Policy [▶ 50]
▶PCI Subsystem Settings	Submenu see: PCI Subsystem Settings [▶ 51]
▶USB Configuration	Submenu see: USB Configuration [▶ 52]
▶Network Stack Configuration	Disabled / Enabled
▶Power Controller Options	Submenu see: Power Controller Options [▶ 54]
▶BeaCon Configuration	Submenu see: BeaCon Configuration [▶ 55]
▶NVMe Configuration	Submenu see: NVMe Configuration [▶ 55]
▶Tls Auth Configuration	Submenu see: TLs Auth Configuration [▶ 56]
▶Intel® Ethernet Controller I226-IT - 00:01:05:92:20:C9	Submenu see: Intel Ethernet Controller I226-IT [▶ 58]
▶Intel® Ethernet Controller I226-IT - 00:01:05:92:20:CA	Submenu see: Intel Ethernet Controller I226-IT [▶ 59]
▶Intel® Ethernet Controller I226-IT - 00:01:05:92:20:CB	Submenu see: Intel Ethernet Controller I226-IT [▶ 60]
▶Intel® Ethernet Connection (14) I219-LM - 88:88:88:88:87:88	Submenu see: Intel Ethernet Connection I219-LM [▶ 61]
▶Driver Health	Submenu see: Driver Health [▶ 62]

MAC address

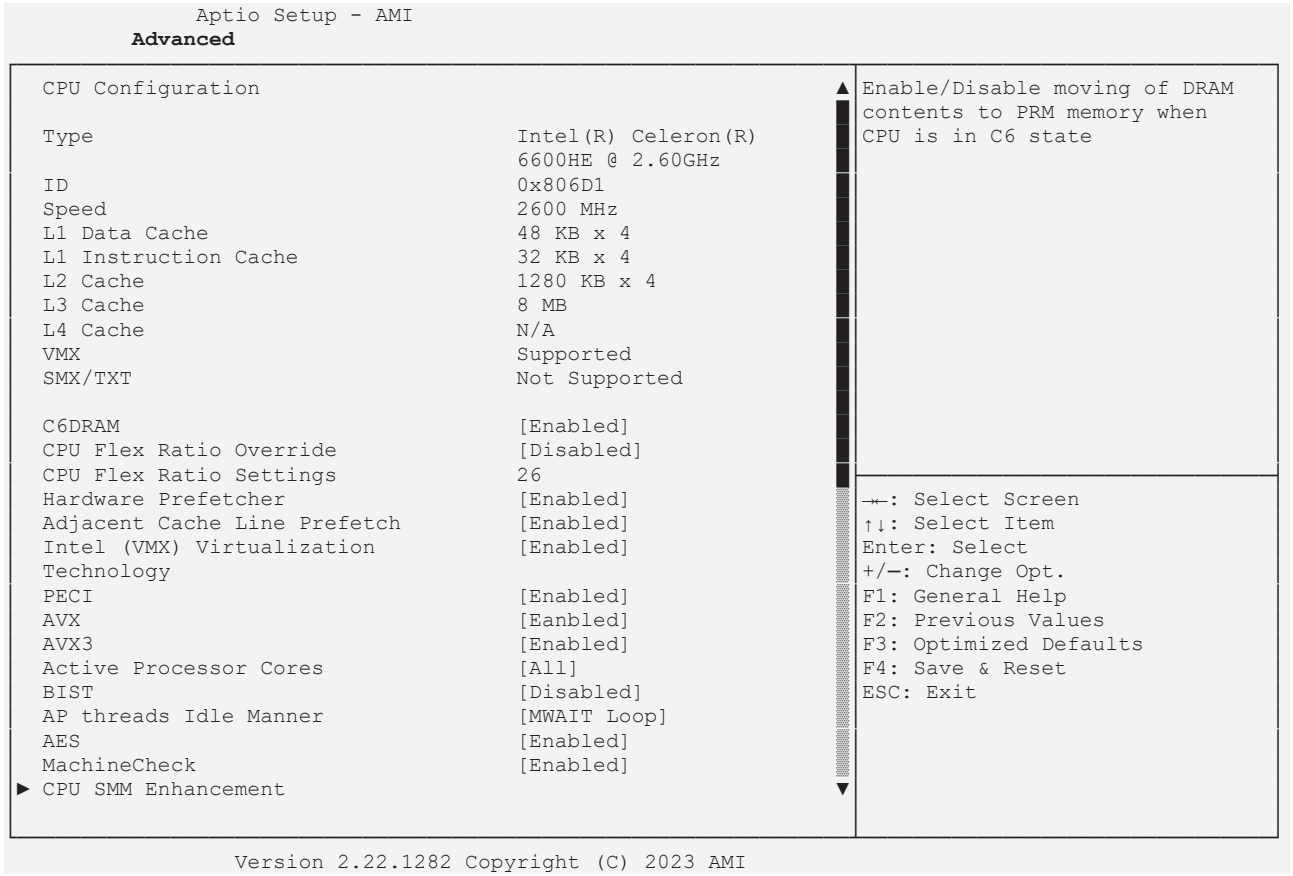
The MAC address is composed of the fixed Beckhoff part 00:01:05 and the board specific part XX:XX:XX.

10.3.1 RC ACPI Settings



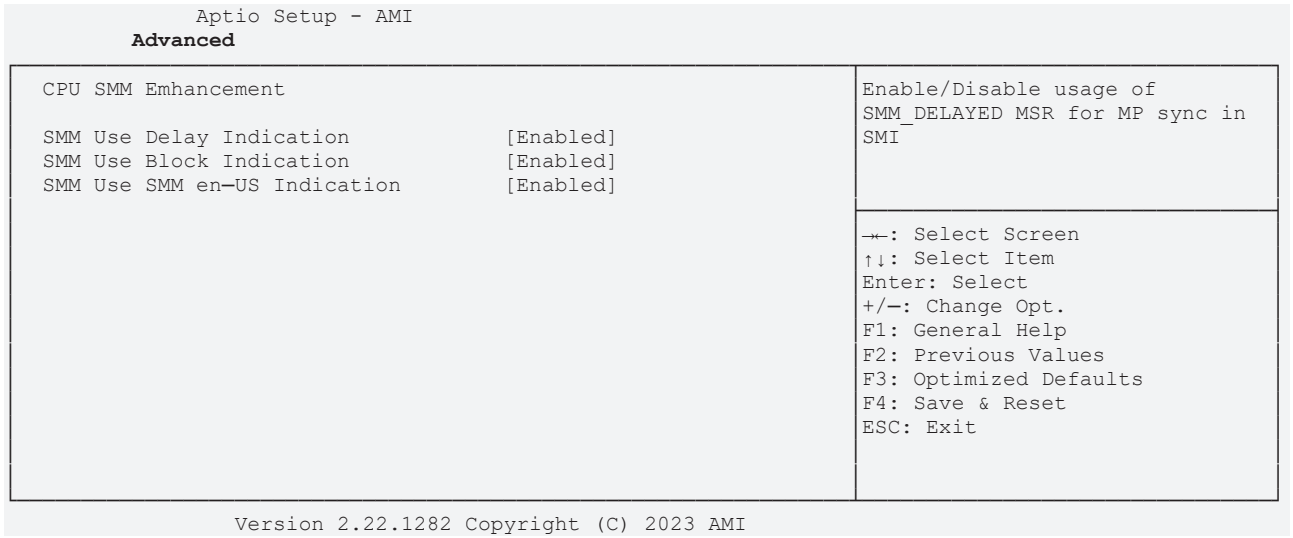
BIOS entry	Options
RC ACPI Settings	
PTID Support	Enabled / Disabled
PECI Access Method	Direct I/O / ACPI
BDAT ACPI Table Support	Disabled / Enabled
ACPI Debug	Disabled / Enabled
MSI enabled	Enabled / Disabled

10.3.2 CPU Configuration



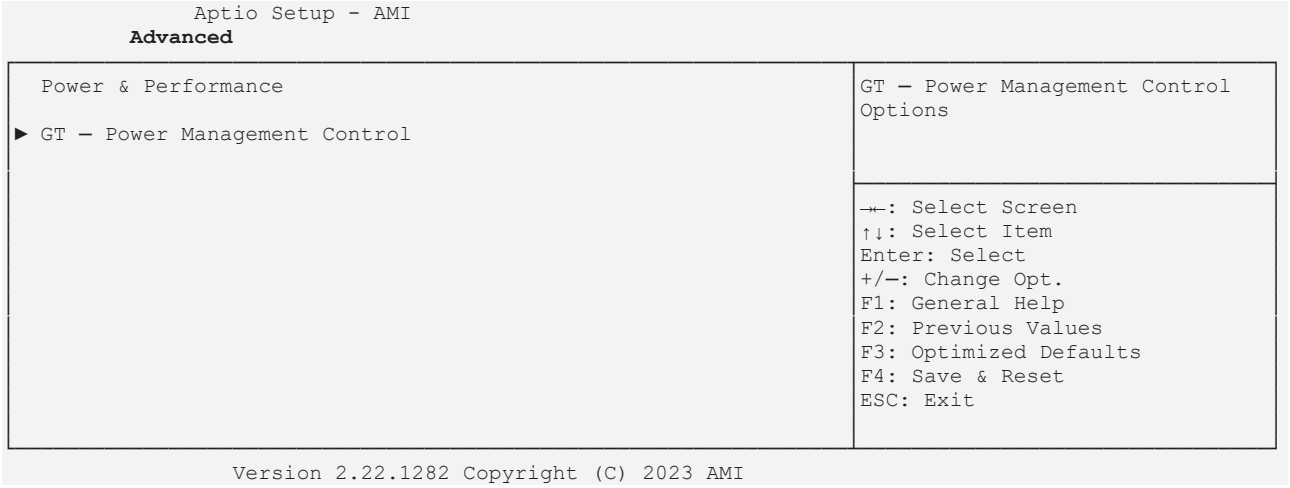
BIOS entry	Options
CPU Configuration	
Type	None
ID	None
Speed	None
L1 Data Cache	None
L1 Instruction Cache	None
L2 Cache	None
L3 Cache	None
L4 Cache	None
VMX	None
SMX/TXT	None
C6DRAM	Enabled / Disabled
CPU Flex Ratio Override	Enabled / Disabled
CPU Flex Ratio Settings	None
Hardware Prefetcher	Enabled / Disabled
Adjacent Cache Line Prefetch	Enabled / Disabled
Intel (VMX)Virtualization Technology	Enabled / Disabled
Hyper - Threading	Disabled / Enabled
PECI	Enabled / Disabled
AVX	Enabled / Disabled
AVX3	Enabled / Disabled
Active Processor Cores	Al l / 1 – 7
Hyper-Threading	Enabled / Disabled
BIST	Disabled / Enabled
AP threads Idle Manner	HALT Loop / MWAIT Loop / Run Loop
AES	Enabled / Disabled
MachineCheck	Enabled / Disabled
MonitorMWait	Enabled / Disabled
Intel Trusted Execution Technology	Disabled / Enabled
Alias Check Request	None
DDR Memory size (MB)	None
Reset Aux Content	No / Yes
►CPU SMM Enhancement	Submenu see: CPU SMM Enhancement [▶ 41]

10.3.2.1 CPU SMM Enhancement



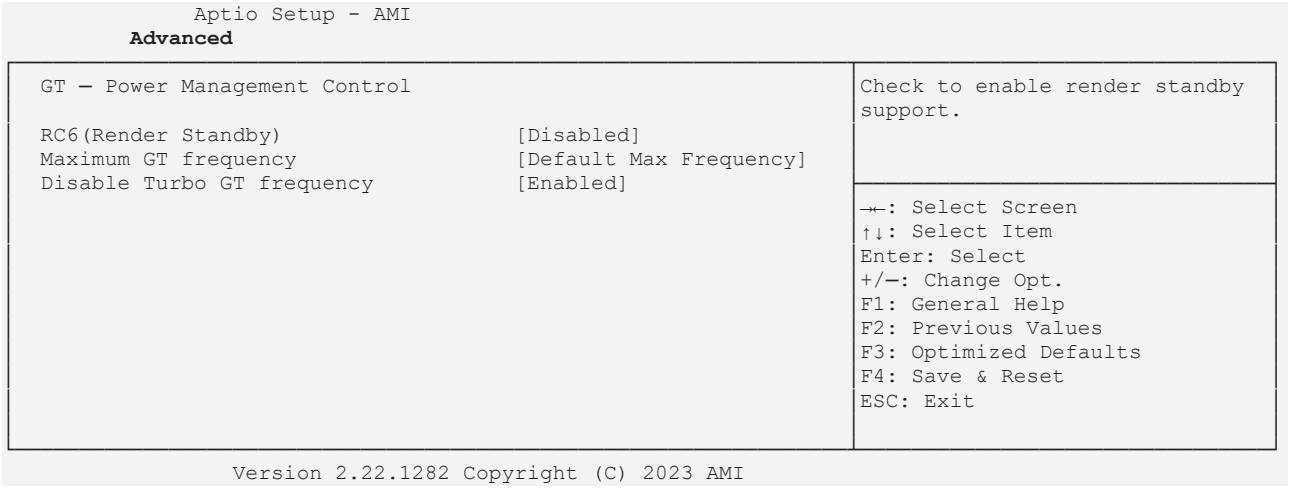
BIOS entry	Options
CPU SMM Enhancement	
SMM Use Delay Indication	Enabled / Disabled
SMM Use Block Indication	Enabled / Disabled
SMM Use SMM en-US Indication	Enabled / Disabled

10.3.3 Power & Performance



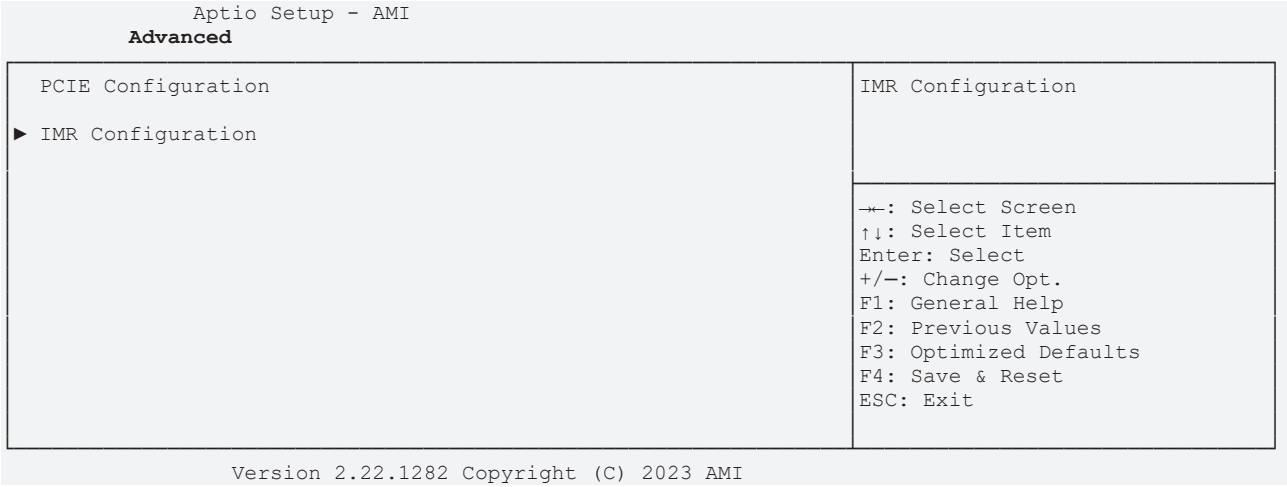
BIOS entry	Options
Power & Performance	
▶GT – Power Management Control	Submenu: see: GT - Power Management Control [▶ 42]

10.3.3.1 GT - Power Management Control



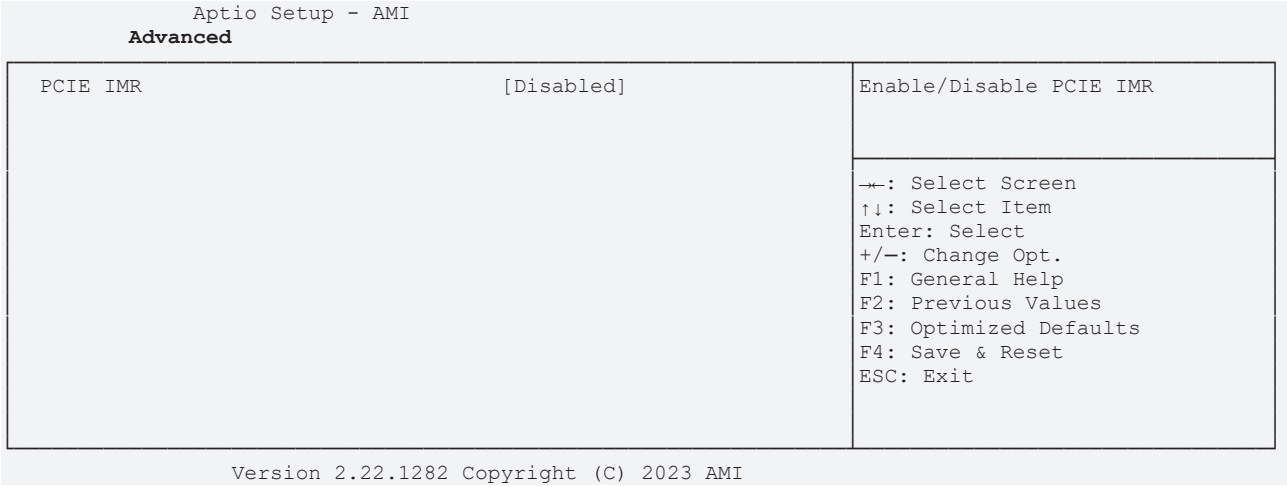
BIOS entry	Options
GT - Power Management Control	
RC6(Render Standby)	Disabled / Enabled
Maximum GT frequency	Default Max Frequency / 100, 150…1100, 1150
Disable Turbo GT frequency	Enabled / Disabled

10.3.4 PCIE Configuration



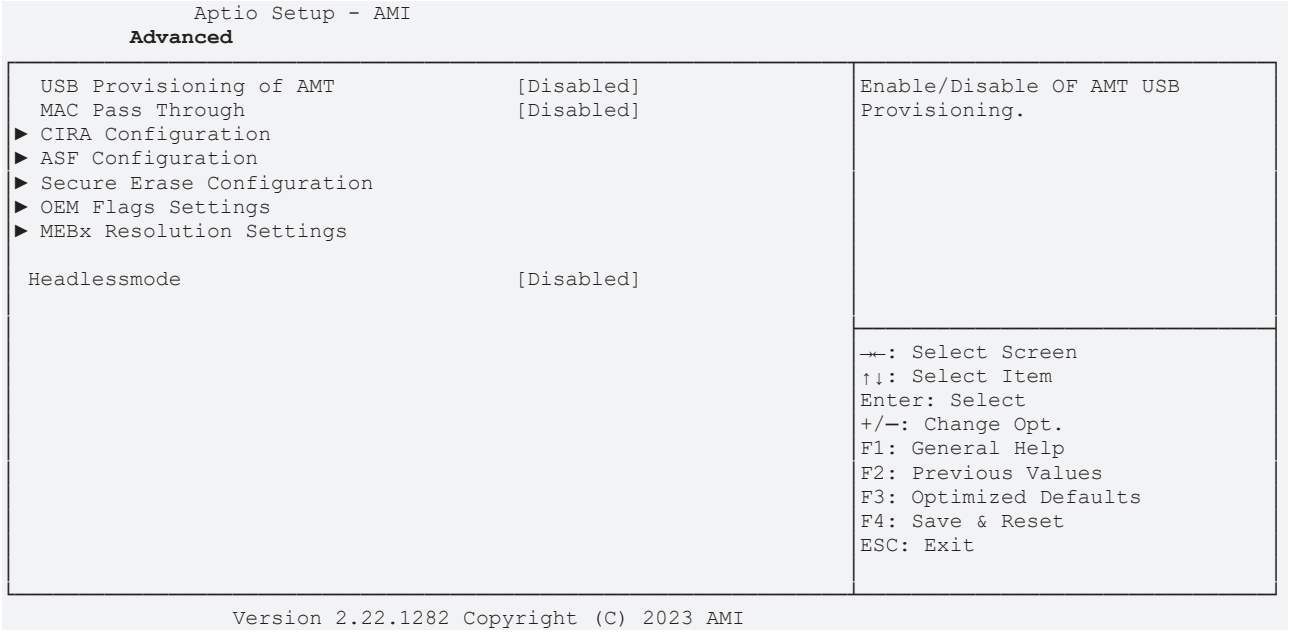
BIOS entry	Options
PCIE Configuration	
▶IMR Configuration	Submenu: see PCIe IMR [▶ 43]

10.3.4.1 PCIe IMR



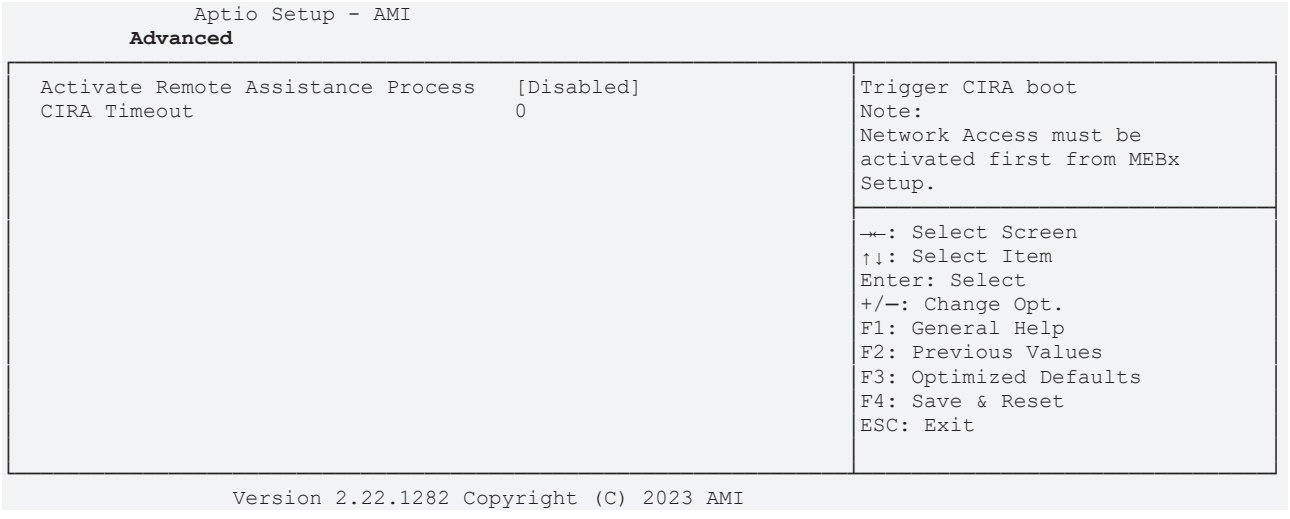
BIOS entry	Options
PCIE IMR	Enabled / Disabled

10.3.5 AMT Configuration



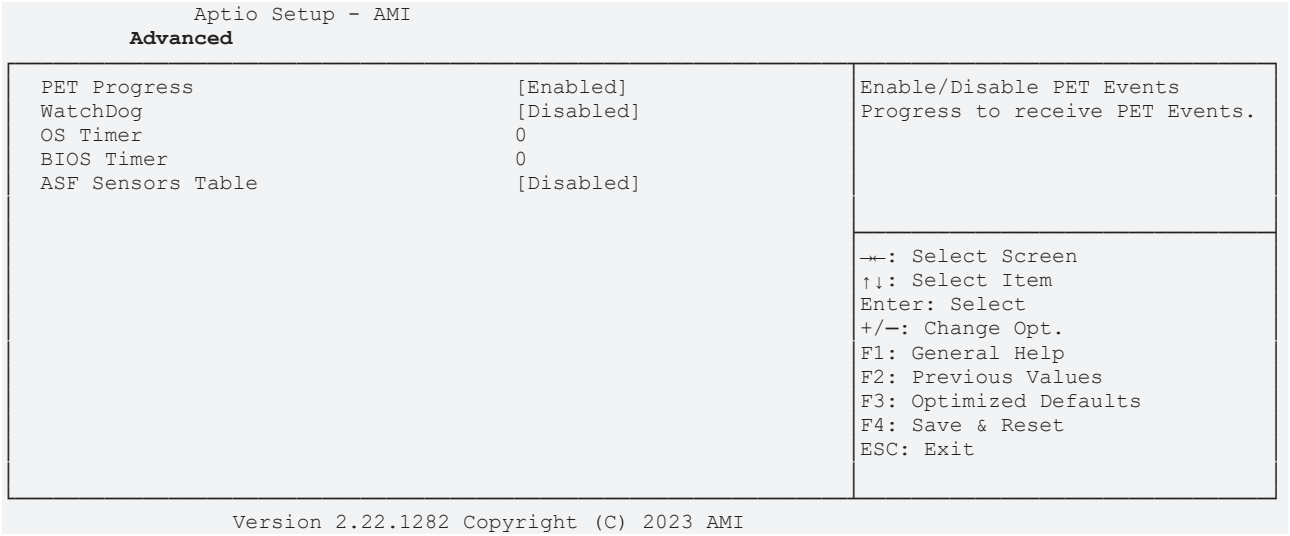
BIOS entry	Options
USB Provisioning of AMT	Disabled / Enabled
MAC Pass Through	Disabled / Enabled
▶CIRA Configuration	Submenu see: CIRA Configuration [▶ 44]
▶ASF Configuration	Submenu see: ASF Configuration [▶ 45]
▶Secure Erase Configuration	Submenu see: Secure Erase Configuration [▶ 45]
▶OEM Flags Settings	Submenu see: OEM Flags Settings [▶ 46]
▶MEBx Resolution Settings	Submenu see: MEBx Resolution Settings [▶ 47]
Headlessmode	Disabled / Enabled

10.3.5.1 CIRA Configuration



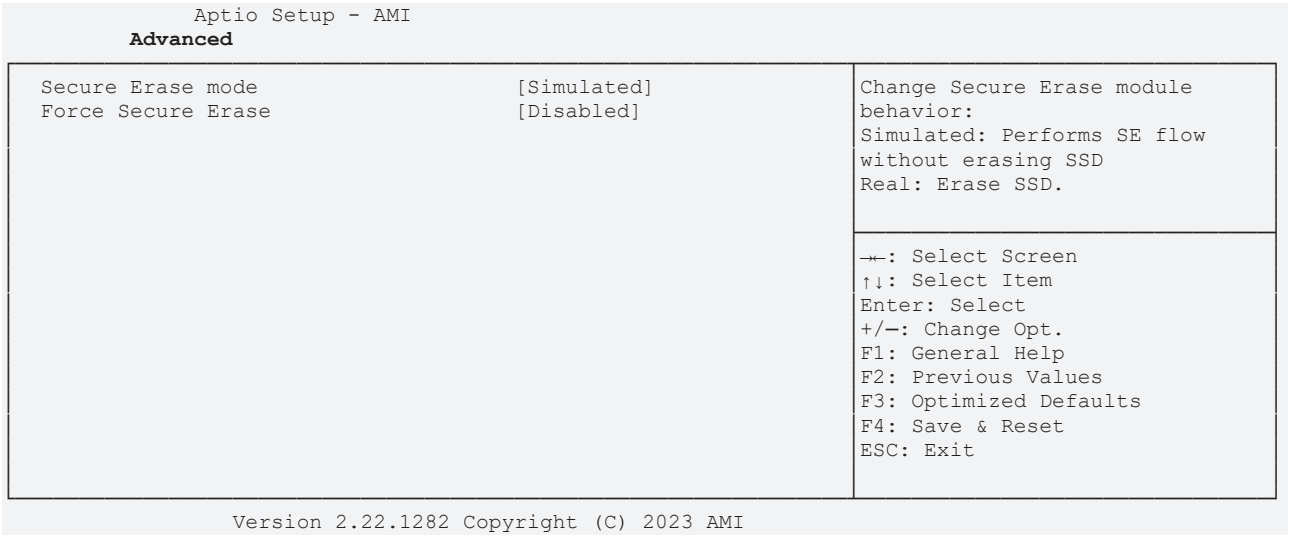
BIOS entry	Options
Activate Remote Assistance Process	Disabled / Enabled
CIRA Timeout	None

10.3.5.2 ASF Configuration



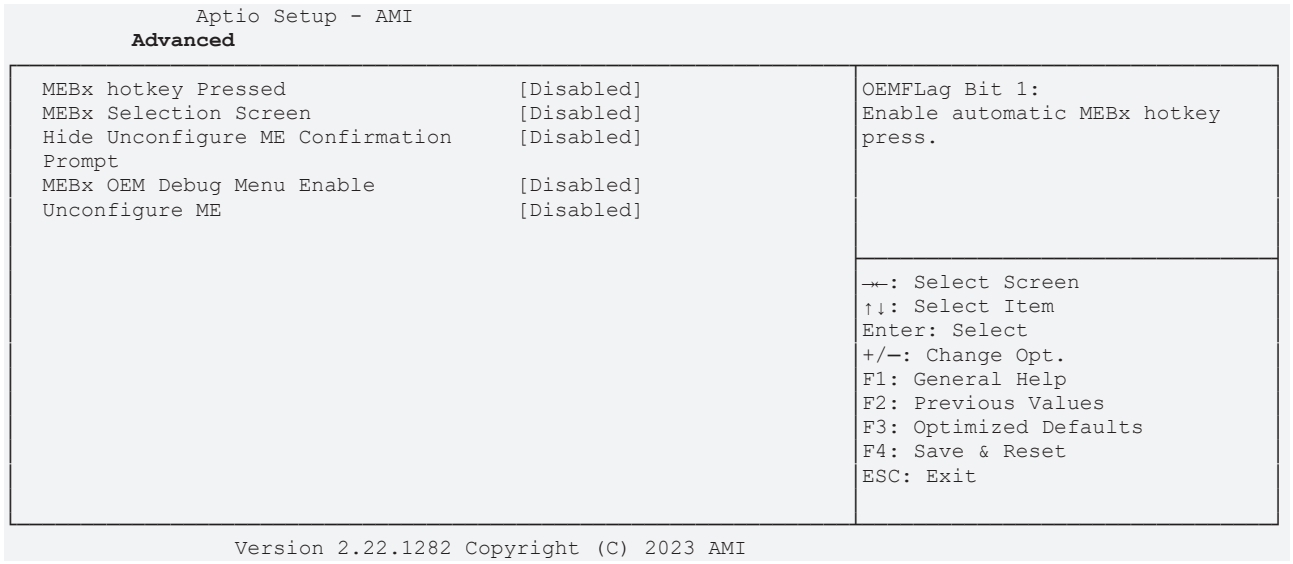
BIOS entry	Options
PET Progress	Enabled / Disabled
WatchDog	Disabled / Enabled
OS Timer	None
BIOS Timer	None
ASF Sensors Table	Disabled / Enabled

10.3.5.3 Secure Erase Configuration



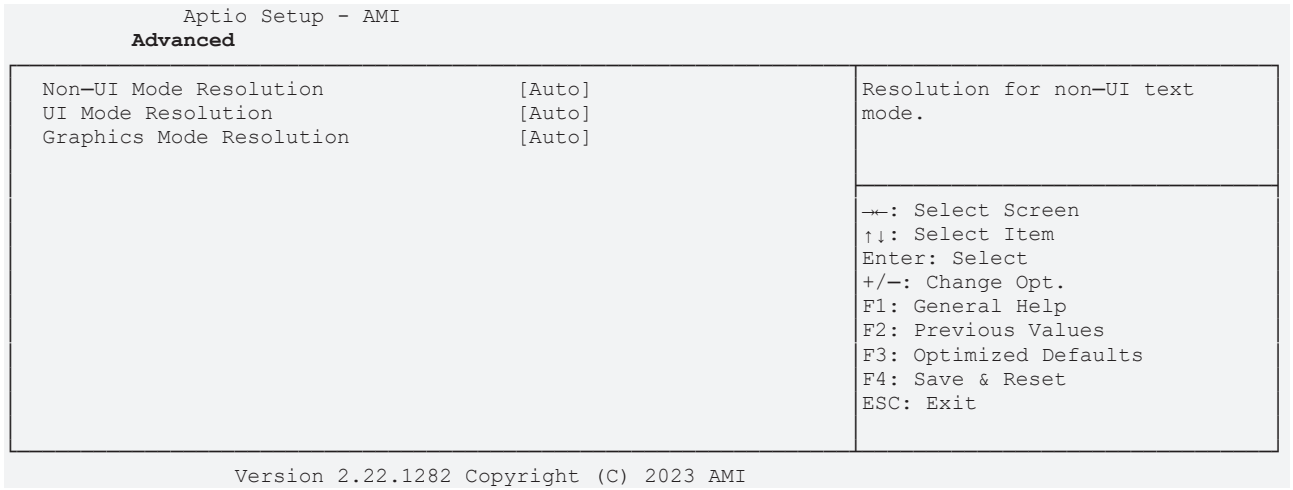
BIOS entry	Options
Secure Erase mode	Simulated / Real
Force Secure Erase	Disabled / Enabled

10.3.5.4 OEM Flags Settings



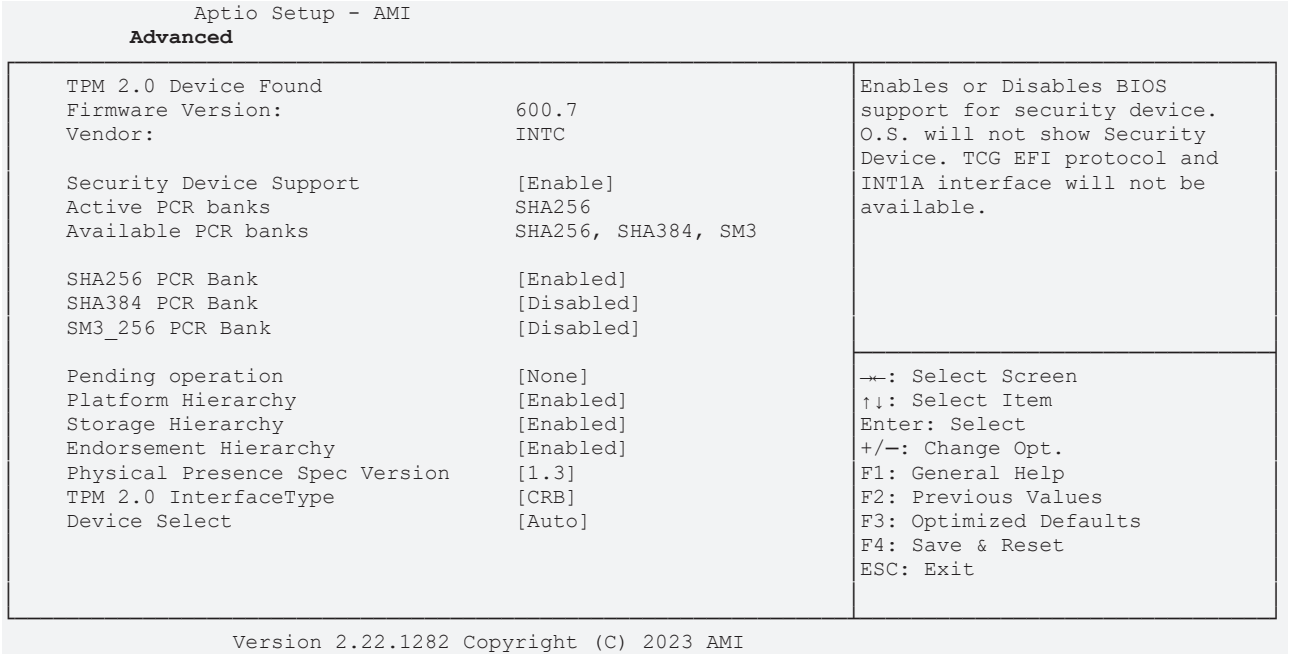
BIOS entry	Options
MBEx hotkey Pressed	Disabled / Enabled
MBEx Selection Screen	Disabled / Enabled
Hide Unconfigure ME Confirmation Prompt	Disabled / Enabled
MBEx OEM Debug Menu Enable	Disabled / Enabled
Unconfigure ME	Disabled / Enabled

10.3.5.5 MEBx Resolution Settings



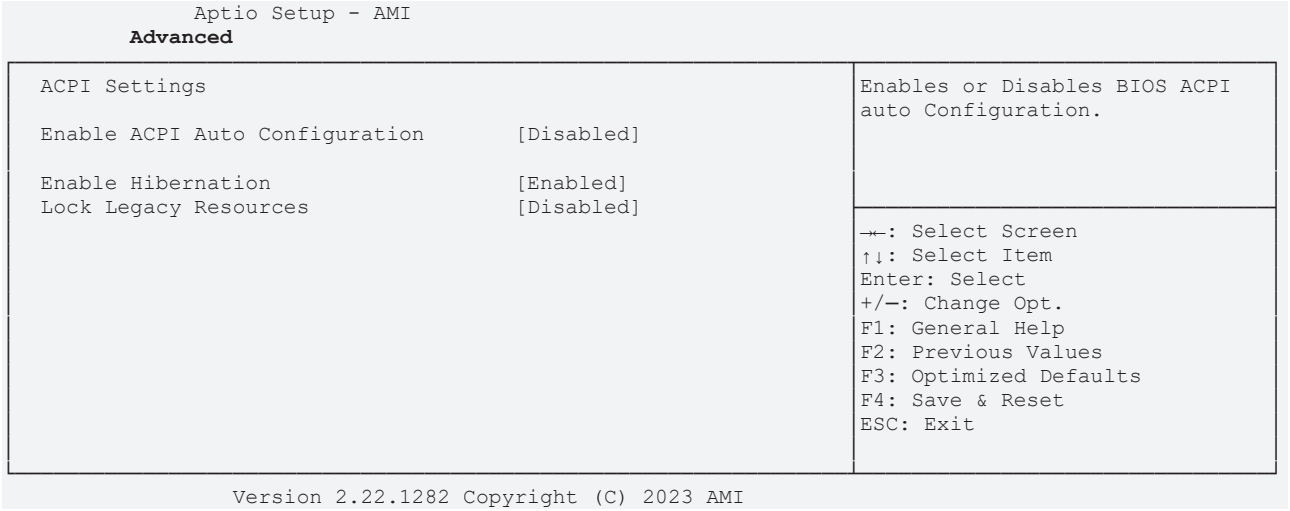
BIOS entry	Options
Non-UI Resolution	Auto / 80x25 / 100x31
UI Mode Resolution	Auto / 80x25 / 100x31
Graphics Mode Resolution	Auto / 640x480 / 800x600 / 1024x768

10.3.6 Trusted Computing



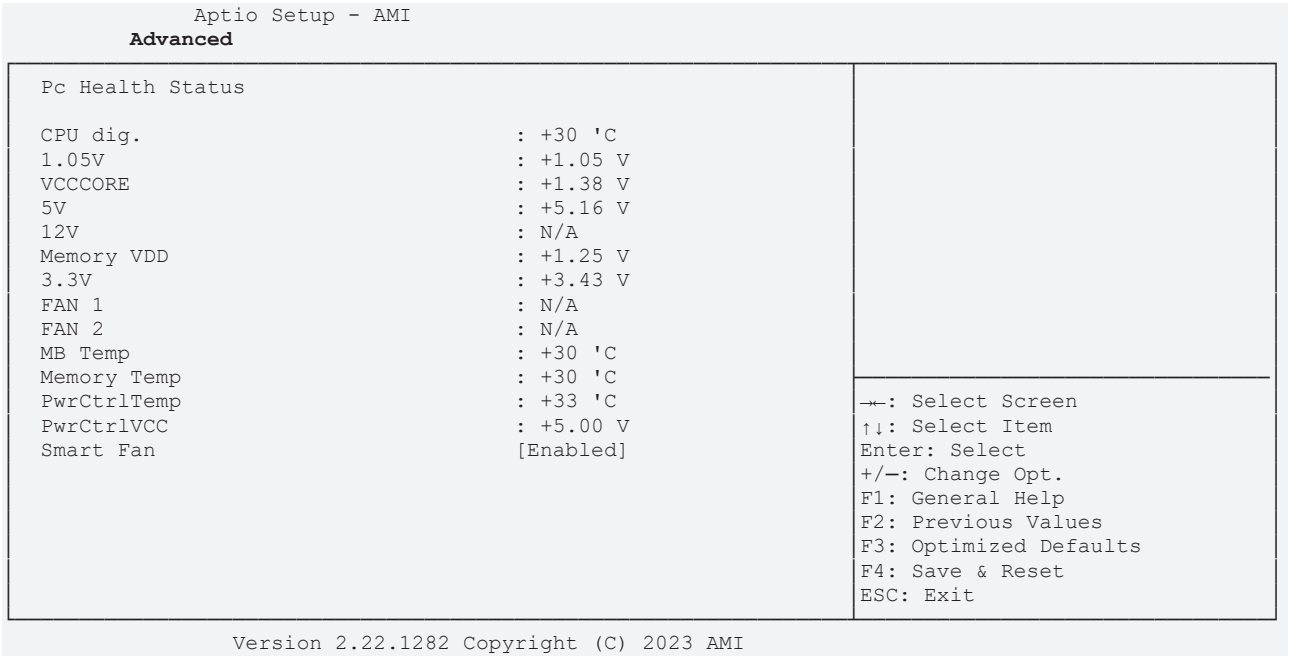
BIOS entry	Options
TPM 2.0 Device Found	
Firmware version:	600.7
Vendor:	INTC
Security Device Support	Enable / Disable
Active PCR banks	None
Available PCR banks	None
SHA256 PCR Bank	Enabled / Disabled
SHA384 PCR Bank	Disabled / Enabled
SM3_256 PCR Bank	Disabled / Enabled
Pending operation	None / TPM clear
Platform Hierarchy	Enabled / Disabled
Storage Hierarchy	Enabled / Disabled
Endorsement Hierarchy	Enabled / Disabled
Physical Presence Spec Version	1.3 / 1.2
TPM 2.0 InterfaceType	None
Device Select	Auto / TPM 1.2 / TPM 2.0

10.3.7 ACPI Settings



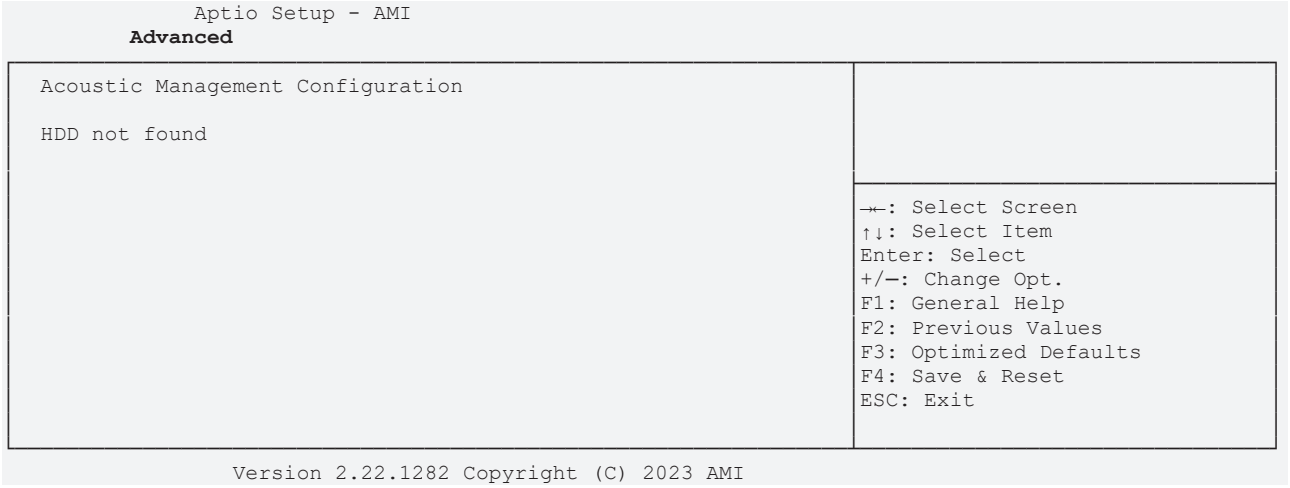
BIOS entry	Options
ACPI Settings	
Enable ACPI Auto Configuration	Disabled / Enabled
Enable Hibernation	Enabled / Disabled
Lock Legacy Resources	Disabled / Enabled

10.3.8 Hardware Monitor



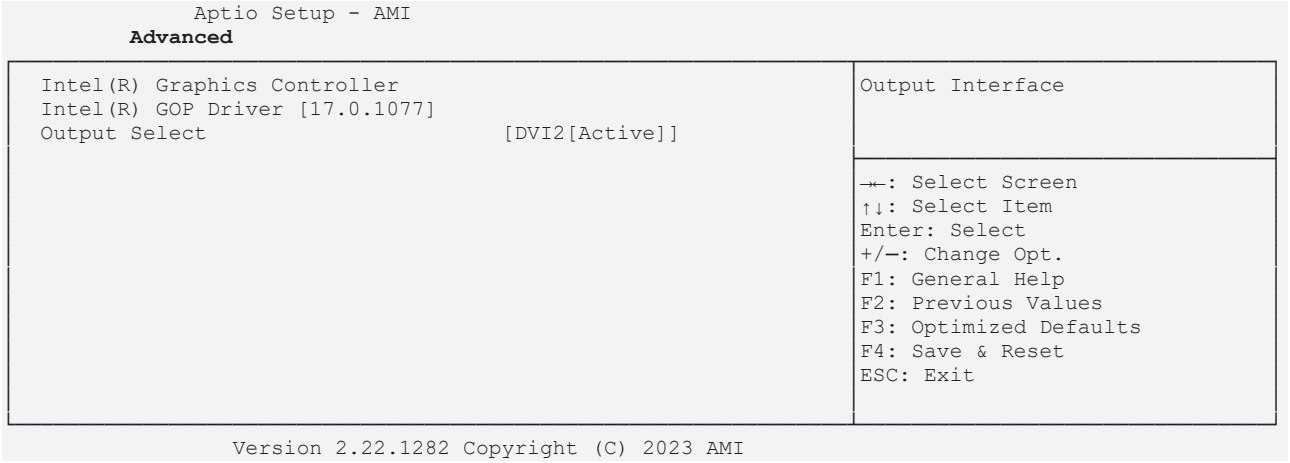
BIOS entry	Options
PC Health Status	None
Smart Fan	Enabled / Disabled

10.3.9 Acoustic Management Configuration



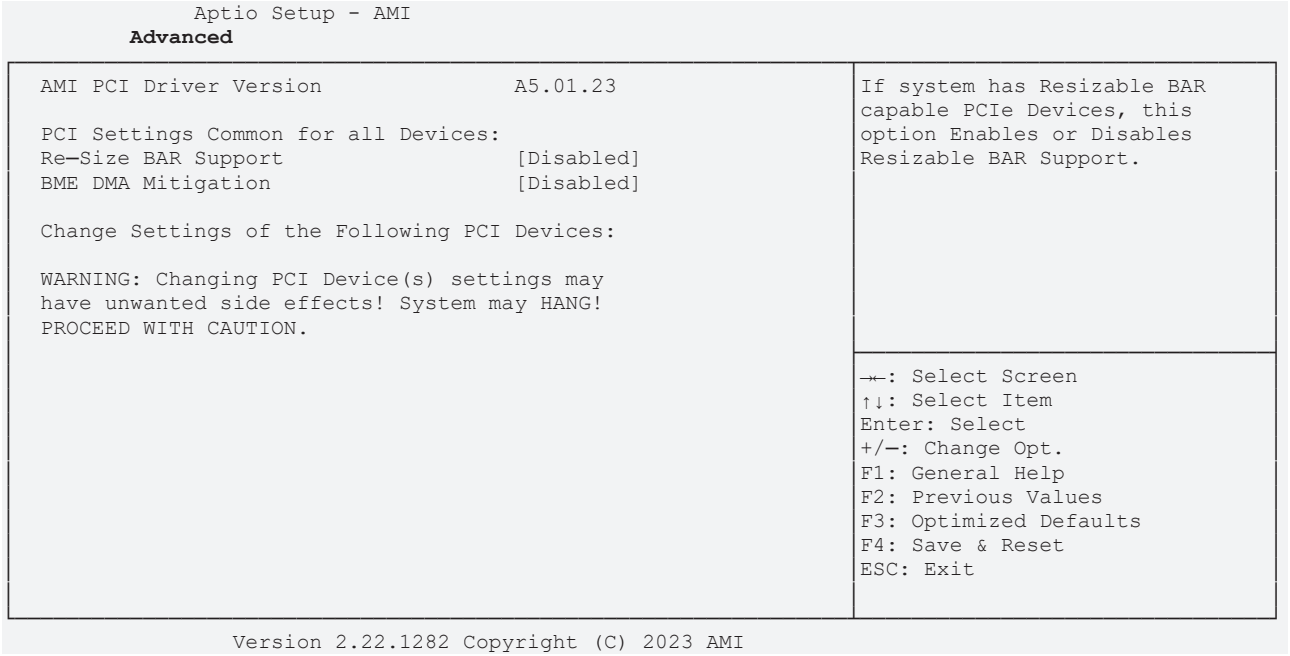
BIOS entry	Options
Acoustic Management Configuration	
HDD not found	

10.3.10 AMI Graphic Output Protocol Policy



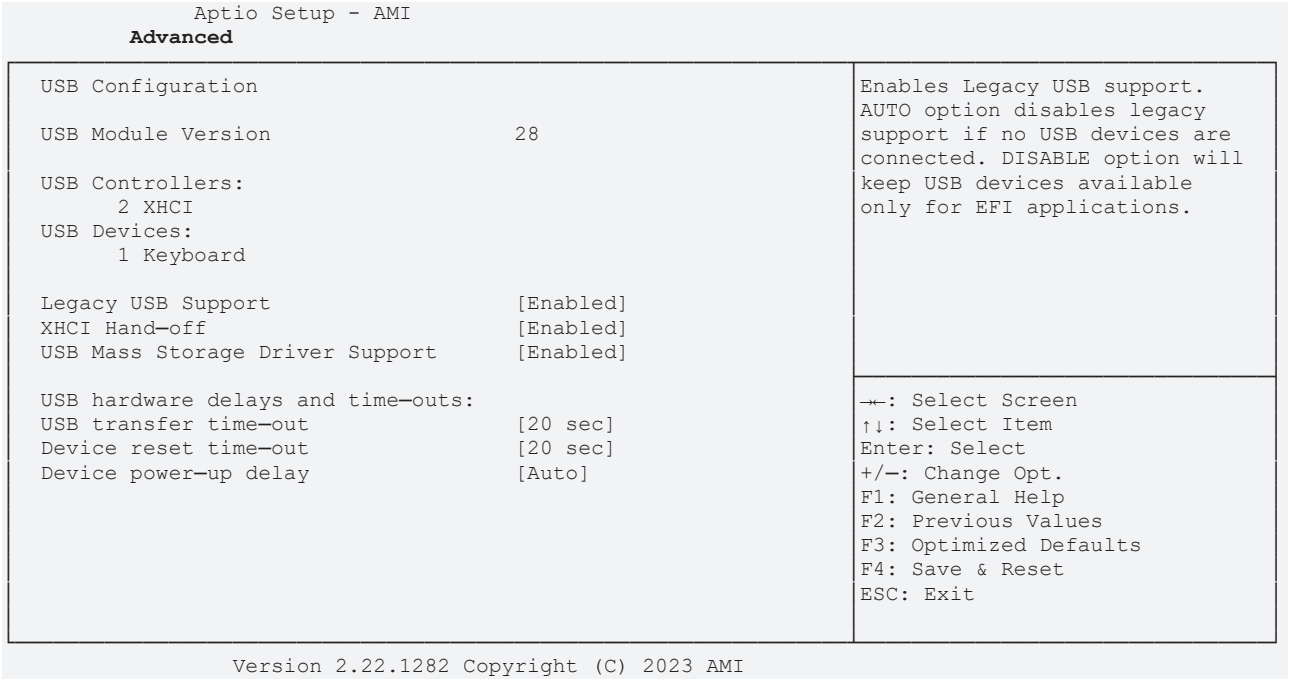
BIOS entry	Options
Intel(R) Graphics Controller Intel(R) GOP Driver [17.0.1077]	
Output Select	None

10.3.11 PCI Subsystem Settings



BIOS entry	Options
AMI PCI Driver Version: A5.01.23	
PCI Settings Common for all Devices:	
Re-Size BAR Support	Disabled / Enabled
BME DMA Mitigation	Disabled / Enabled
Change Settings of the Following PCI Devices:	
WARNING: Changing PCI Device(s) settings may have unwanted side effects! System may HANG! PROCEED WITH CAUTION.	

10.3.12 USB Configuration

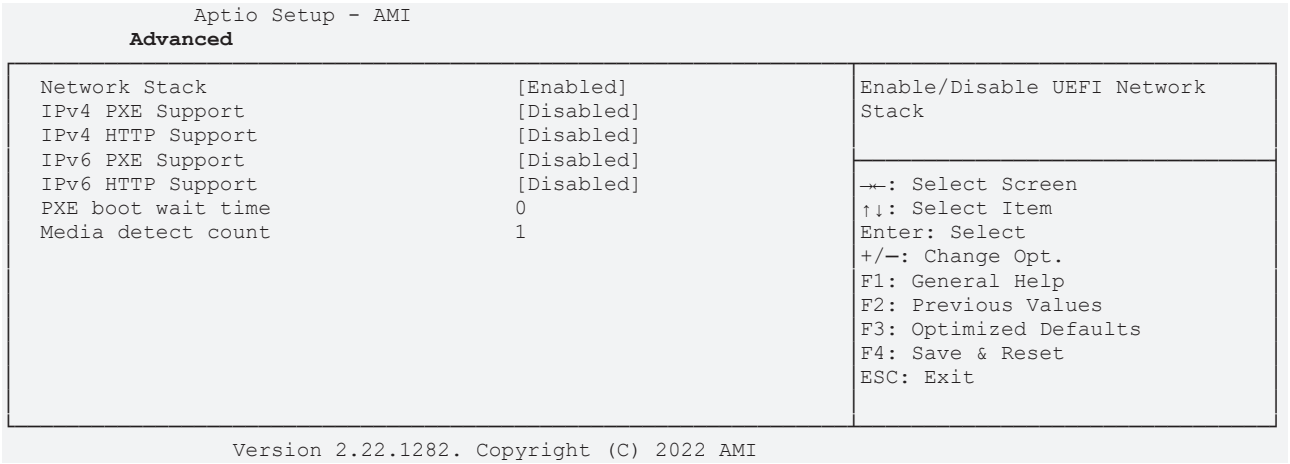


BIOS entry	Options
USB Configuration	
USB Module Version	None
USB Controllers: 2 XHCI	None
USB Devices: 1 Keyboard	None
Legacy USB Support	Enabled / Disabled
XHCI Hand-off	Enabled / Disabled
USB Mass Storage Driver Support	Enabled / Disabled
USB hardware delays and time-outs:	None
USB transfer time-out	20 sec (1, 5, 10, 20 sec)
Device reset time-out	20 sec (10, 20, 30, 40 sec)
Device power-up delay	Auto / Manual

10.3.13 Network Stack Configuration

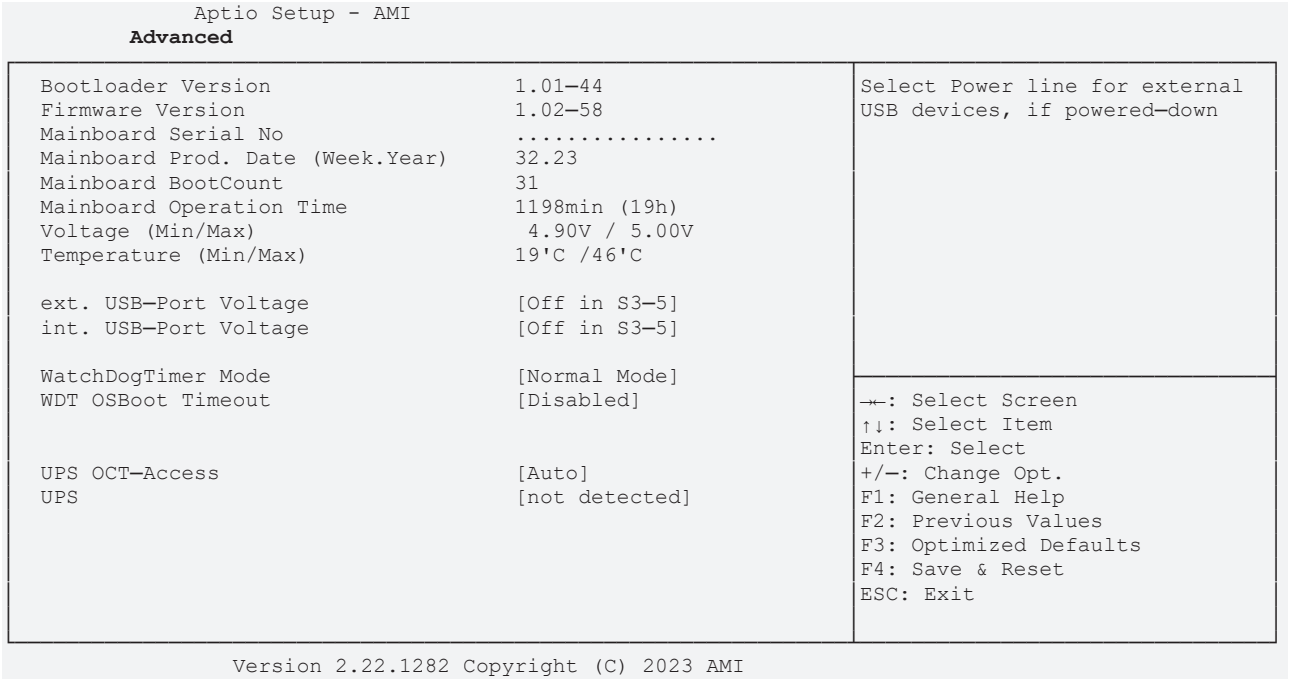
BIOS entry	Options
Network Stack	Disabled / Enabled

10.3.14 Network Stack Configuration enabled



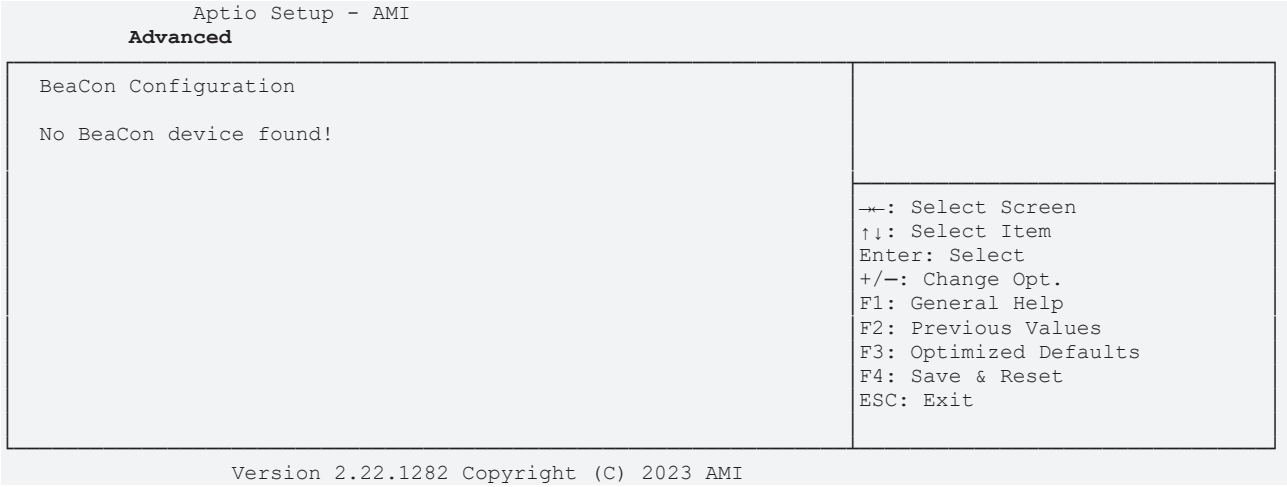
BIOS entry	Options
Network Stack	Enabled
Ipv4 PXE Support	Disabled / Enabled
Ipv4 HTTP Support	Disabled / Enabled
Ipv6 PXE Support	Disabled / Enabled
Ipv6 HTTP Support	Disabled / Enabled
PXE boot wait time	None
Media detect count	None

10.3.15 Power Controller Options



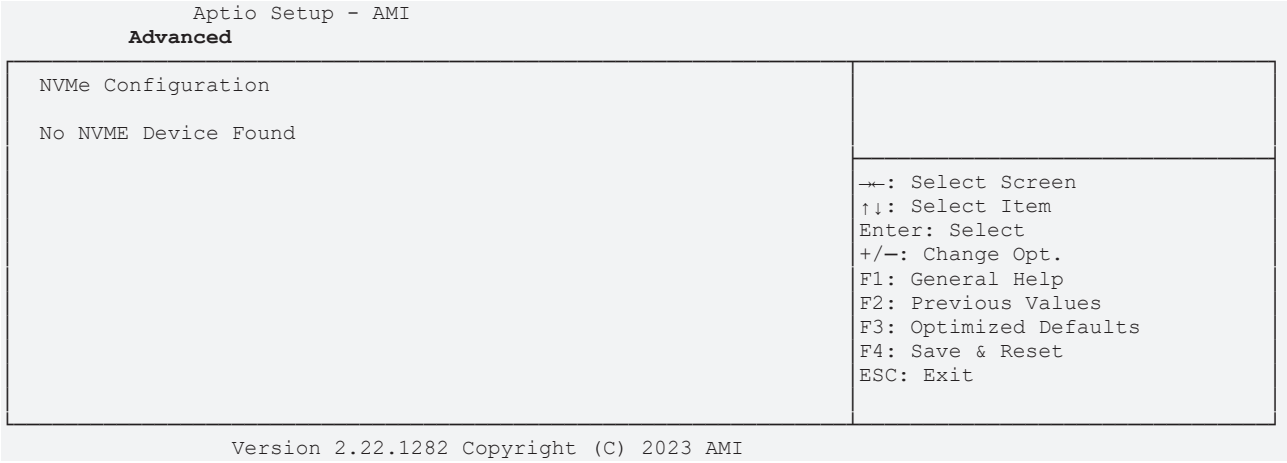
BIOS entry	Options
Bootloader version	None
Firmware version	None
Mainboard Serial No	None
Mainboard Prod. Date (Week.Year)	None
Mainboard BootCount	None
Mainboard Operation Time	None
Voltage (Min/Max)	None
Temperature (Min/Max)	None
ext. USB-Port Voltage	Off in S3-5 / by SVCC
int. USB-Port Voltage	Off in S3-5 / by SVCC
WatchDogTimer Mode	Normal Mode / Compatibility Mode
WDT OSBoot Timeout	Disabled / 45…255 Seconds (in steps +15)
UPS OCT-Access	Auto / Off
UPS	None

10.3.16 BeaCon Configuration



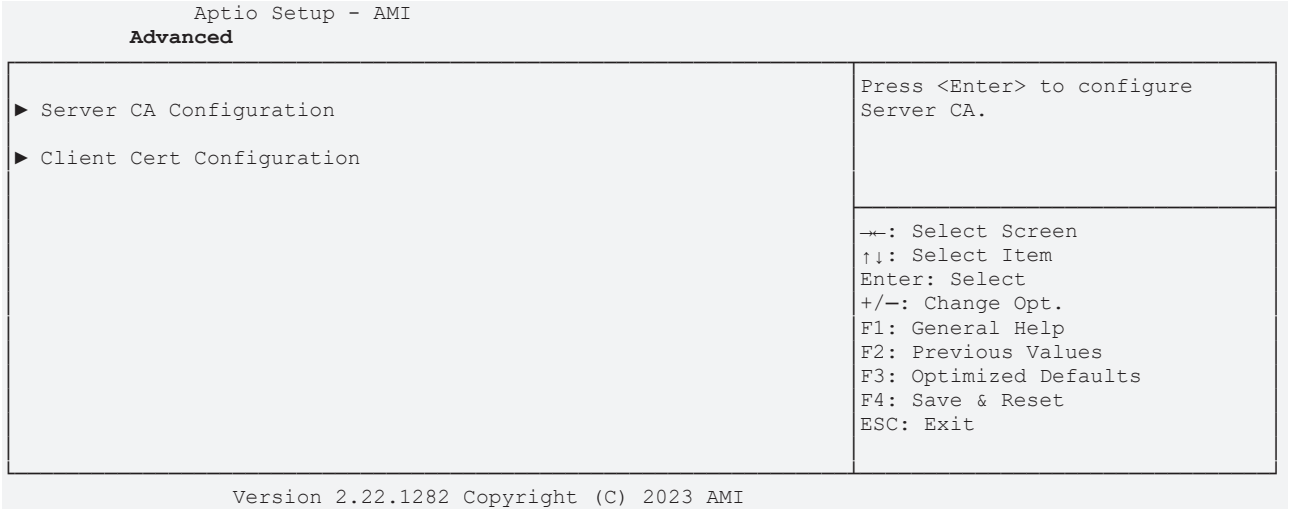
BIOS entry	Options
BeaCon Configuration	
No BeaCon device found	

10.3.17 NVMe Configuration



BIOS entry	Options
NVMe Configuration	
No NVME Device Found	None

10.3.18 TLs Auth Configuration

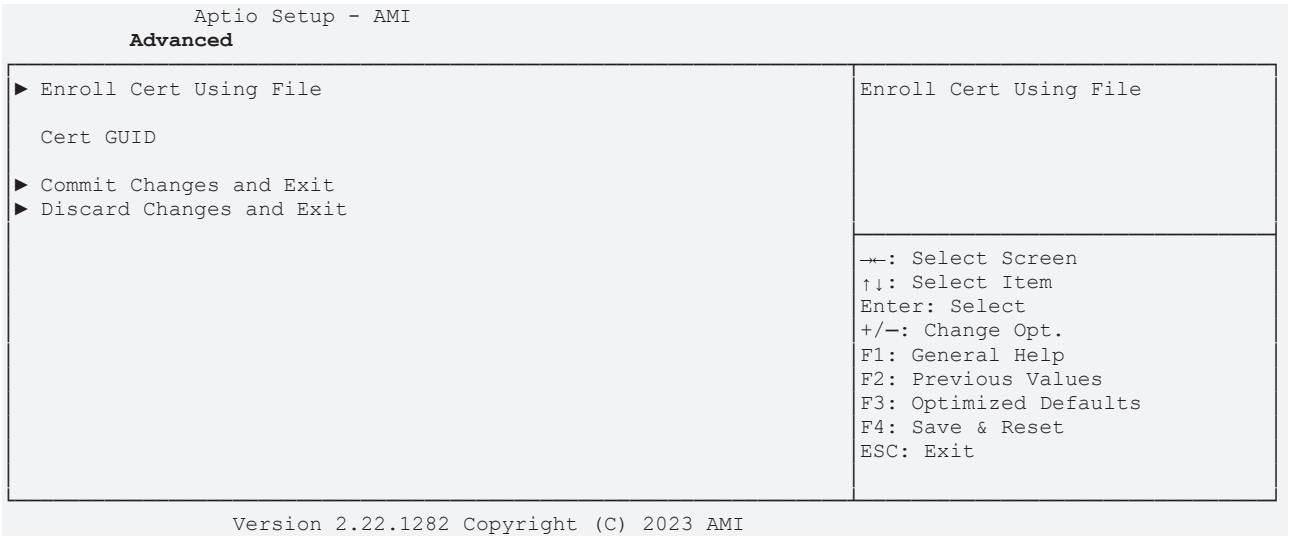


BIOS entry	Options
►Server CA Configuration	
►Client Cert Configuration	

10.3.18.1 Server CA Configuration

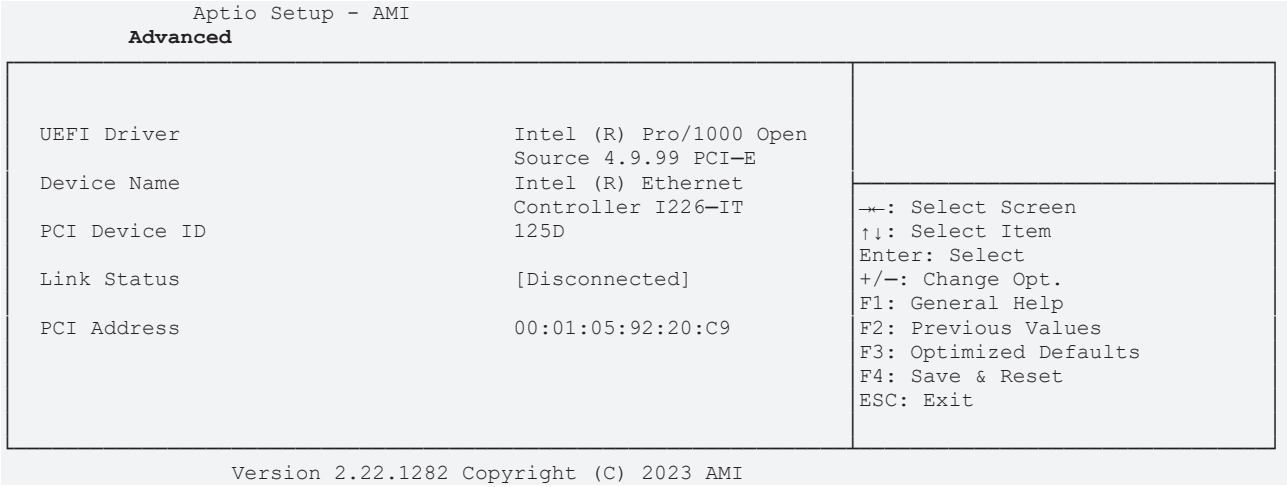
BIOS entry	Options
▶Enroll Cert	Submenu see: Enroll Cert [▶ 57]
▶Delete Cert	None

10.3.18.1.1 Enroll Cert



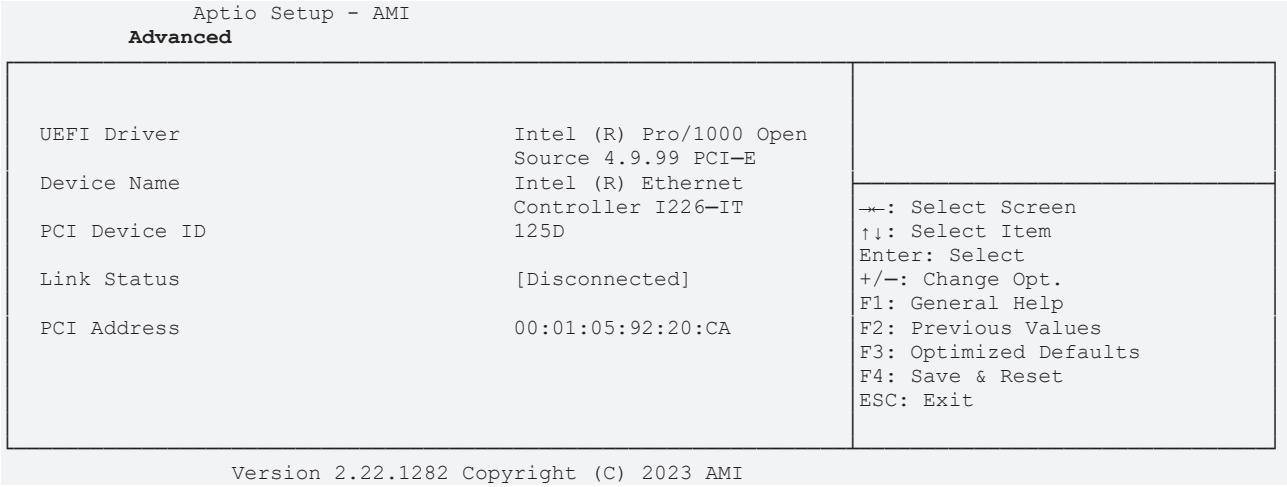
BIOS entry	Options
▶Enroll Cert Using File	None
Cert GUID	None
▶Commit Changes and Exit	None
▶Discard Changes and Exit	None

10.3.19 Intel Ethernet Controller I226-IT



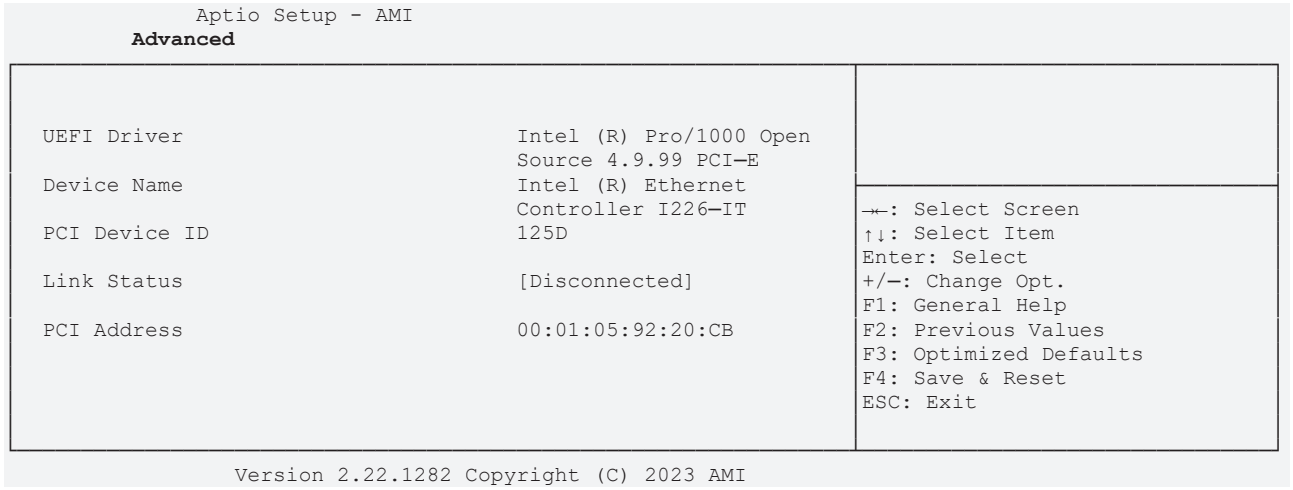
BIOS entry	Options
UEFI Driver	None
Device Name	None
PCI Device ID	None
Link Status	None
PCI Address	None

10.3.20 Intel Ethernet Controller I226-IT



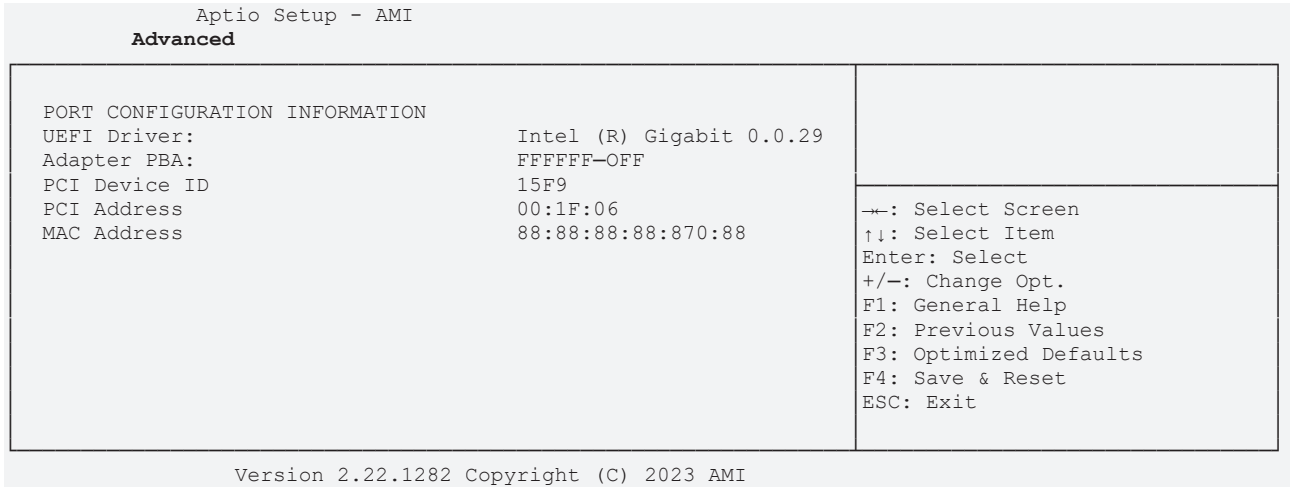
BIOS entry	Options
UEFI Driver	None
Device Name	None
PCI Device ID	None
Link Status	None
PCI Address	None

10.3.21 Intel Ethernet Controller I226-IT



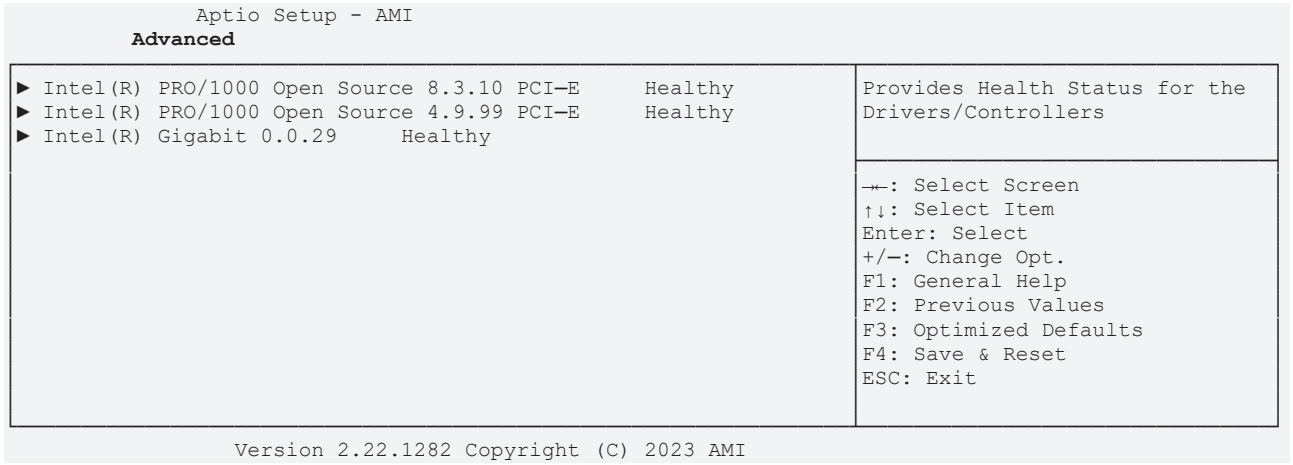
BIOS entry	Options
UEFI Driver	None
Device Name	None
PCI Device ID	None
Link Status	None
PCI Address	None

10.3.22 Intel Ethernet Connection I219-LM



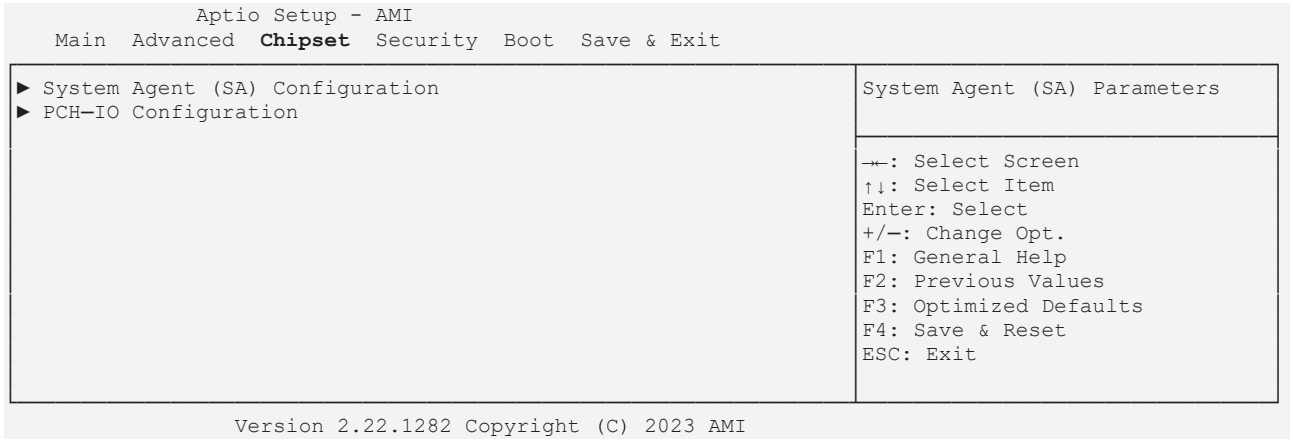
BIOS entry	Options
UEFI Driver	None
Device Name	None
PCI Device ID	None
Link Status	None
PCI Address	None

10.3.23 Driver Health



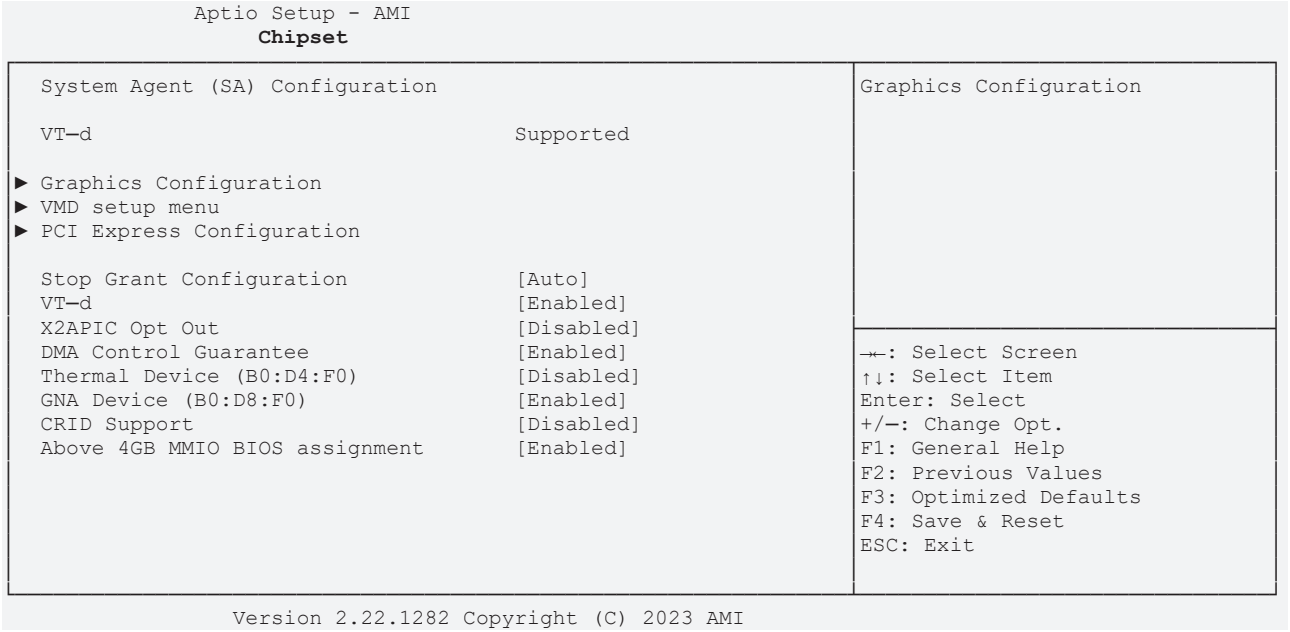
BIOS entry	Options
►Intel(R) PRO/1000 Open Source 8.3.10 PCI-E	None
►Intel(R) PRO/1000 Open Source 4.9.99 PCI-E	None
►Intel(R) Gigabit 0.0.29	None

10.4 Chipset CB6472



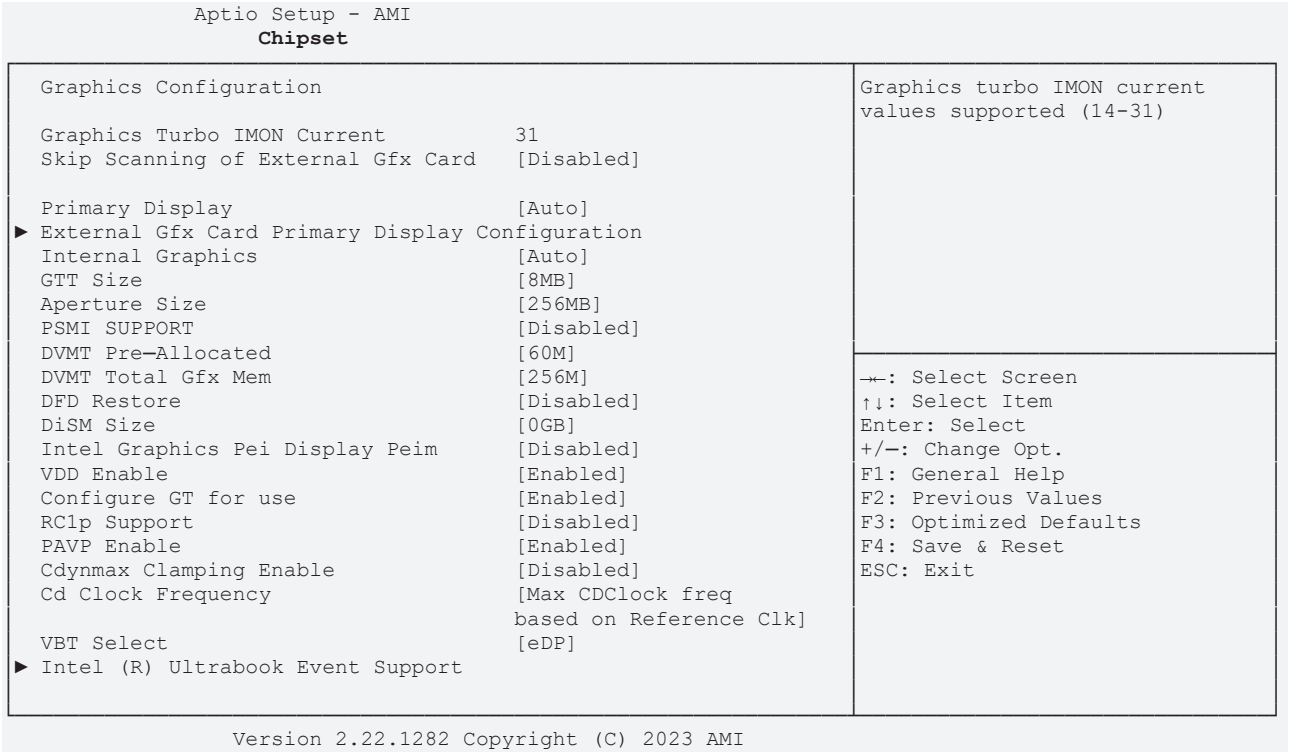
BIOS entry	Options
►System Agent (SA) Configuration	Submenu see: System Agent (SA) Configuration [▶ 64]
►PCH-IO Configuration	Submenu see: PCI Express Configuration [▶ 68]

10.4.1 System Agent (SA) Configuration



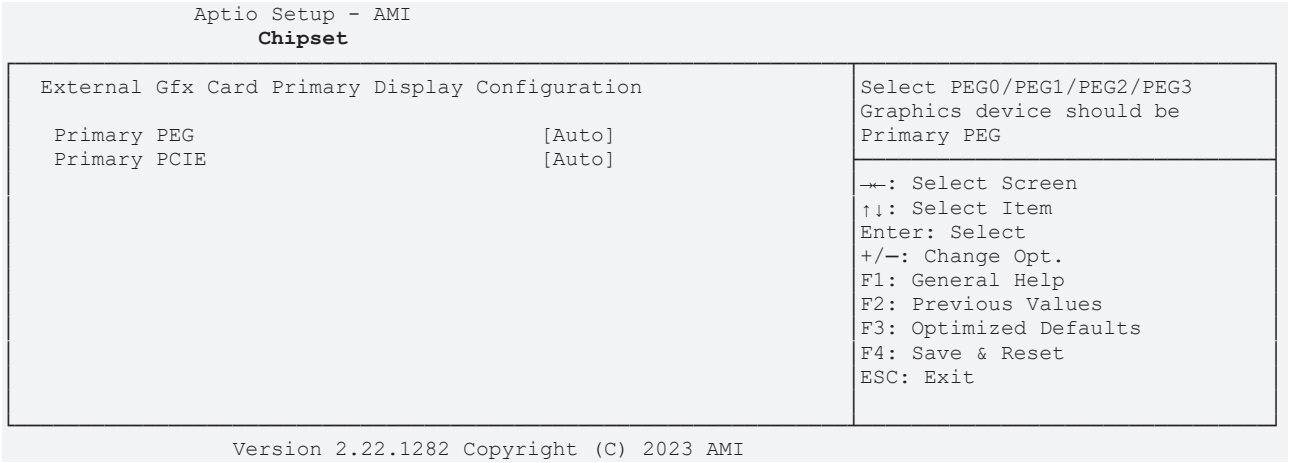
BIOS entry	Options
System Agent (SA) Configuration	
VT-d	None
►Graphics Configuration	Submenu see: Graphics Configuration [▶ 65]
►VMD setup menu	Submenu see: VMD setup menu enabled [▶ 67]
►PCI Express Configuration	Submenu see: PCI Express Configuration [▶ 68]
Stop Grant Configuration	Auto / Manual
VT-d	Enabled / Disabled
X2APIC Opt Out	Disabled / Enabled
DMA Control Guarantee	Enabled / Disabled
Thermal Device (B0:D4:F0)	Disabled / Enabled
GNA Device (B0:D8:F0)	Enabled / Disabled
CRID Support	Disabled / Enabled
Above 4GB MMIO BIOS assignment	Enabled / Disabled

10.4.1.1 Graphics Configuration



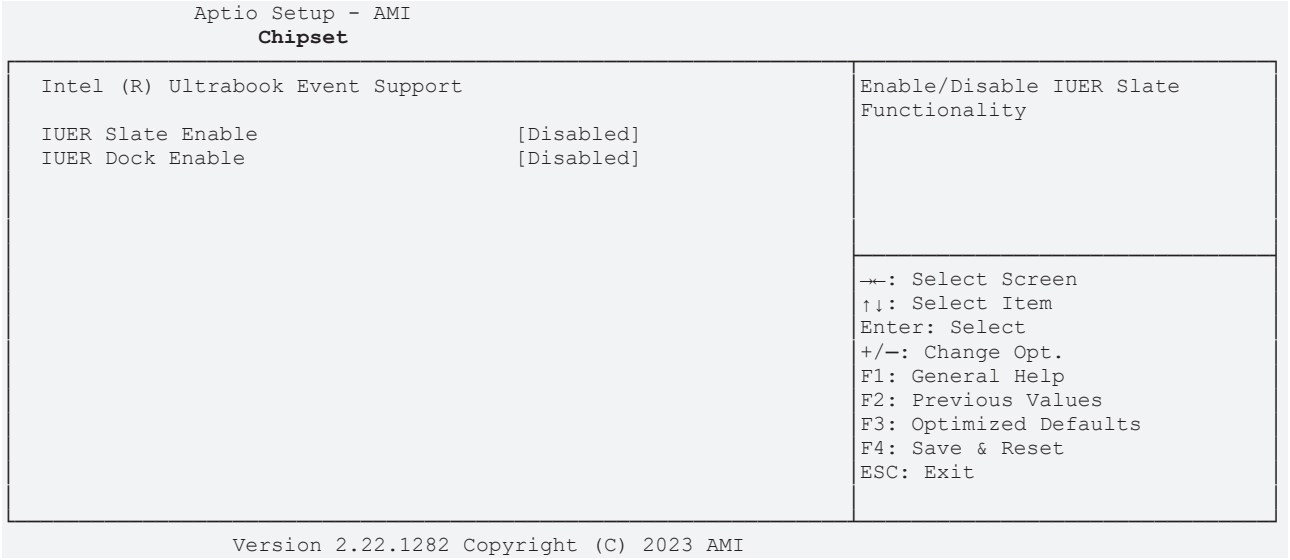
BIOS entry	Options
Graphics Configuration	
Graphics Turbo IMON Current	None
Skip Scanning of External Gfx Card	Disabled / Enabled
Primary Display	Auto / IGFX / PEG Slot / PCH PCI / HG
►External Gfx Card Primary Display Configuration	Submenu see: External Gfx Card Primary Display Configuration [▶ 66]
Internal Graphics	Auto / Disabled / Enabled
GTT Size	2 / 4 / 8 MB
Aperture Size	128 / 256 / 512 / 1024 MB
PSMI SUPPORT	Disabled / Enabled
DVMT Pre-Allocated	0M, 32M…64M, 96M, 128M, 160M
DVMT Total Gfx Mem	128M / 256M / MAX
DFD Restore	Disabled / Enabled
DiSM Size	0 - 7 GB
Intel Graphics Pei Display Peim	Disabled / Enabled
VDD Enable	Enabled / Disabled
Configure GT for use	Enabled / Disabled
RC1p Support	Disabled / Enabled
PAVP Enable	Enabled / Disabled
Cdynmax Clamping Enable	Enabled / Disabled
Cd Clock Frequency	192 / 307.2 / 326.4 / 556.8 / 652.8 Mhz Max CdClock freq based on Reference Clk
VBT Select	eDP / MIPI / eDP & HDMI / eDP & HDMI for TGLH
►Intel (R) Ultrabook Event Support	Submenu see: Intel Ultrabook Event Support [▶ 66]

10.4.1.1.1 External Gfx Card Primary Display Configuration



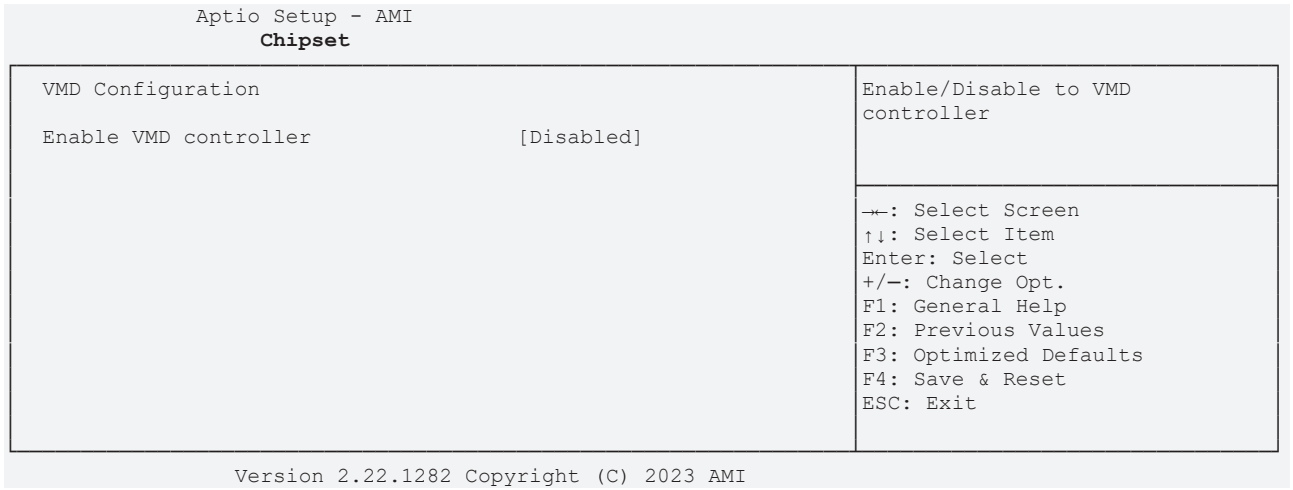
BIOS entry	Options
External Gfx Card Primary Display Configuration	
Primary PEG	Auto / PEG11 / PEG 12
Primary PCIE	Auto / PCI1 - PCIE19

10.4.1.1.2 Intel Ultrabook Event Support



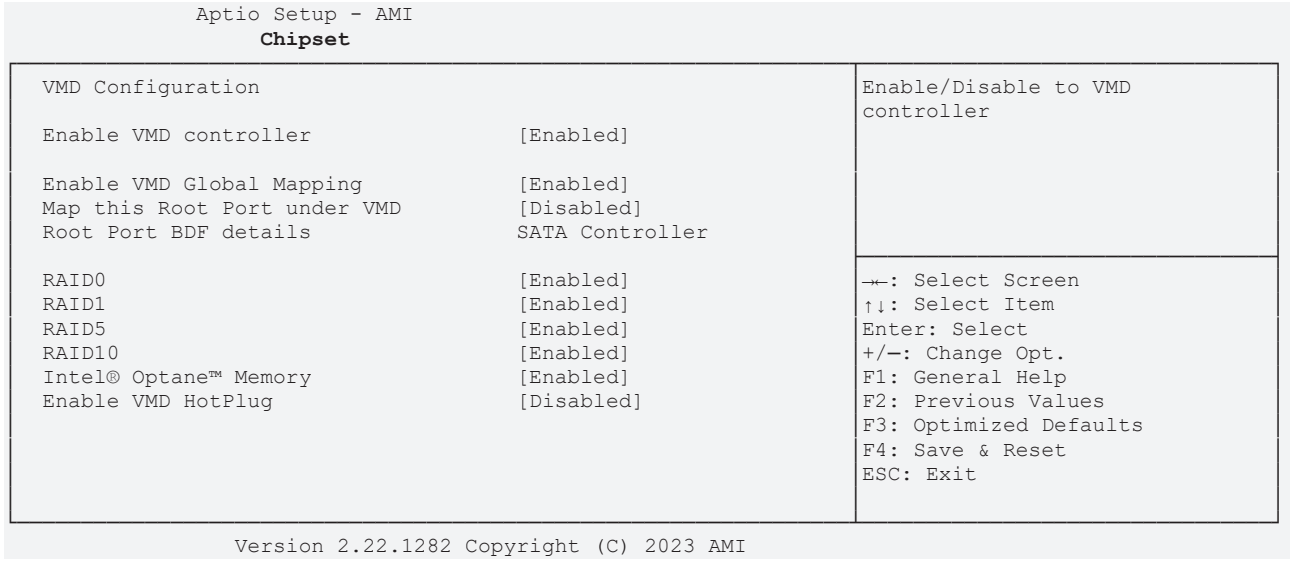
BIOS entry	Options
Intel ® Ultrabook Event Support	
IUER Slate Enable	Disabled / Enabled
IUER Dock Enable	Disabled / Enabled

10.4.1.2 VMD setup menu



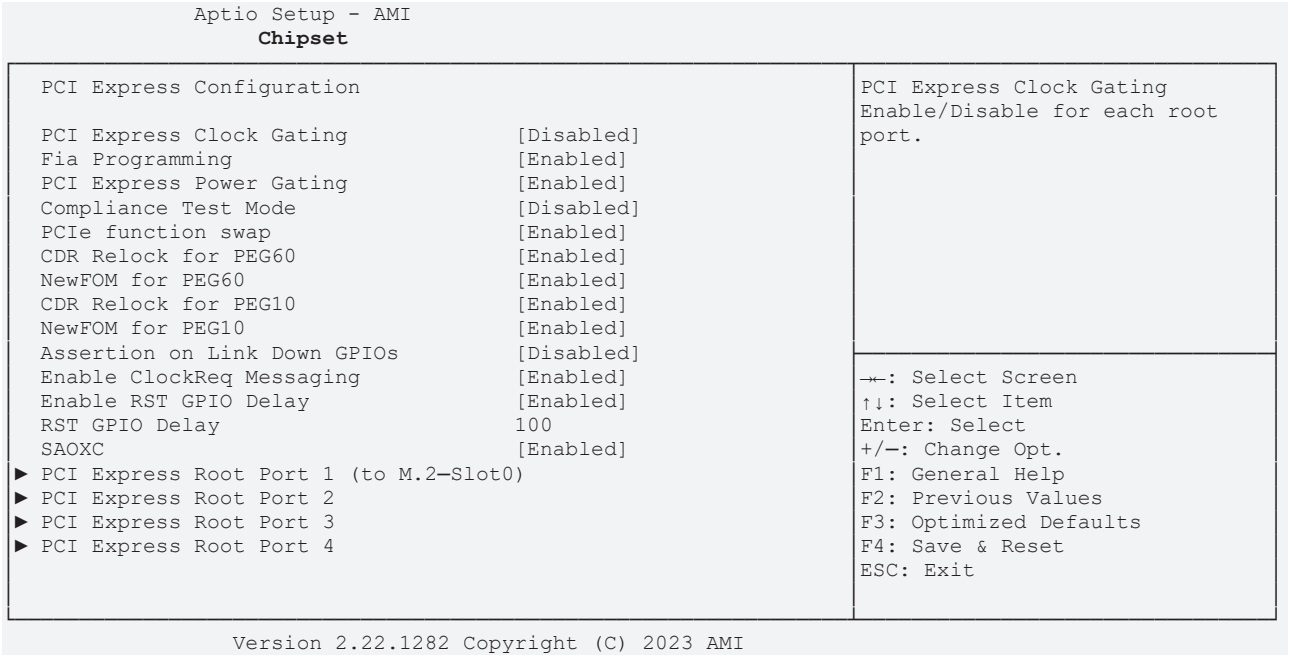
BIOS entry	Options
VMD Configuration	
Enable VMD controller	Disabled / Enabled

10.4.1.3 VMD setup menu enabled



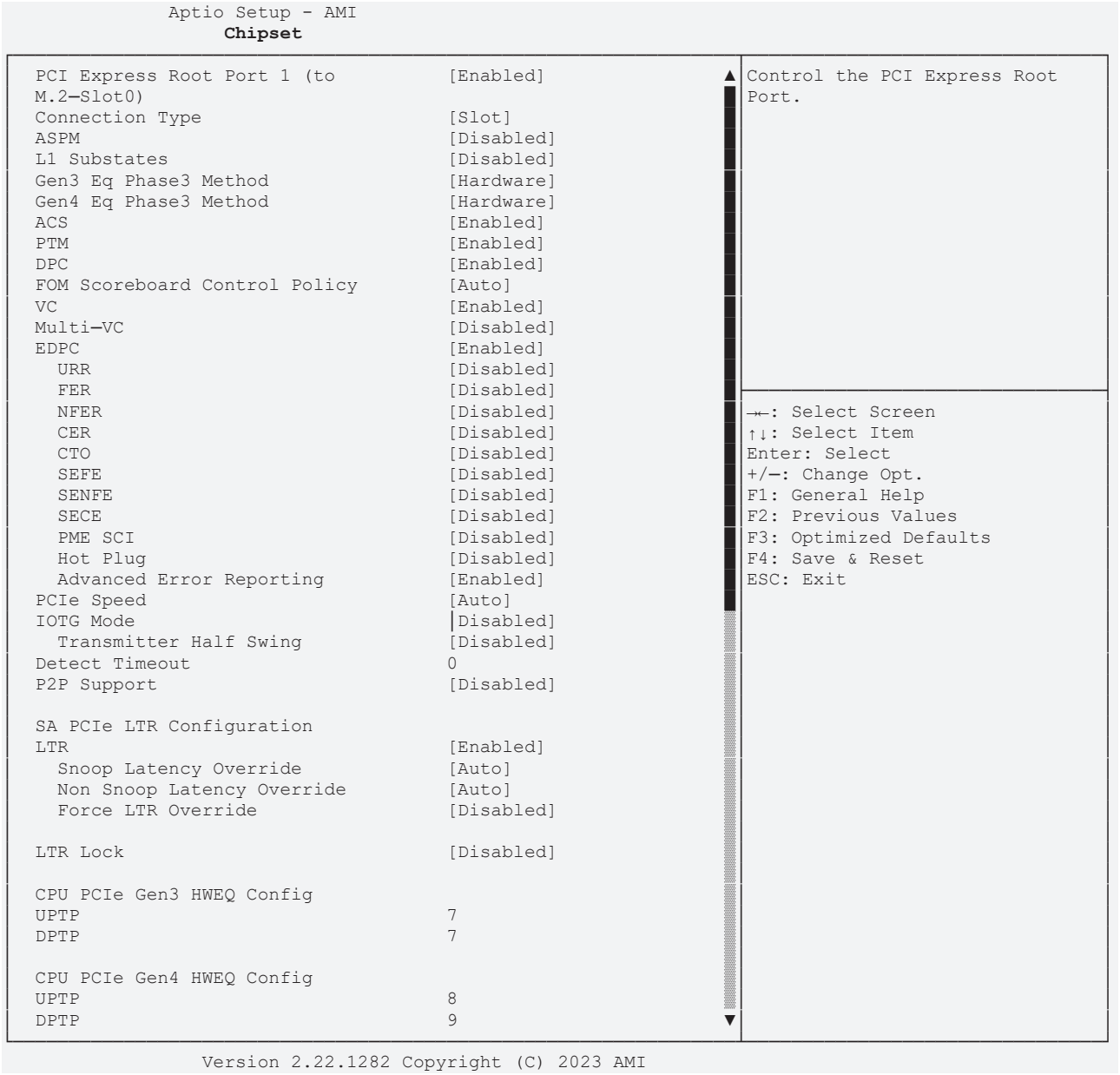
BIOS entry	Options
VMD Configuration	
Enable VMD controller	Enabled
Enable VMD Global Mapping	Enabled
Map this Root Port under VMD	Enabled
Root Port BDF details	None
RAID0	Enabled
RAID1	Enabled
RAID5	Enabled
RAID10	Enabled
Intel® Optane™ Memory	Enabled

10.4.1.4 PCI Express Configuration



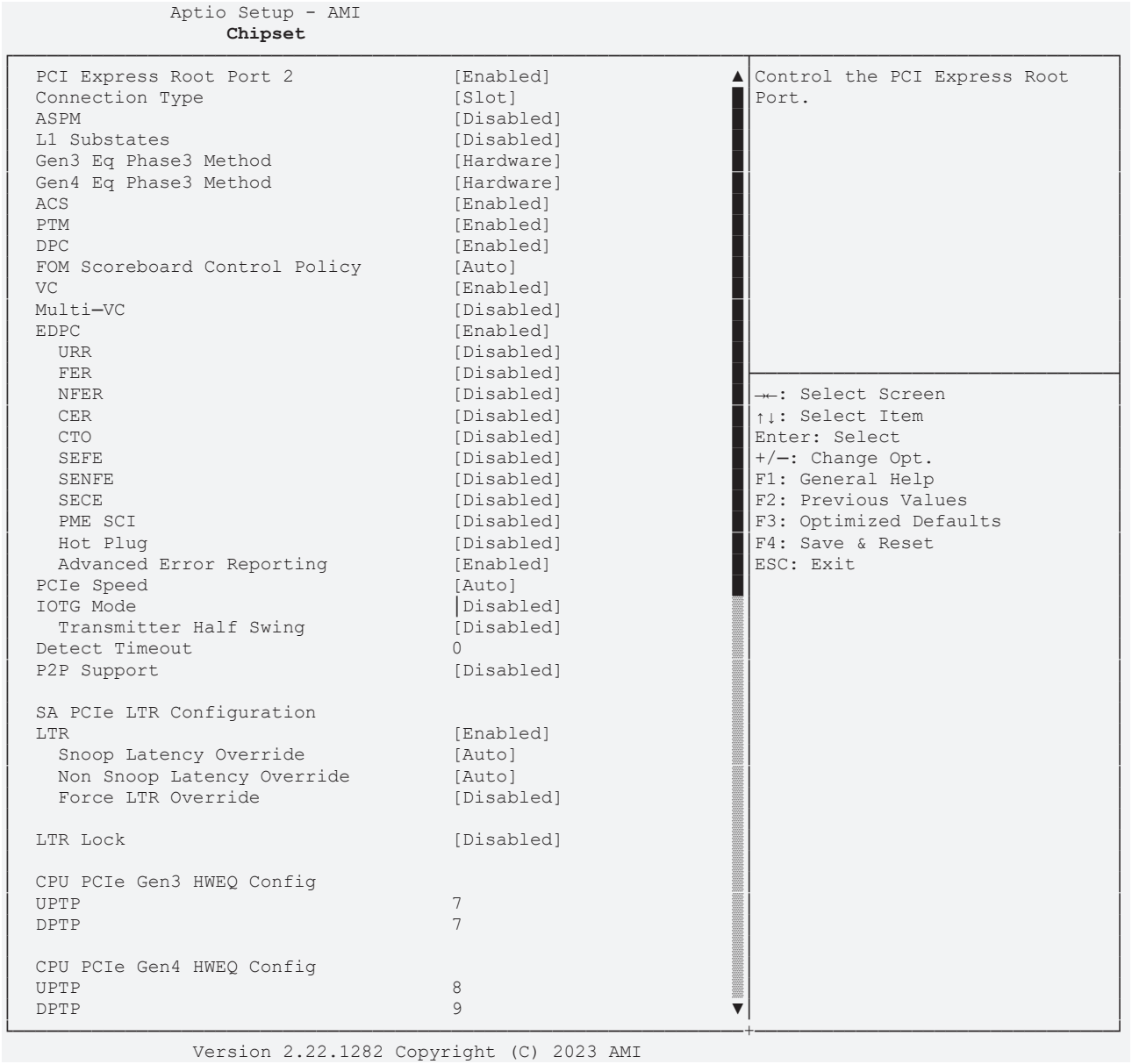
BIOS entry	Options
PCI Express Configuration	
PCI Express Clock Gating	Enabled / Disabled
Fia Programming	Enabled / Disabled
PCI Express Power Gating	Enabled / Disabled
Compliance Test Mode	Disabled / Enabled
PCIe function swap	Disabled / Enabled
CDR Relock for PEG60	Enabled / Disabled
NewFOM for PEG60	Enabled / Disabled
CDR Relock for PEG10	Enabled / Disabled
NewFOM for PEG10	Enabled / Disabled
Assertion on Link Down GPIOs	Disabled / Enabled
Enable ClockReq Messaging	Enabled / Disabled
Enable RST GPIO Delay	Enabled / Disabled
RST GPIO Delay	None
SAOXC	Enabled / Disabled
▶PCI Express Root Port 1 (to M.2 Slot0)	Submenu see: PCI Express Root Port 1 [▶ 69]
▶PCI Express Root Port 2	Submenu see: PCI Express Root Port 2 [▶ 71]
▶PCI Express Root Port 3	Submenu see: PCI Express Root Port 3 [▶ 73]
▶PCI Express Root Port 4	Submenu see: PCI Express Root Port 4 [▶ 75]

10.4.1.4.1 PCI Express Root Port 1



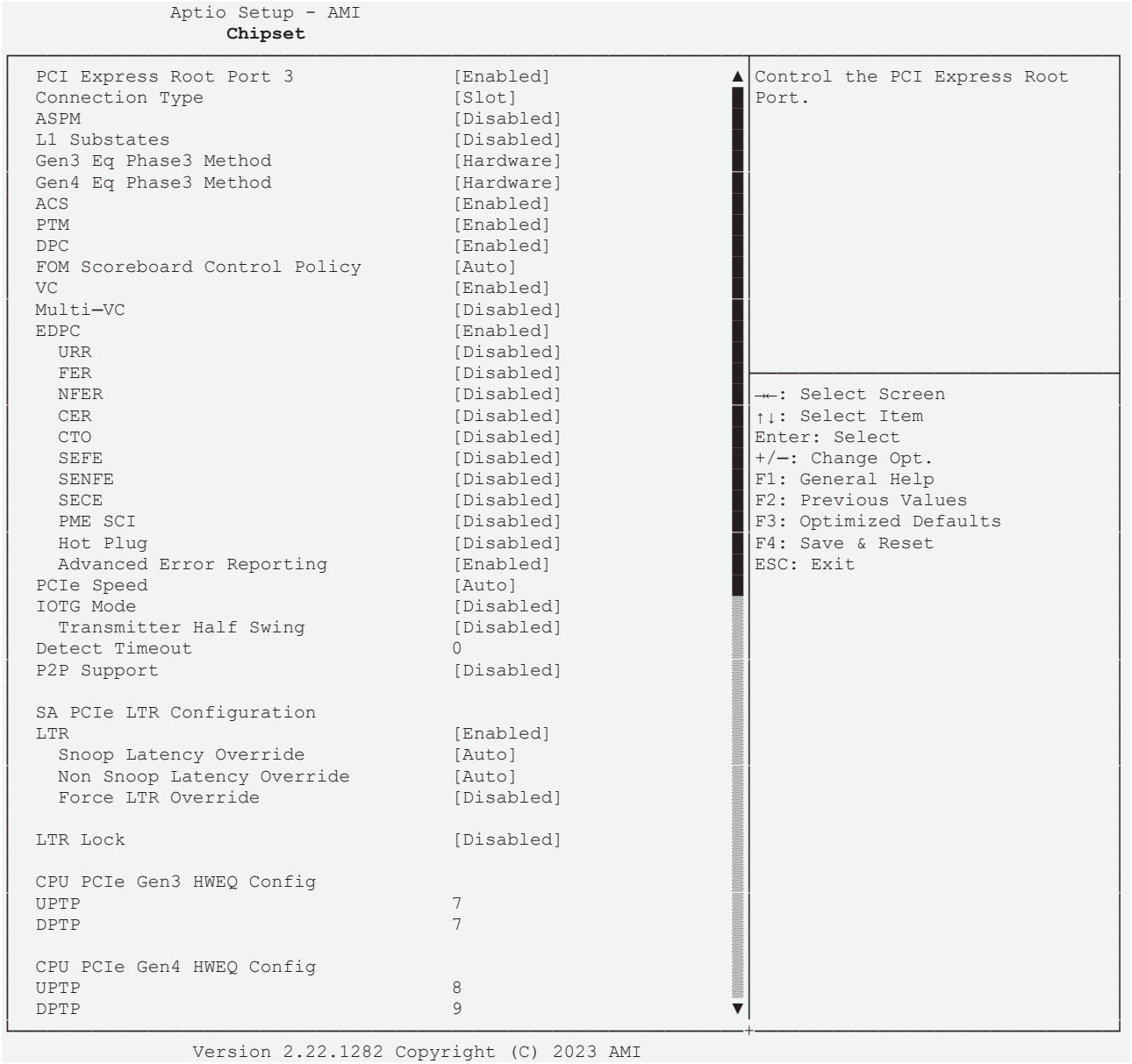
BIOS entry	Options
PCI Express Root Port 1	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
Gen3 Eq Phase3 Method	Hardware / Static Coeff.
Gen4 Eq Phase3 Method	Hardware / Static Coeff.
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
FOM Scoreboard Control Policy	Auto / Gen3 / Gen4 / Gen3 / Gen4
VC	Disabled / Enabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
CTO	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Enabled / Disabled
Hot Plug	None
Advanced Error Reporting	Disabled / Enabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3 / Gen4
IOTG Mode	Disabled / Enabled
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
PSP Support	Disabled / Enabled
SA PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled
CPU PCIe Gen3 HWEQ Config	
UPTP	None
DPTP	None
CPU PCIe Gen HWEQ Config	
UPTP	None
DPTP	None

10.4.1.4.2 PCI Express Root Port 2



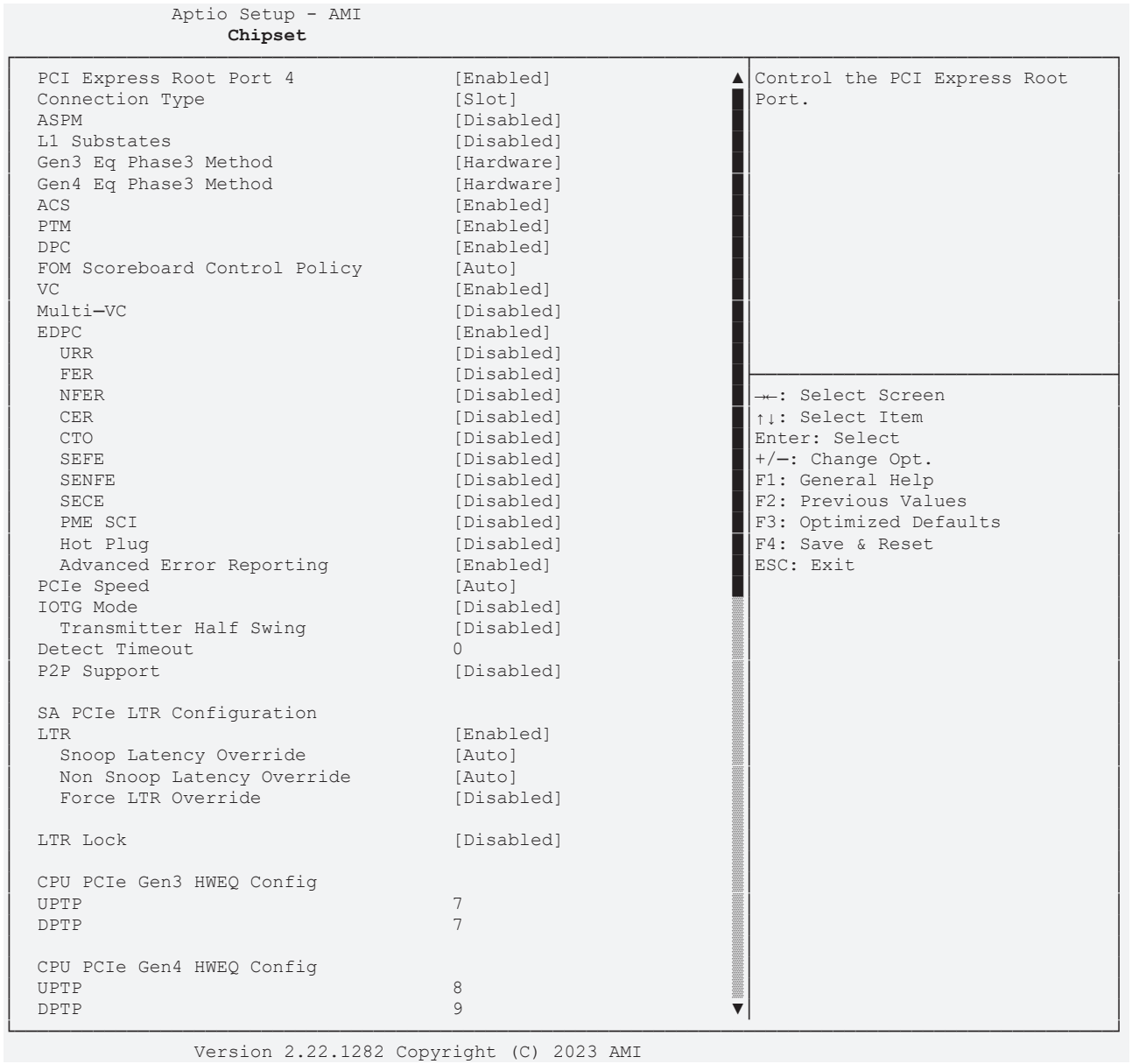
BIOS entry	Options
PCI Express Root Port 2	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
Gen3 Eq Phase3 Method	Hardware / Static Coeff.
Gen4 Eq Phase3 Method	Hardware / Static Coeff.
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
FOM Scoreboard Control Policy	Auto / Gen3 / Gen4 / Gen3 / Gen4
VC	Disabled / Enabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
CTO	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Enabled / Disabled
Hot Plug	None
Advanced Error Reporting	Disabled / Enabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3 / Gen4
IOTG Mode	Disabled / Enabled
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
PSP Support	Disabled / Enabled
SA PCIe LTR Congguration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled
CPU PCIe Gen3 HWEQ Config	
UPTP	None
DPTP	None
CPU PCIe Gen HWEQ Config	
UPTP	None
DPTP	None

10.4.1.4.3 PCI Express Root Port 3



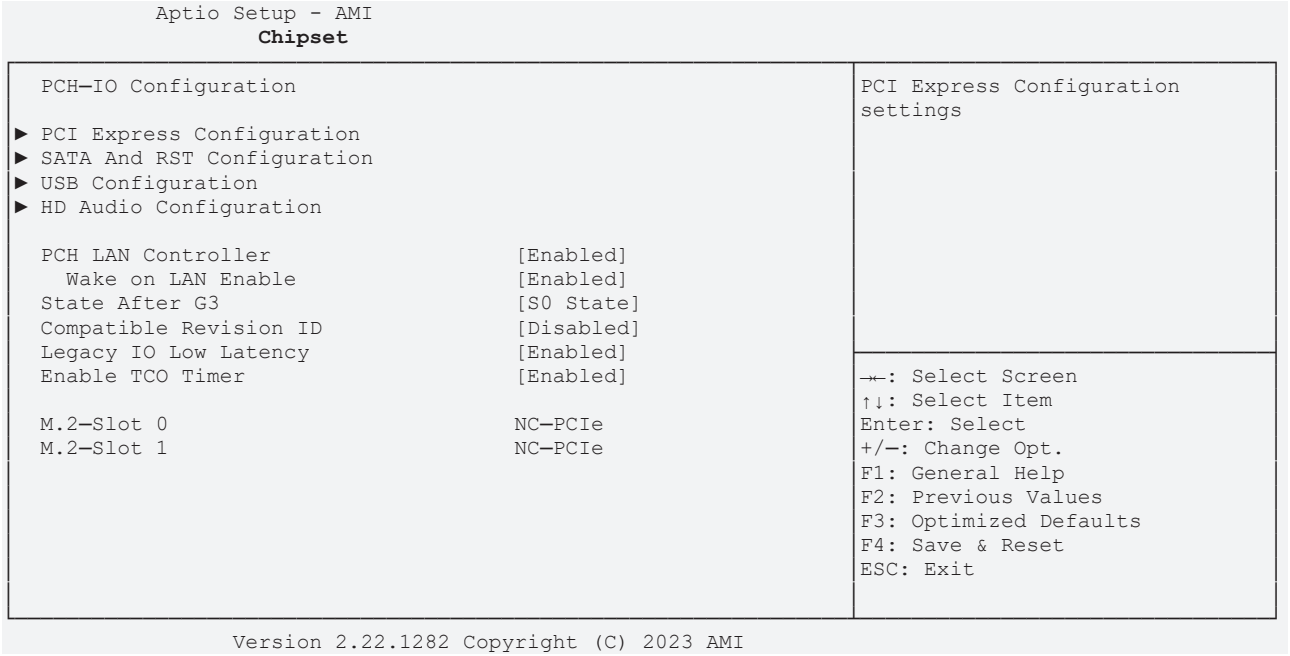
BIOS entry	Options
PCI Express Root Port 3	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
Gen3 Eq Phase3 Method	Hardware / Static Coeff.
Gen4 Eq Phase3 Method	Hardware / Static Coeff.
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
FOM Scoreboard Control Policy	Auto / Gen3 / Gen4 / Gen3 / Gen4
VC	Disabled / Enabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
CTO	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Enabled / Disabled
Hot Plug	None
Advanced Error Reporting	Disabled / Enabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3 / Gen4
IOTG Mode	Disabled / Enabled
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
PSP Support	Disabled / Enabled
SA PCIe LTR Congguration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled
CPU PCIe Gen3 HWEQ Config	
UPTP	None
DPTP	None
CPU PCIe Gen HWEQ Config	
UPTP	None
DPTP	None

10.4.1.4.4 PCI Express Root Port 4



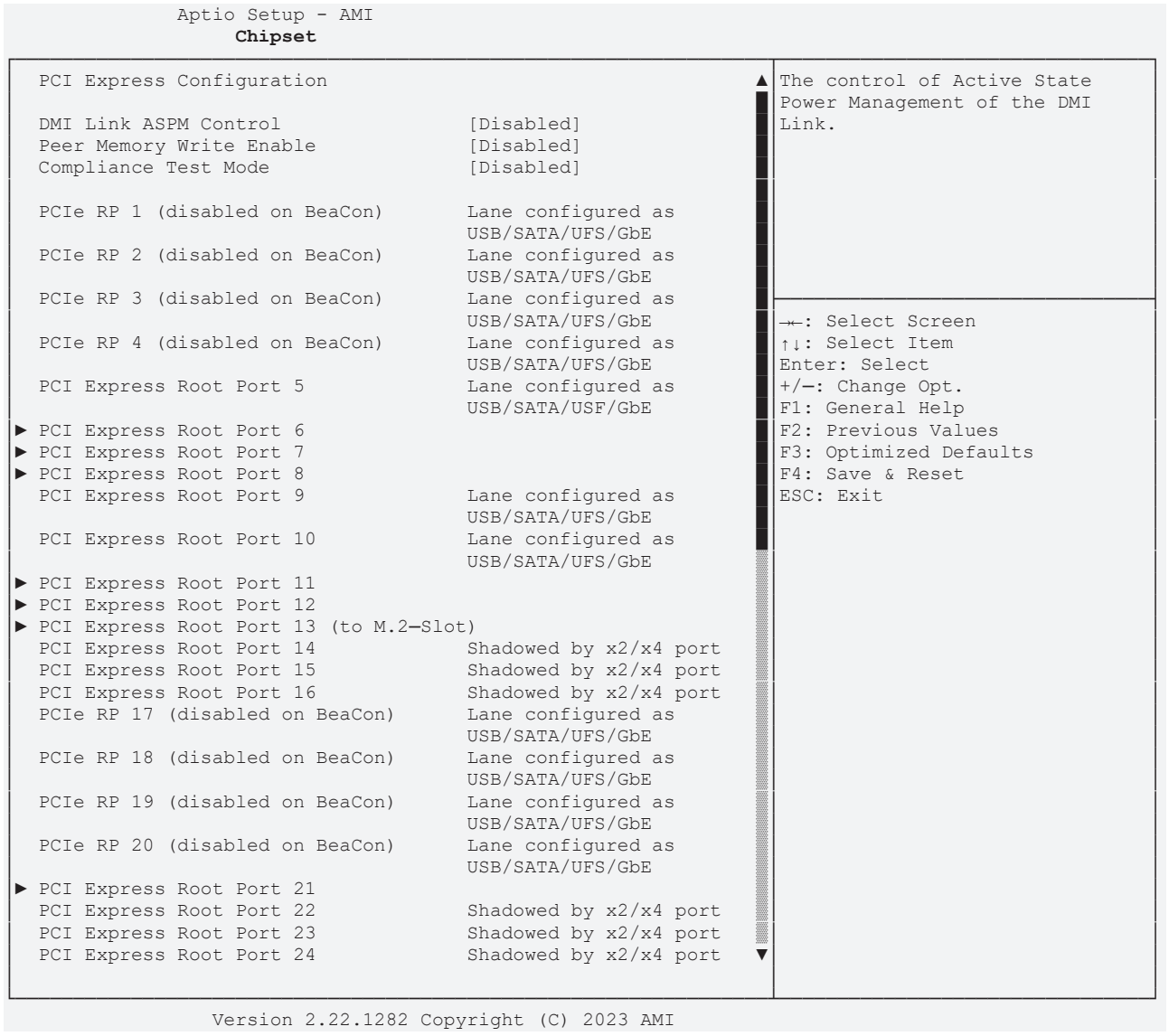
BIOS entry	Options
PCI Express Root Port 4	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
Gen3 Eq Phase3 Method	Hardware / Static Coeff.
Gen4 Eq Phase3 Method	Hardware / Static Coeff.
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
FOM Scoreboard Control Policy	Auto / Gen3 / Gen4 / Gen3 / Gen4
VC	Disabled / Enabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
CTO	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Enabled / Disabled
Hot Plug	None
Advanced Error Reporting	Disabled / Enabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3 / Gen4
IOTG Mode	Disabled / Enabled
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
PSP Support	Disabled / Enabled
SA PCIe LTR Congguration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled
CPU PCIe Gen3 HWEQ Config	
UPTP	None
DPTP	None
CPU PCIe Gen HWEQ Config	
UPTP	None
DPTP	None

10.4.2 PCH-IO Configuration



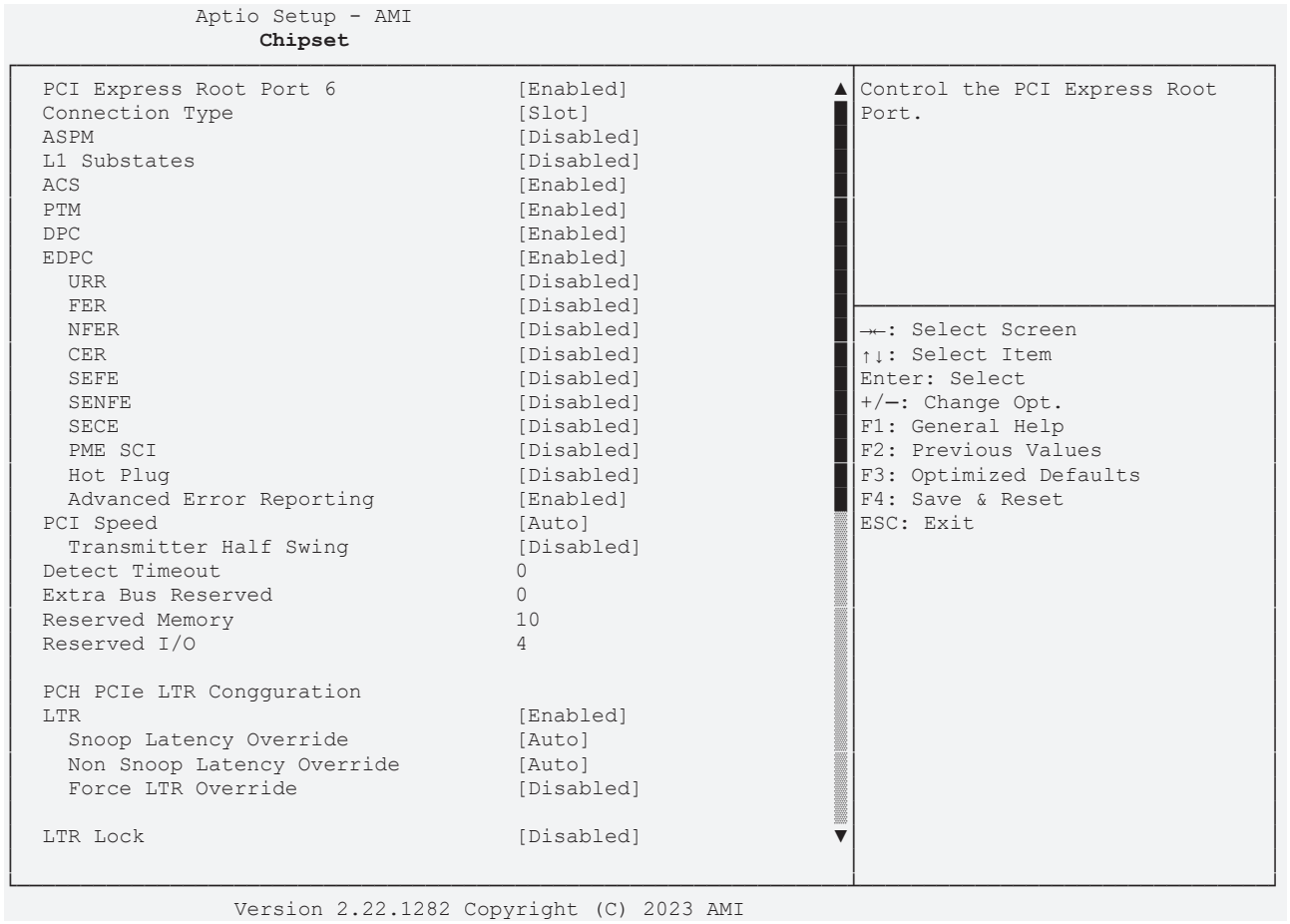
BIOS entry	Options
PCH-IO Configuration	
►PCI Express Configuration	Submenu see: PCI Express Configuration [▶ 78]
►SATA And RST Configuration	Submenu see: SATA And RST Configuration [▶ 94]
►USB Configuration	Submenu see: USB Configuration [▶ 99]
►HD Audio Configuration	Submenu see: HD Audio Configuration [▶ 100]
PCH LAN Controller	Enabled / Disabled
Wake on LAN Enable	S0 State / S5 State
State After G3	Disabled / Enabled
Compatible Revision ID	None
Legacy IO Low Latency	Disabled / Enabled
Enable TCO Timer	Enabled / Disabled
M.2-Slot 0	None
M.2-Slot 1	None

10.4.2.1 PCI Express Configuration



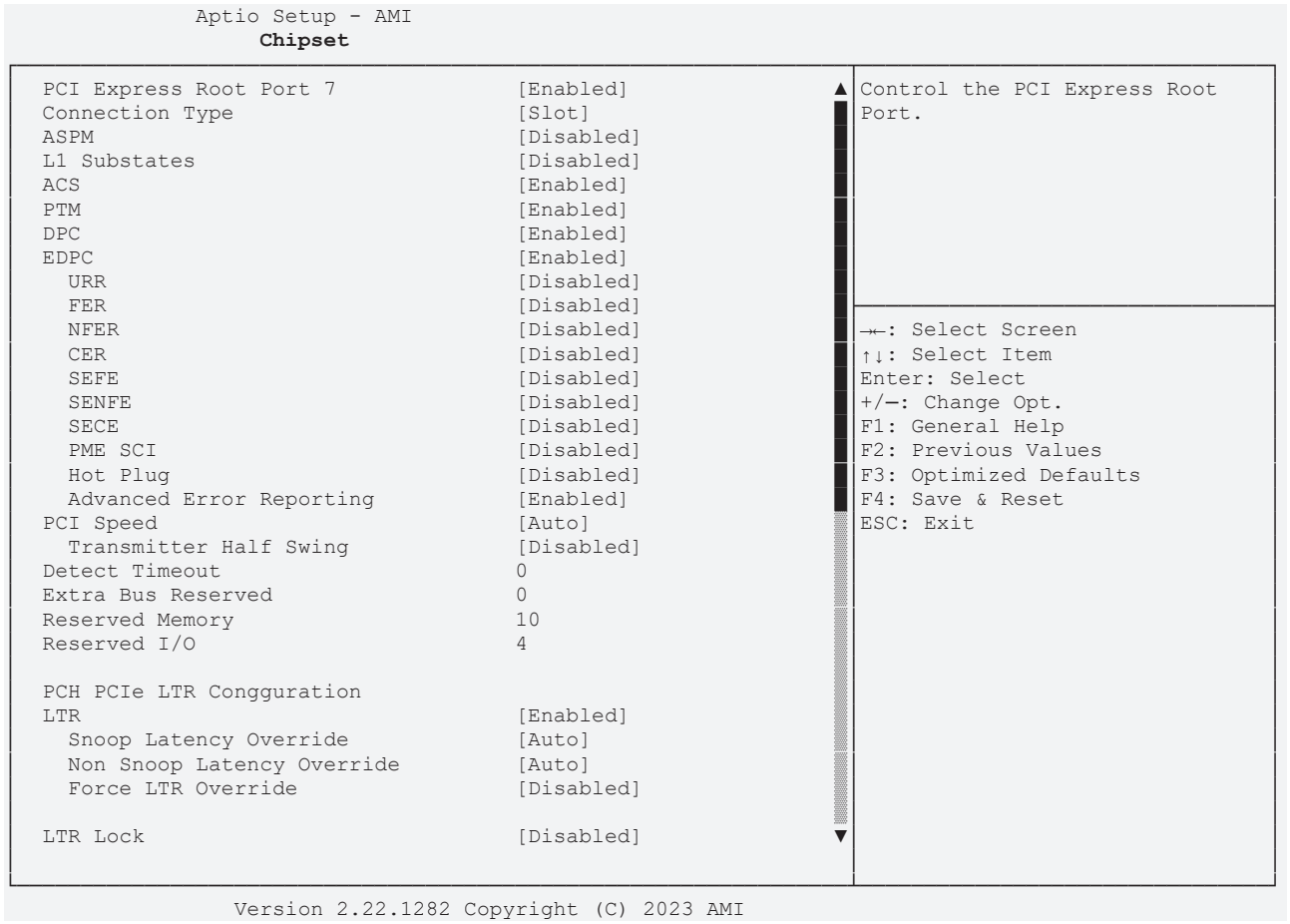
BIOS entry	Options
PCI Express Configuration	
DMI Link ASPM Control	Disabled / L0s / L1 / L0sL1 / Auto
Peer Memory Write Enable	Disabled / Enabled
Compliance Test Mode	Disabled / Enabled
PCIe RP 1 (disabled on BeaCon)	none
PCIe RP 2 (disabled on BeaCon)	None
PCIe RP 3 (disabled on BeaCon)	None
PCIe RP 4 (disabled on BeaCon)	None
PCI Express Root Port 5	None
►PCI Express Root Port 6	Submenu see: PCI Express Root Port 6 [▶ 80]
►PCI Express Root Port 7	Submenu see: PCI Express Root Port 7 [▶ 82]
►PCI Express Root Port 8	Submenu see: PCI Express Root Port 8 [▶ 84]
PCI Express Root Port 9	None
PCI Express Root Port 10	None
►PCI Express Root Port 11	Submenu see: PCI Express Root Port11 [▶ 86]
►PCI Express Root Port 12	None
►PCIe Express Root Port 13 (to M.2-Slot1)	Submenu see: PCI Express Root Port13 [▶ 90]
PCIe Express Root Port 14	None
PCIe Express Root Port 15	None
PCIe Express Root Port 16	None
PCIe RP 17 (disabled on BeaCon)	None
PCIe RP 18 (disabled on BeaCon)	None
PCIe RP 19 (disabled on BeaCon)	None
PCIe RP 20 (disabled on BeaCon)	None
►PCI Express Root Port 21	Submenu see: PCI Express Root Port21 [▶ 92]
PCI Express Root Port 22	None
PCI Express Root Port 23	None
PCI Express Root Port 24	None

10.4.2.1.1 PCI Express Root Port 6



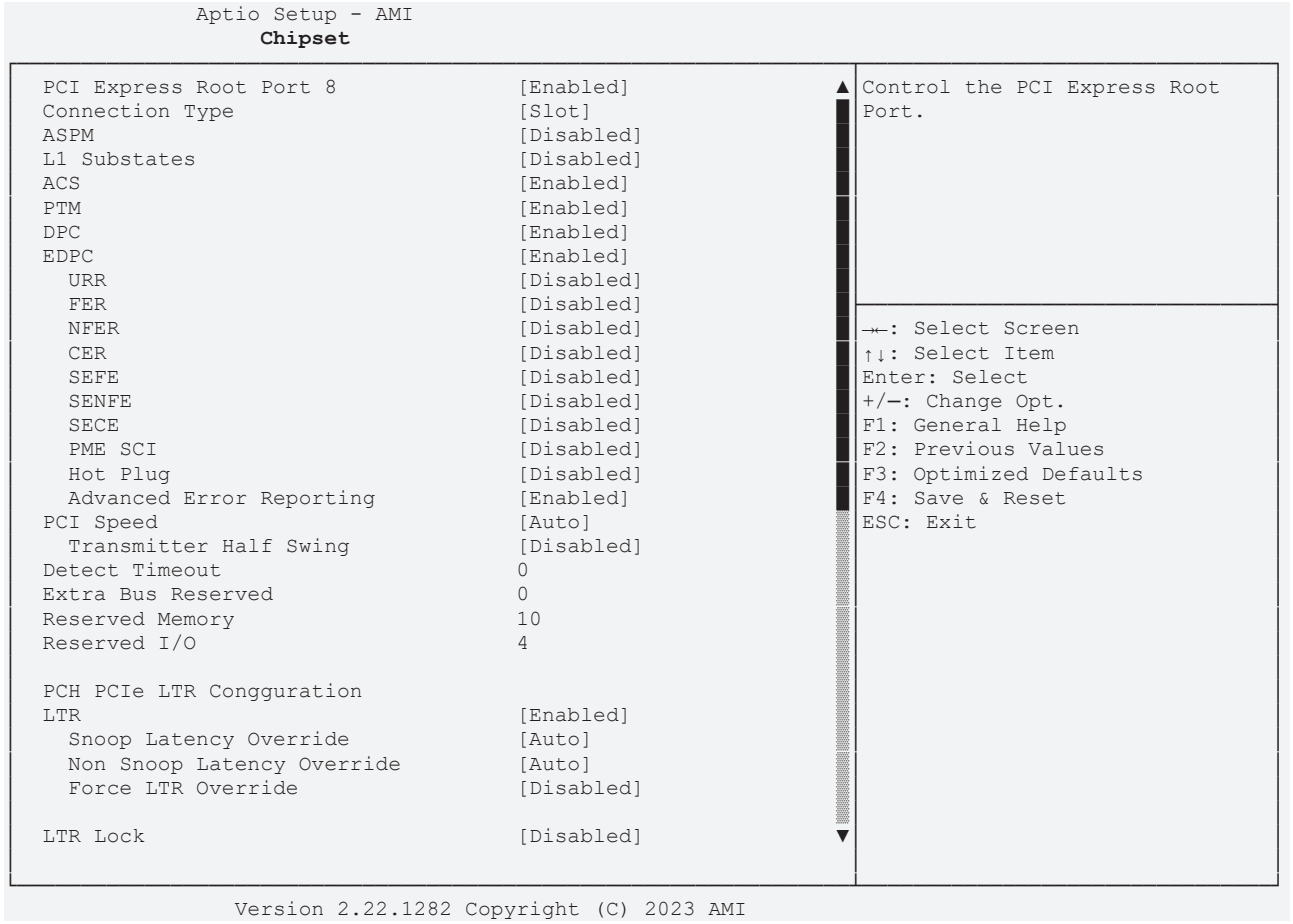
BIOS entry	Options
PCI Express Root Port 6	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

10.4.2.1.2 PCI Express Root Port 7



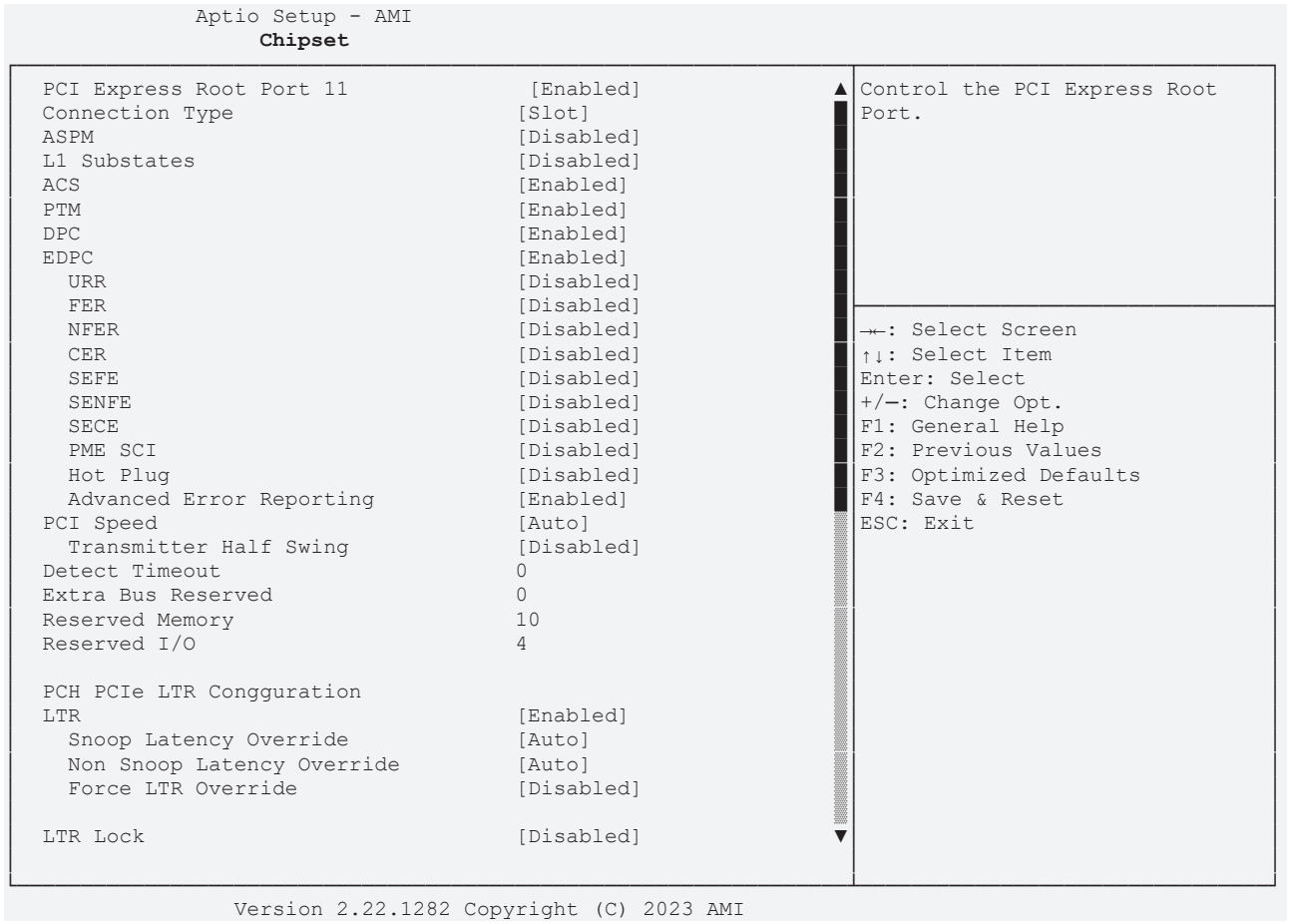
BIOS entry	Options
PCI Express Root Port 7	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

10.4.2.1.3 PCI Express Root Port 8



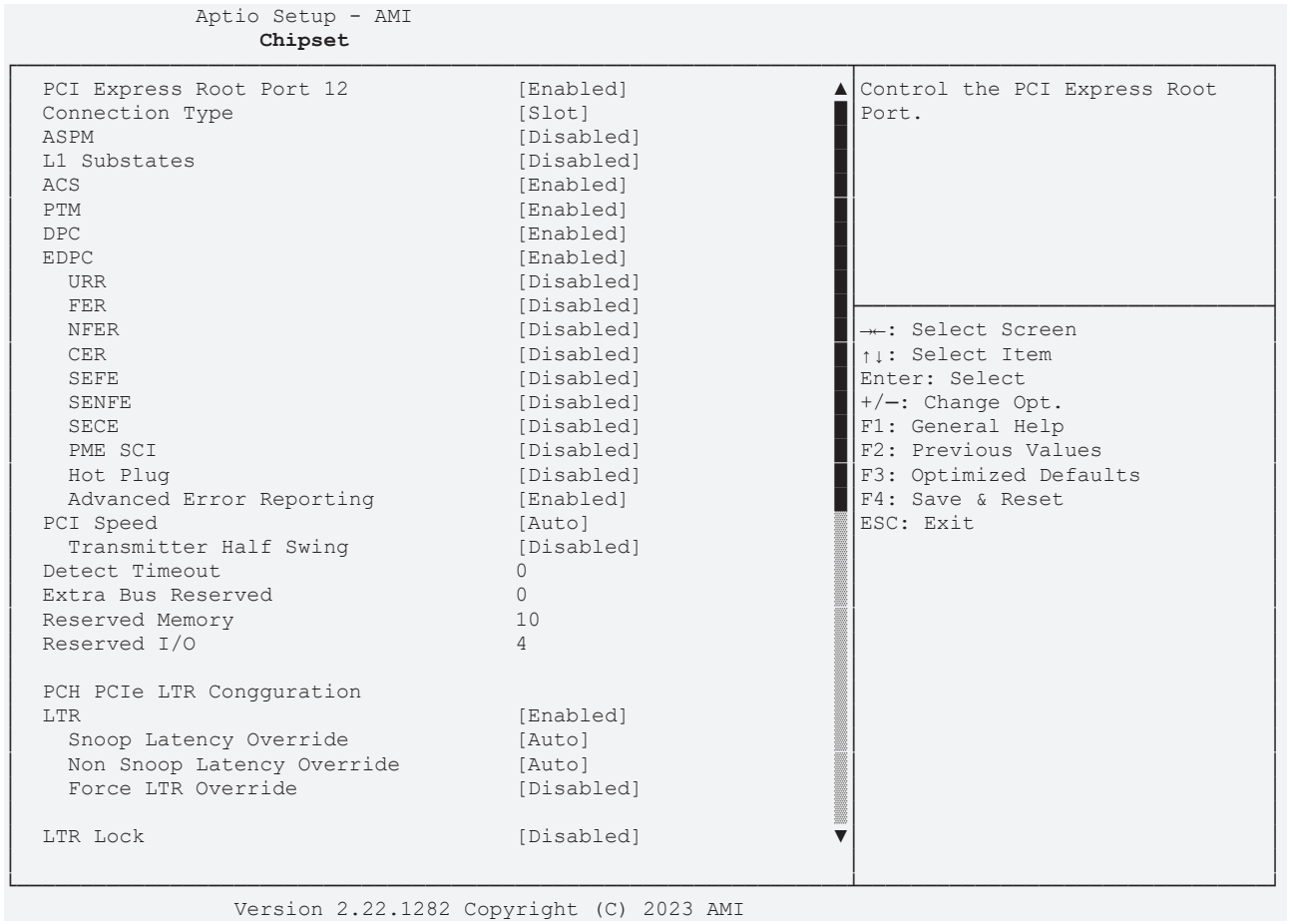
BIOS entry	Options
PCI Express Root Port 8	Enabled / Disabled
Connection Type	Slot / /Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

10.4.2.1.4 PCI Express Root Port11



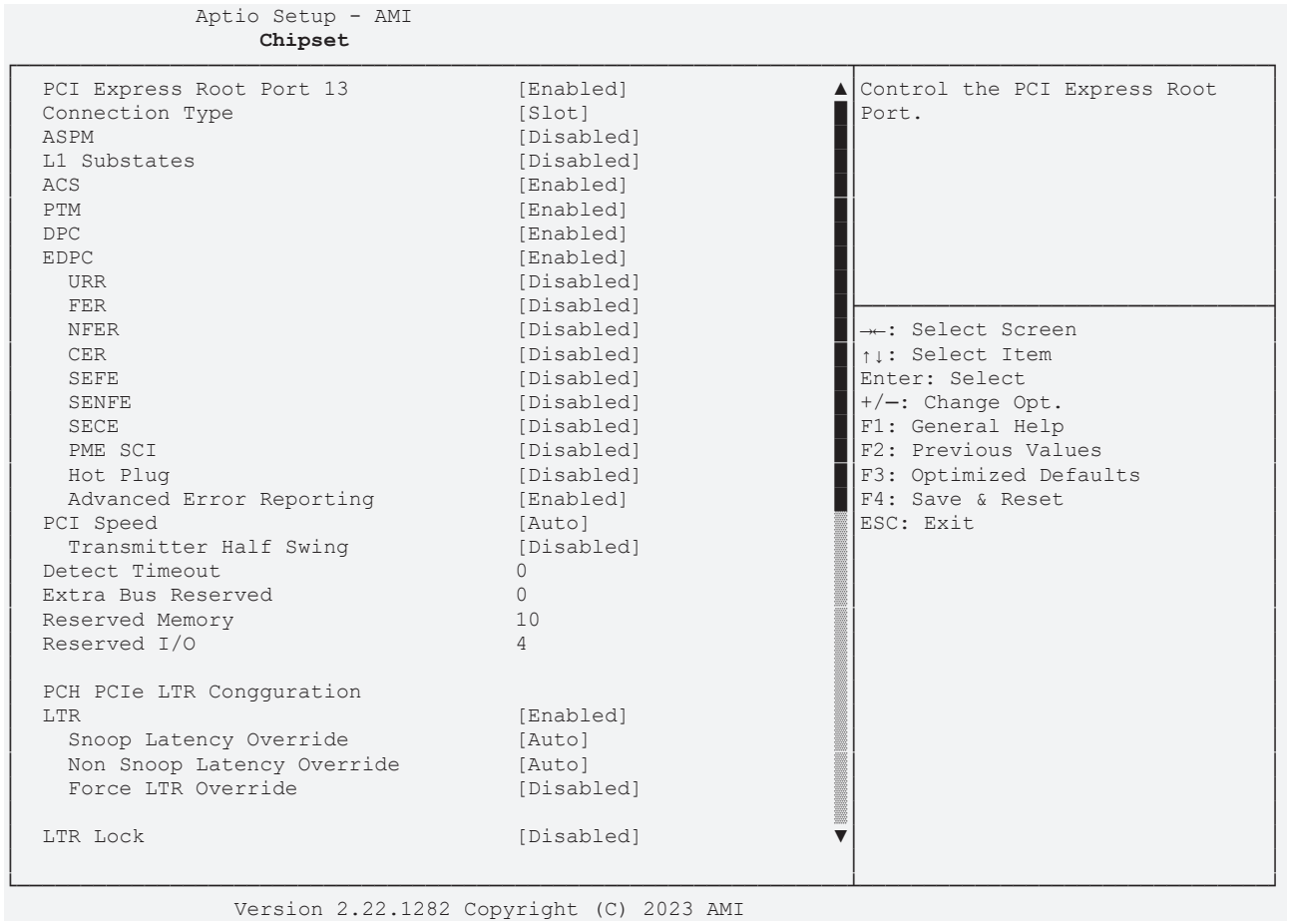
BIOS entry	Options
PCI Express Root Port 11	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

10.4.2.1.5 PCI Express Root Port12



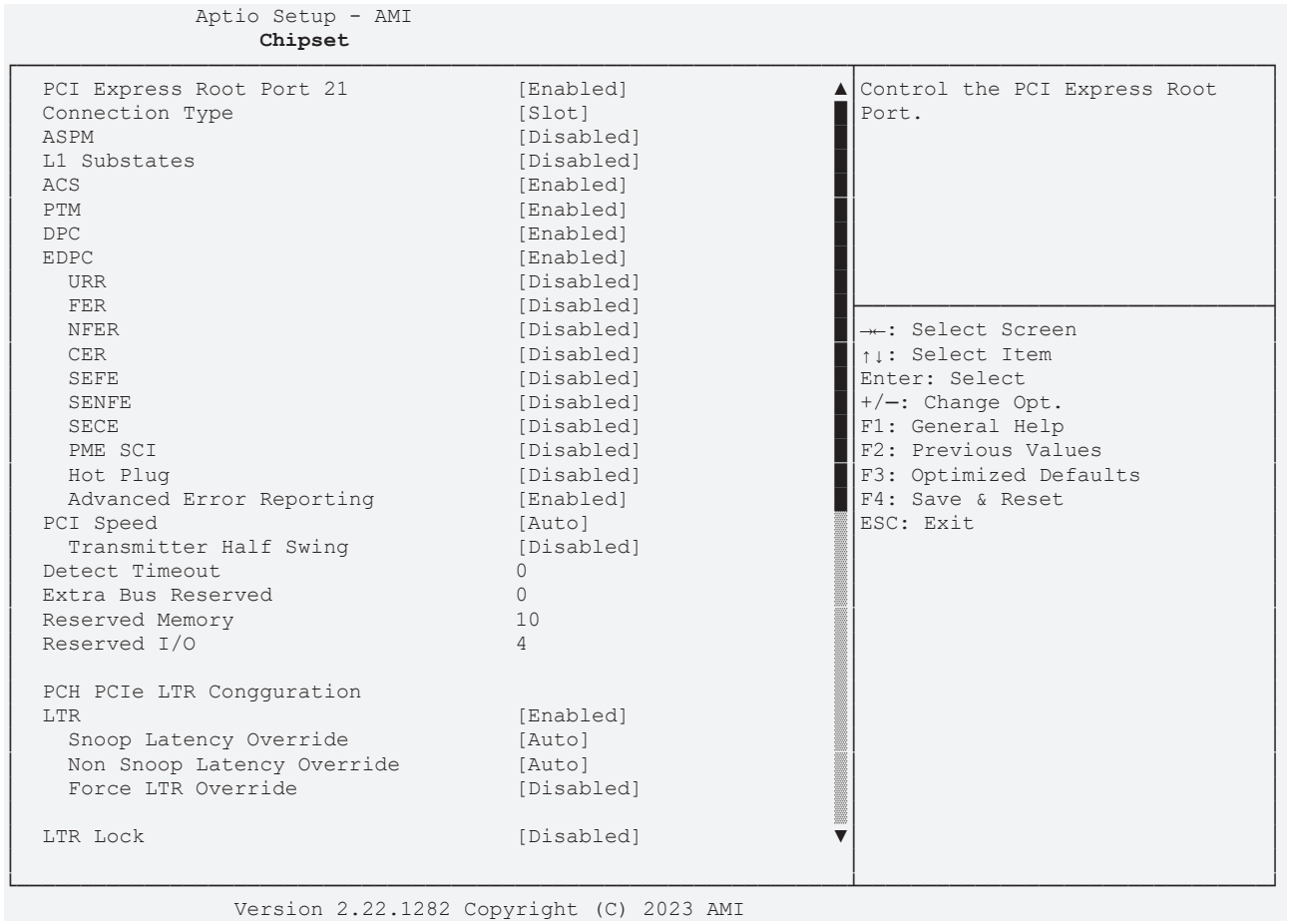
BIOS entry	Options
PCI Express Root Port 12	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

10.4.2.1.6 PCI Express Root Port13



BIOS entry	Options
PCI Express Root Port 13	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

10.4.2.1.7 PCI Express Root Port21

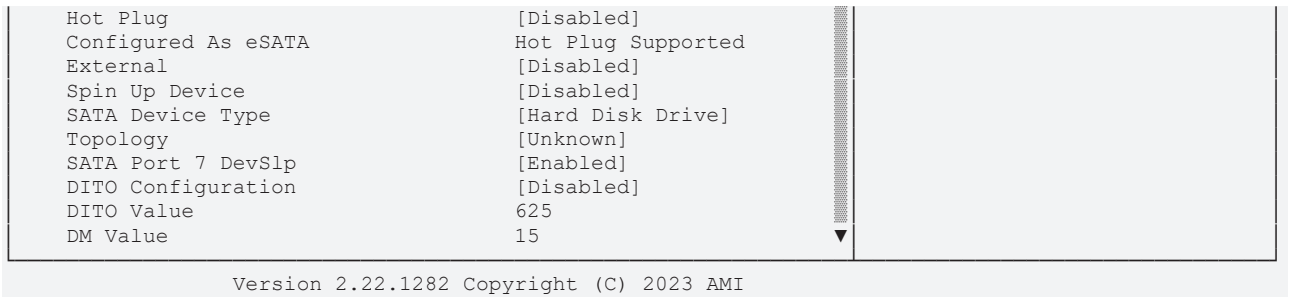


BIOS entry	Options
PCI Express Root Port 21	Enabled / Disabled
Connection Type	Slot / /Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

10.4.2.2 SATA And RST Configuration

```
                Aptio Setup - AMI
                     Chipset
```

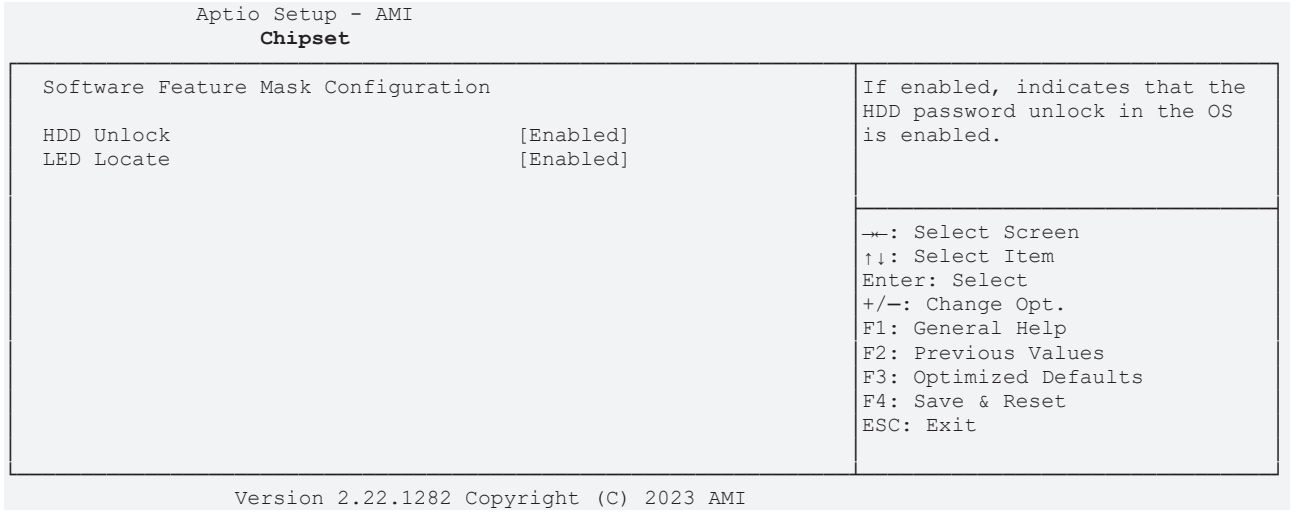
SATA and RST Configuration		Enable/Disable SATA Device.
SATA Controller(s)	[Enabled]	
SATA Test Mode	[Disabled]	
▶ Software Feature Mask Configuration		
Aggressive LPM Support	[Enabled]	
Serial ATA Port 1	Empty	
Software Preserve	Unknown	
Port 1	[Enabled]	→←: Select Screen
Hot Plug	[Disabled]	↑↓: Select Item
Configured As eSATA	Hot Plug Supported	Enter: Select
External	[Disabled]	+/—: Change Opt.
Spin Up Device	[Disabled]	F1: General Help
SATA Device Type	[Hard Disk Drive]	F2: Previous Values
Topology	[Unknown]	F3: Optimized Defaults
SATA Port 1 DevSlp	[Enabled]	F4: Save & Reset
DITO Configuration	[Disabled]	ESC: Exit
DITO Value	625	
DM Value	15	
Serial ATA Port 3	Empty	
Software Preserve	Unknown	
Port 3	[Enabled]	
Hot Plug	[Disabled]	
Configured As eSATA	Hot Plug Supported	
External	[Disabled]	
Spin Up Device	[Disabled]	
SATA Device Type	[Hard Disk Drive]	
Topology	[Unknown]	
SATA Port 3 DevSlp	[Enabled]	
DITO Configuration	[Disabled]	
DITO Value	625	
DM Value	15	
Serial ATA Port 4	Empty	
Software Preserve	Unknown	
Port 4	[Enabled]	
Hot Plug	[Disabled]	
Configured As eSATA	Hot Plug Supported	
External	[Disabled]	
Spin Up Device	[Disabled]	
SATA Device Typ	[Hard Disk Drive]	
Topology	[Unknown]	
SATA Port 4 DevSlp	[Enabled]	
DITO Configuration	[Disabled]	
DITO Value	625	
DM Value	15	
Serial ATA Port 5	Empty	
Software Preserve	Unknown	
Port 5	[Enabled]	
Hot Plug	[Disabled]	
Configured As eSATA	Hot Plug Supported	
External	[Disabled]	
Spin Up Device	[Disabled]	
SATA Device Type	[Hard Disk Drive]	
Topology	[Unknown]	
SATA Port 5 DevSlp	[Enabled]	
DITO Configuration	[Disabled]	
DITO Value	625	
DM Value	15	
Serial ATA Port 6	Empty	
Software Preserve	Unknown	
Port 6	[Enabled]	
Hot Plug	[Disabled]	
Configured As eSATA	Hot Plug Supported	
External	[Disabled]	
Spin Up Device	[Disabled]	
SATA Device Type	[Hard Disk Drive]	
Topology	[Unknown]	
SATA Port 6 DevSlp	[Enabled]	
DITO Configuration	[Disabled]	
DITO Value	625	
DM Value	15	
Serial ATA Port 7	Empty	
Software Preserve	Unknown	
Port 7	[Enabled]	


Hot Plug [Disabled]
Configured As eSATA Hot Plug Supported
External [Disabled]
Spin Up Device [Disabled]
SATA Device Type [Hard Disk Drive]
Topology [Unknown]
SATA Port 7 DevSlp [Enabled]
DITO Configuration [Disabled]
DITO Value 625
DM Value 15
Version 2.22.1282 Copyright (C) 2023 AMI

BIOS entry	Options
SATA and RST Configuration	
SATA Controller(s)	Enabled / Disabled
SATA Mode Selection	None
SATA Test Mode	Disabled / Enabled
►Software Feature Mask Configuration	Submenu see: Software Feature Mask Configuration [▶ 98]
Aggressive LPM Support	Enabled / Disabled
Serial ATA Port 1	None
Software Preserve	None
Port 1	Enabled / Disabled
Hot Plug	Disabled / Enabled
Configured As eSATA	None
External	Disabled / Enabled
Spin Up Device	Disabled / Enabled
SATA Device Type	Hard Disk Drive / Solid State Drive
Topology	Unknown / ISATA / Direct Connect / Flex / M2
SATA Port 1 DevSlp	Enabled / Disabled
DITO Configuration	Disabled / Enabled
DITO Value	None
DM Value	None
Serial ATA Port 3	None
Software Preserve	None
Port 3	Enabled / Disabled
Hot Plug	Disabled / Enabled
Configured As eSATA	None
External	Disabled / Enabled
Spin Up Device	Disabled / Enabled
SATA Device Type	Hard Disk Drive / Solid State Drive
Topology	Unknown / ISATA / Direct Connect / Flex / M2
SATA Port 3 DevSlp	Enabled / Disabled
DITO Configuration	Disabled / Enabled
DITO Value	None
DM Value	None
Serial ATA Port 4	None
Software Preserve	None
Port 4	Enabled / Disabled
Hot Plug	Disabled / Enabled
Configured As eSATA	None
External	Disabled / Enabled
Spin Up Device	Disabled / Enabled
SATA Device Type	Hard Disk Drive / Solid State Drive
Topology	Unknown / ISATA / Direct Connect / Flex / M2
SATA Port 4 DevSlp	Enabled / Disabled
DITO Configuration	Disabled / Enabled
DITO Value	None
DM Value	None

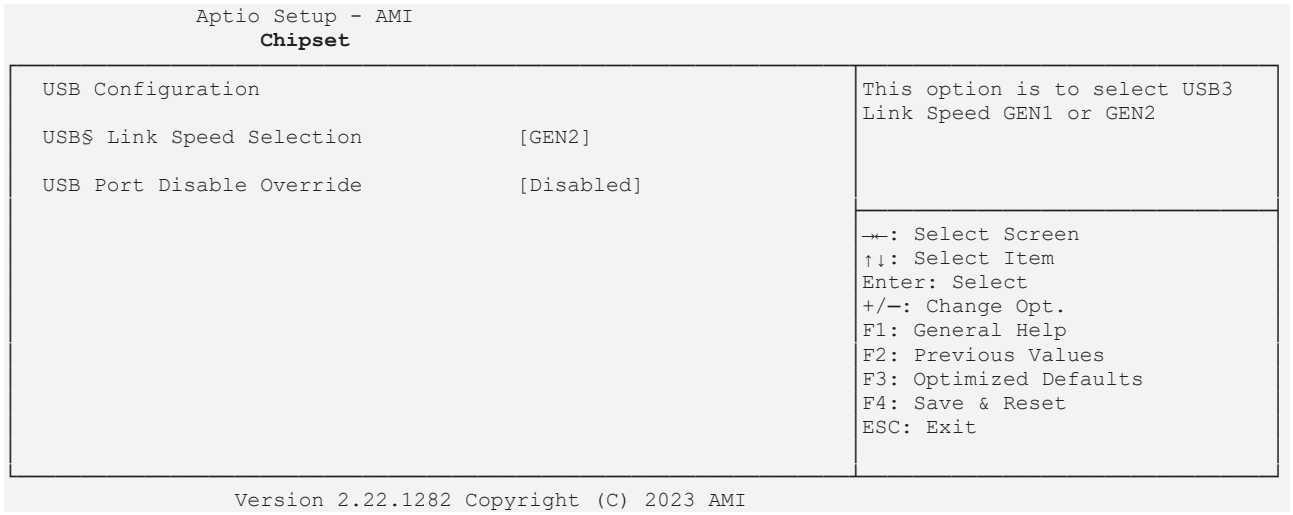
BIOS entry	Options
Serial ATA Port 5	None
Software Preserve	None
Port 5	Enabled / Disabled
Hot Plug	Disabled / Enabled
Configured As eSATA	None
External	Disabled / Enabled
Spin Up Device	Disabled / Enabled
SATA Device Type	Hard Disk Drive / Solid State Drive
Topology	Unknown / ISATA / Direct Connect / Flex / M2
SATA Port 5 DevSlp	Enabled / Disabled
DITO Configuration	Disabled / Enabled
DITO Value	None
DM Value	None
Serial ATA Port 6	None
Software Preserve	None
Port 6	Enabled / Disabled
Hot Plug	Disabled / Enabled
Configured As eSATA	None
External	Disabled / Enabled
Spin Up Device	Disabled / Enabled
SATA Device Type	Hard Disk Drive / Solid State Drive
Topology	Unknown / ISATA / Direct Connect / Flex / M2
SATA Port 6 DevSlp	Enabled / Disabled
DITO Configuration	Disabled / Enabled
DITO Value	None
DM Value	None
Serial ATA Port 7	None
Software Preserve	None
Port 7	Enabled / Disabled
Hot Plug	Disabled / Enabled
Configured As eSATA	None
External	Disabled / Enabled
Spin Up Device	Disabled / Enabled
SATA Device Type	Hard Disk Drive / Solid State Drive
Topology	Unknown / ISATA / Direct Connect / Flex / M2
SATA Port 7 DevSlp	Enabled / Disabled
DITO Configuration	Disabled / Enabled
DITO Value	None
DM Value	None

10.4.2.2.1 Software Feature Mask Configuration



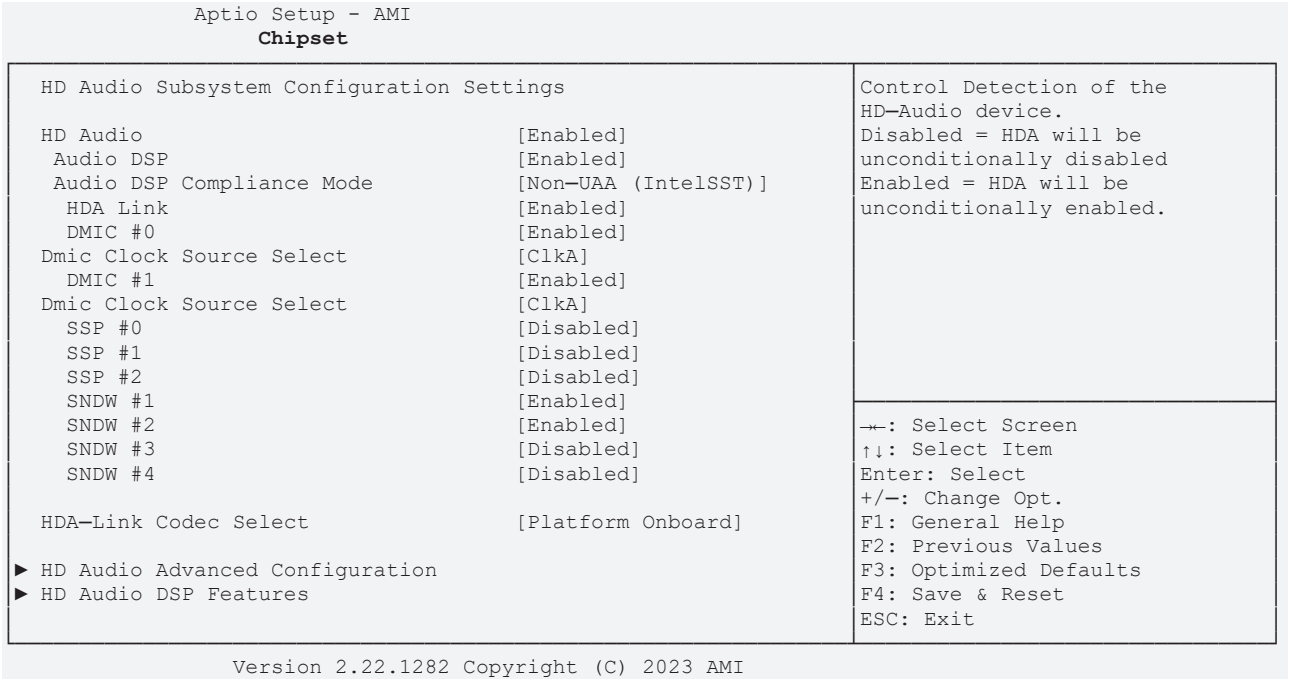
BIOS entry	Options
Software Feature Mask Configuration	
HDD Unlock	Enabled / Disabled
LED Locate	Enabled / Disabled

10.4.2.3 USB Configuration



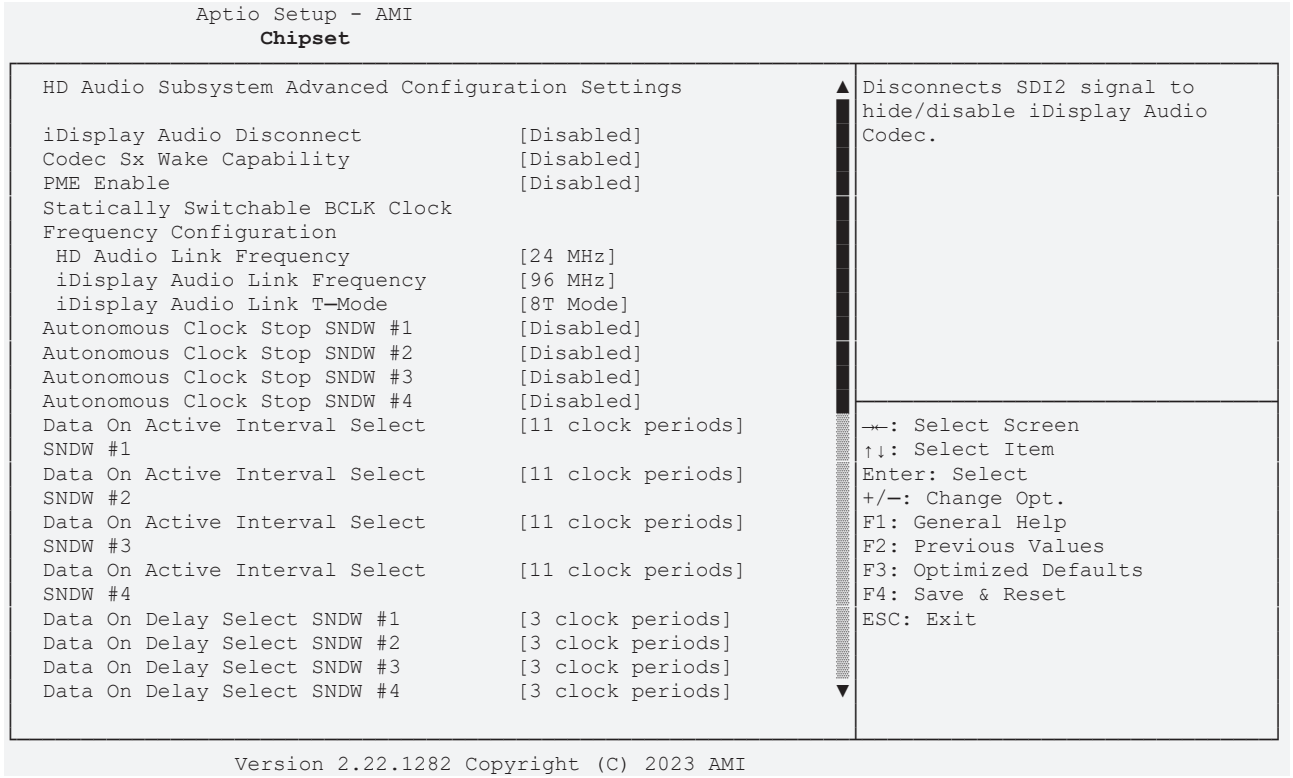
BIOS entry	Options
USB Configuration	
USB3 Link Speed Selection	Gen2 / Gen1
USB Port Disable Override	Disabled / Select Per-Pin

10.4.2.4 HD Audio Configuration



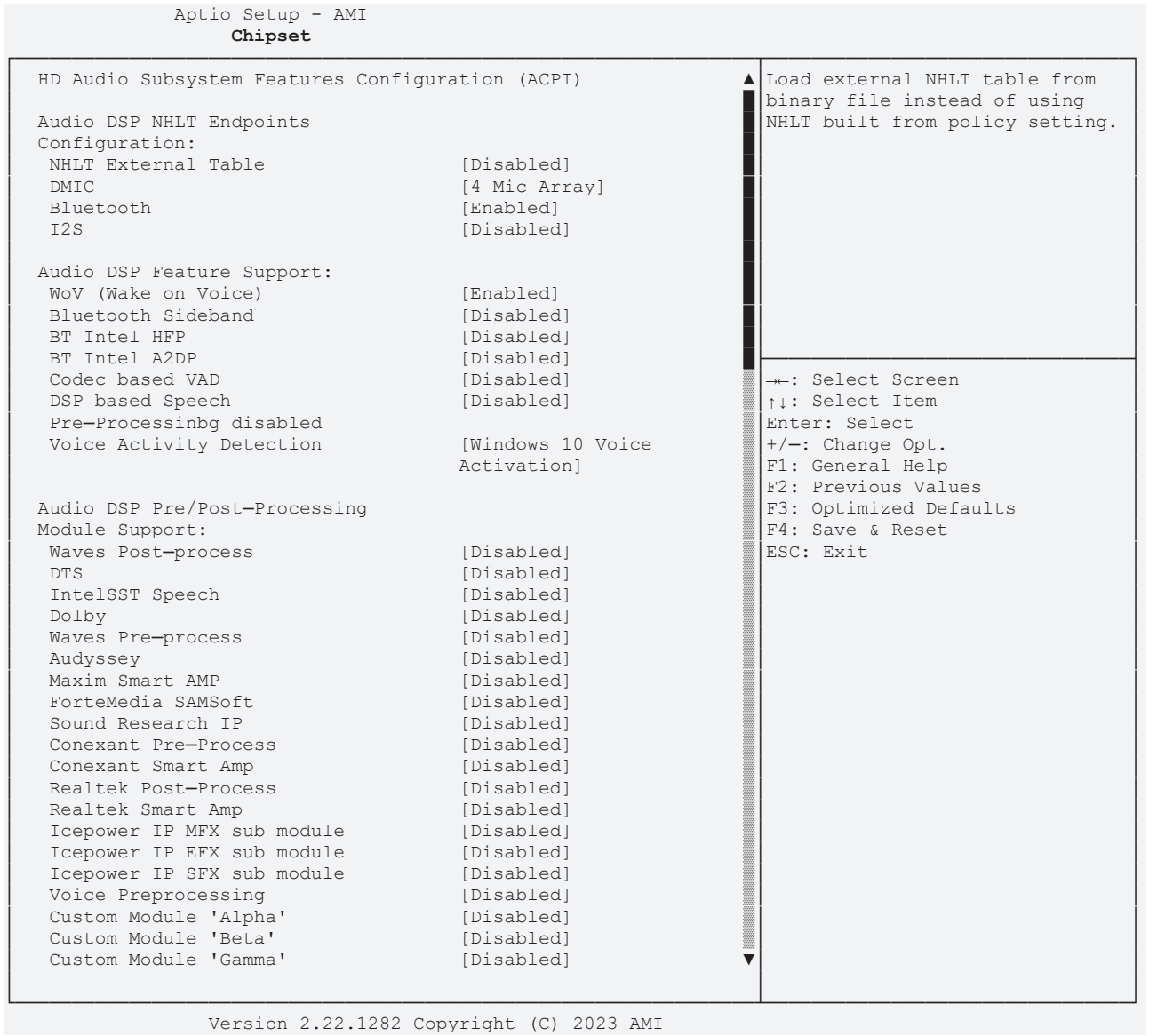
BIOS entry	Options
HD Audio Subsystem Configuration Settings	
HD Audio	Enabled / Disabled
Audio DSP	Enabled / Disabled
Audio DSP Compliance Mode	Non-UAA (IntelSST) / UAA (HDA Inbox/IntelSST)
HDA Link	Enabled / Disabled
DMIC #0	Enabled / Disabled
Dmic Clock Source Select	None
DMIC #1	Enabled / Disabled
Dmic Clock Source Select	None
SSP #0	Disabled / Enabled
SSP #1	Disabled / Enabled
SSP #2	Disabled / Enabled
SNDW #1	Enabled / Disabled
SNDW #2	Enabled / Disabled
SNDW #3	Disabled / Enabled
SNDW #4	Disabled / Enabled
HDA-Link Codec Select	Platform Onboard / External Kit
►HD Audio Advanced Configuration	Submenu see: HD Audio Advanced Configuration [▶ 101]
►HD Audio DSP Features Configuration	Submenu see: HD Audio DSP Features Configuration [▶ 102]

10.4.2.4.1 HD Audio Advanced Configuration



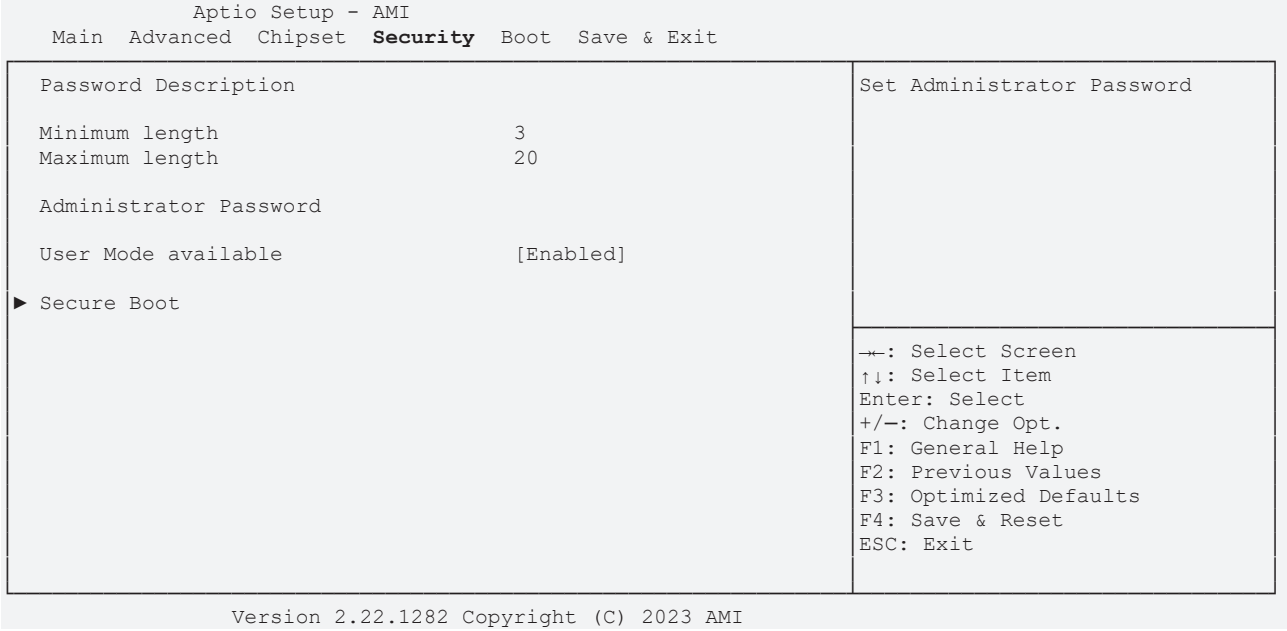
BIOS entry	Options
HD Audio Subsystem Advanced Configuration Settings	
iDisplay Audio Disconnect	Disabled / Enabled
Codec Sx Wake Capability	Disabled / Enabled
PME Enable	Disabled / Enabled
Statically Switchable BCLK Clock DPC Frequency Configuration:	
HD Audio Link Frequency	6 MHz / 12 MHz / 24 MHz
iDisplay Audio Link Frequency	48 MHz / 96 MHz
iDisplay Audio Link T–Mode FER	2T Mode / 4T Mode / 8T Mode / 16T Mode
Autonomous Clock Stop SNDW #1	Disabled / Enabled
Autonomous Clock Stop SNDW #2	Disabled / Enabled
Autonomous Clock Stop SNDW #3	Disabled / Enabled
Autonomous Clock Stop SNDW #4	Disabled / Enabled
Data On Active Interval Select SNDW #1	6 / 7 / 8 / 11 clock periods
Data On Active Interval Select SNDW #2	6 / 7 / 8 / 11 clock periods
Data On Active Interval Select SNDW #3	6 / 7 / 8 / 11 clock periods
Data On Active Interval Select SNDW #4	6 / 7 / 8 / 11 clock periods
Data On Delay Select SNDW #1	2 / 3 clock periods
Data On Delay Select SNDW #2	2 / 3 clock periods
Data On Delay Select SNDW #3	2 / 3 clock periods
Data On Delay Select SNDW #4	2 / 3 clock periods

10.4.2.4.2 HD Audio DSP Features Configuration



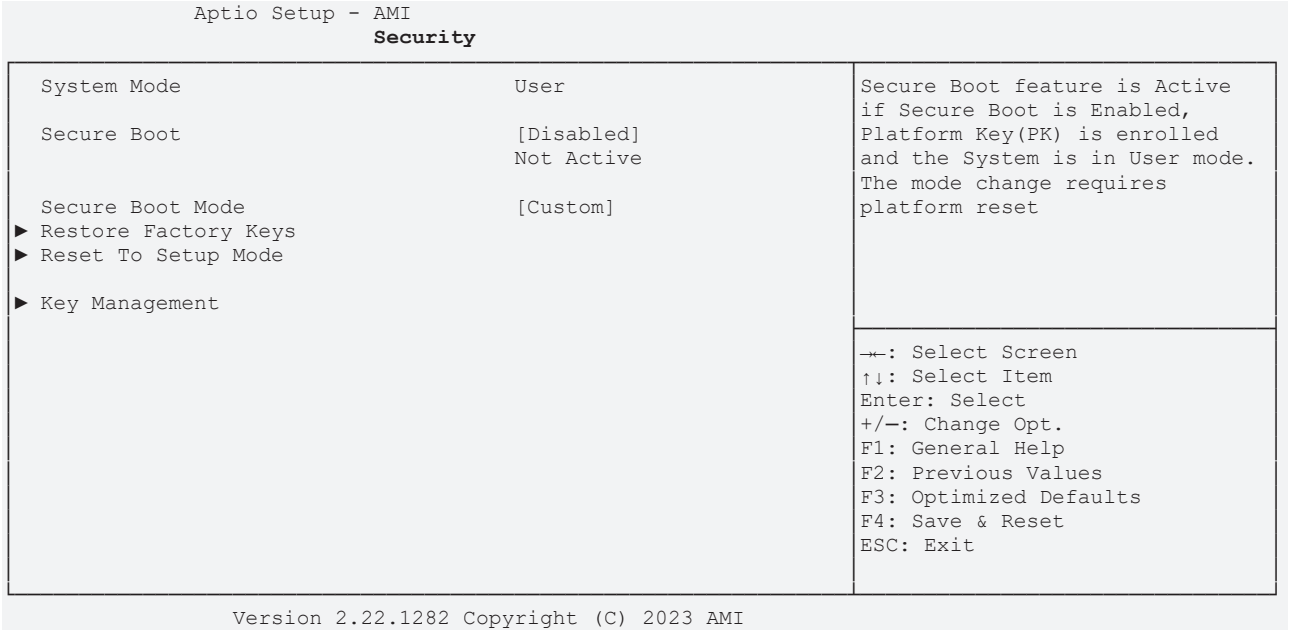
BIOS entry	Options
HD Audio Subsystem Features Configuration (ACPI)	
Audio DSP NHLT Endpoints Configuration:	
NHLT External Table	Disabled / Enabled
DMIC	Disabled / 1 / 2 / 4 Mic Array
Bluetooth	None
I2S	None
Audio DSP Feature Support:	
WoV (Wake on Voice)	Disabled / Enabled
Bluetooth Sideband	Disabled / Enabled
BT Intel HFP	None
BT Intel A2DP	None
Codec based VAD	Disabled / Enabled
DSP based Speech	None
Pre-Processing disabled	
Voice Activity Detection	Intel Wake on Voice / Windows 10 Voice Activation
Audio DSP Pre/Post-Processing Module Support:	
Waves Post-process	Disabled / Enabled
DTS	Disabled / Enabled
IntelSST Speech	Disabled / Enabled
Dolby	Disabled / Enabled
Waves Pre-process	Disabled / Enabled
Audyssey	Disabled / Enabled
Maxim Smart AMP	Disabled / Enabled
ForteMedia SAMSoft	Disabled / Enabled
Sound Research IP	Disabled / Enabled
Conexant Pre-Process	Disabled / Enabled
Conexant Smart Amp	Disabled / Enabled
Realtek Post-Process	Disabled / Enabled
Realtek Smart Amp	Disabled / Enabled
Icepower IP MFX sub module	Disabled / Enabled
Icepower IP EFX sub module	Disabled / Enabled
Icepower IP SFX sub module	Disabled / Enabled
Voice Preprocessing	Disabled / Enabled
Custom Module 'Alpha'	Disabled / Enabled
Custom Module 'Beta'	Disabled / Enabled
Custom Module 'Gamma'	Disabled / Enabled

10.5 Security CB6472



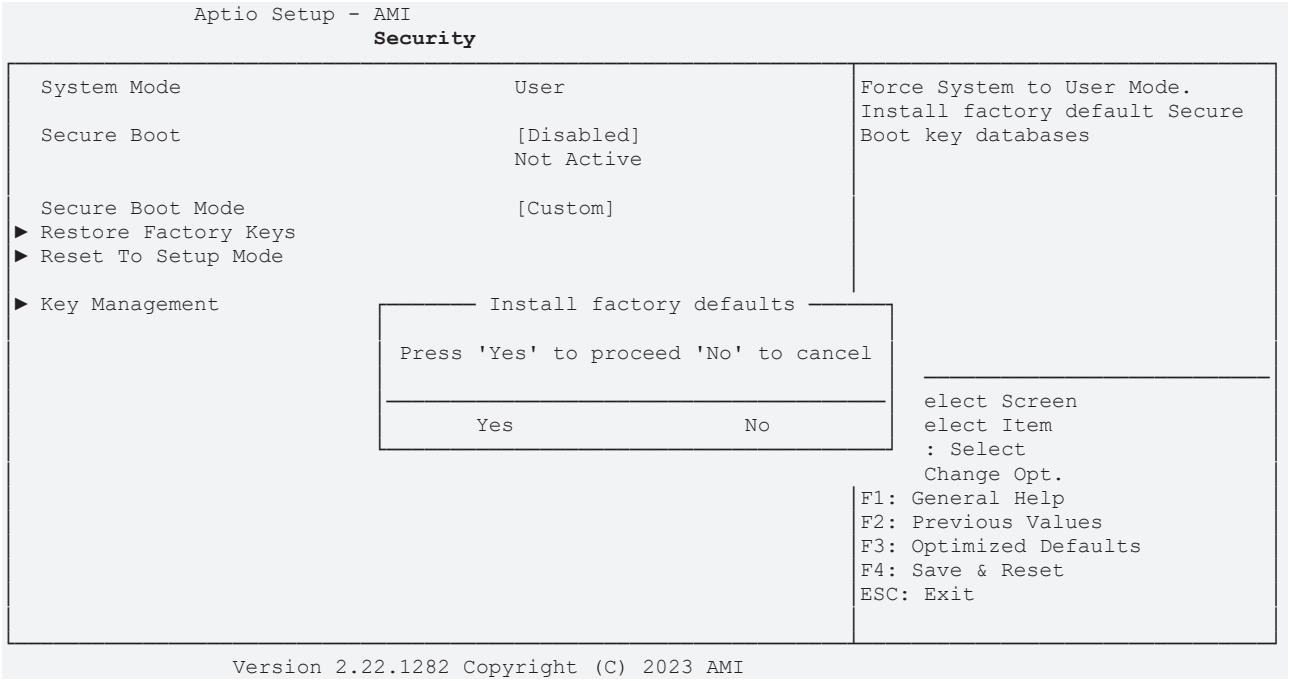
BIOS entry	Options
Password Description	
Minimum length	None
Maximum length	None
Administrator Password	An administrator password can be set here.
User Mode available	Enabled / Disabled
▶Secure Boot	Submenu see: Secure Boot [▶ 105]

10.5.1 Secure Boot



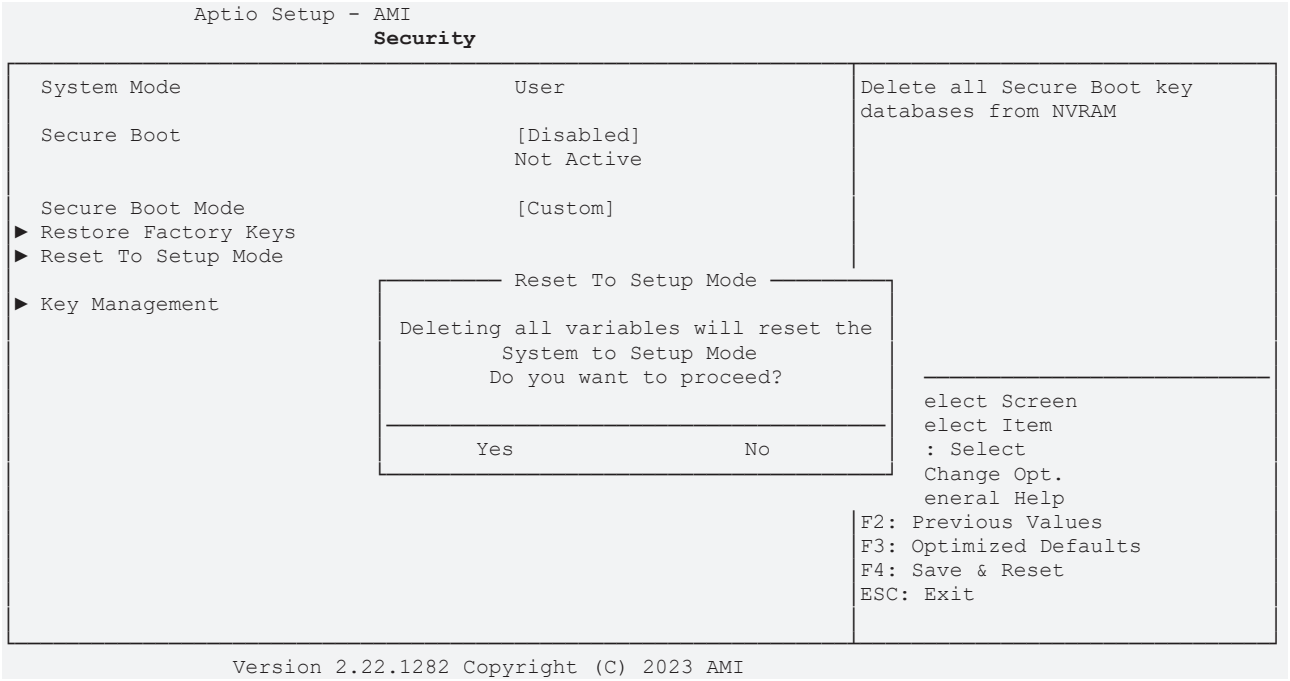
BIOS entry	Options
System Mode	None
Secure Boot	Disabled / Enabled Not Active
Secure Boot Mode	Custom / Standard
►Restore Factory Keys	Submenu see: Restore Factory Keys [▶ 106]
►Reset To Setup Mode	Submenu see: Reset To Setup Mode [▶ 107]
►Key Management	Submenu see: Key Management [▶ 108]

10.5.1.1 Restore Factory Keys



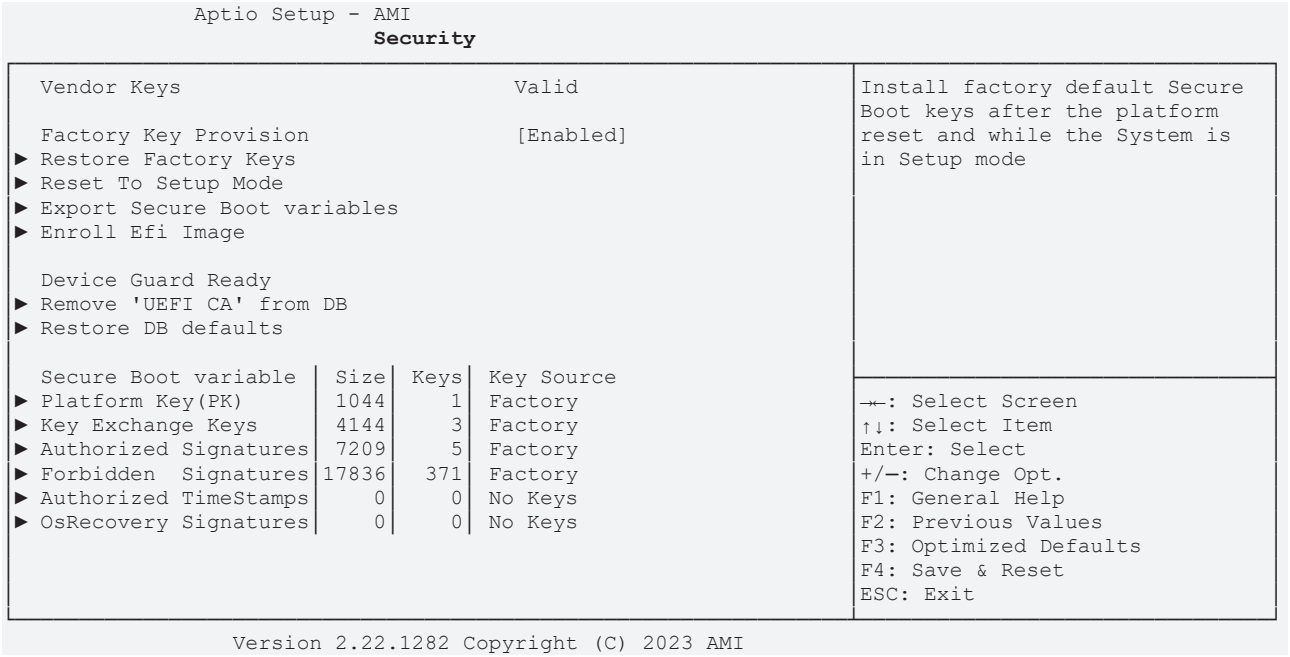
BIOS entry	Options
System Mode	None
Secure Boot	Disabled / Enabled
Secure Boot Mode	Custom / Standard
Restore Factory Keys	Install factory defaults, see box

10.5.1.2 Reset To Setup Mode



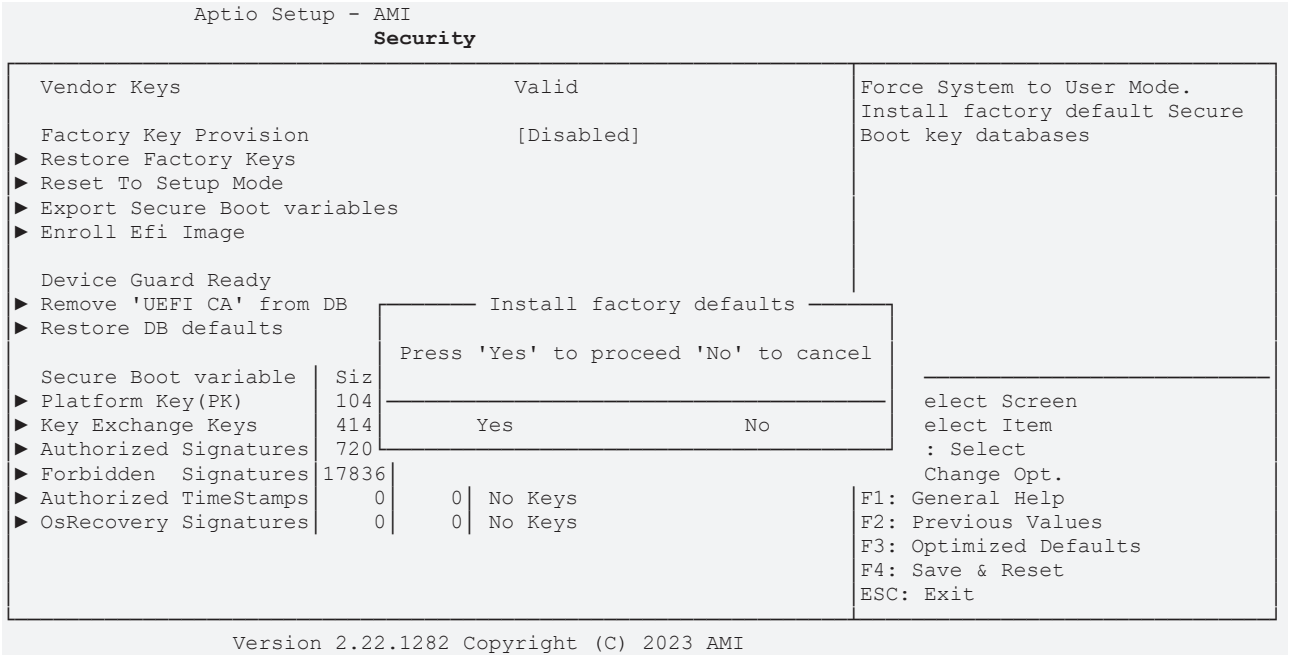
BIOS entry	Options
System Mode	None
Secure Boot	Disabled / Enabled Not Active
Secure Boot Mode	Custom / Standard
Reset To Setup Mode	Reset To Setup Mode (see box)

10.5.1.3 Key Management



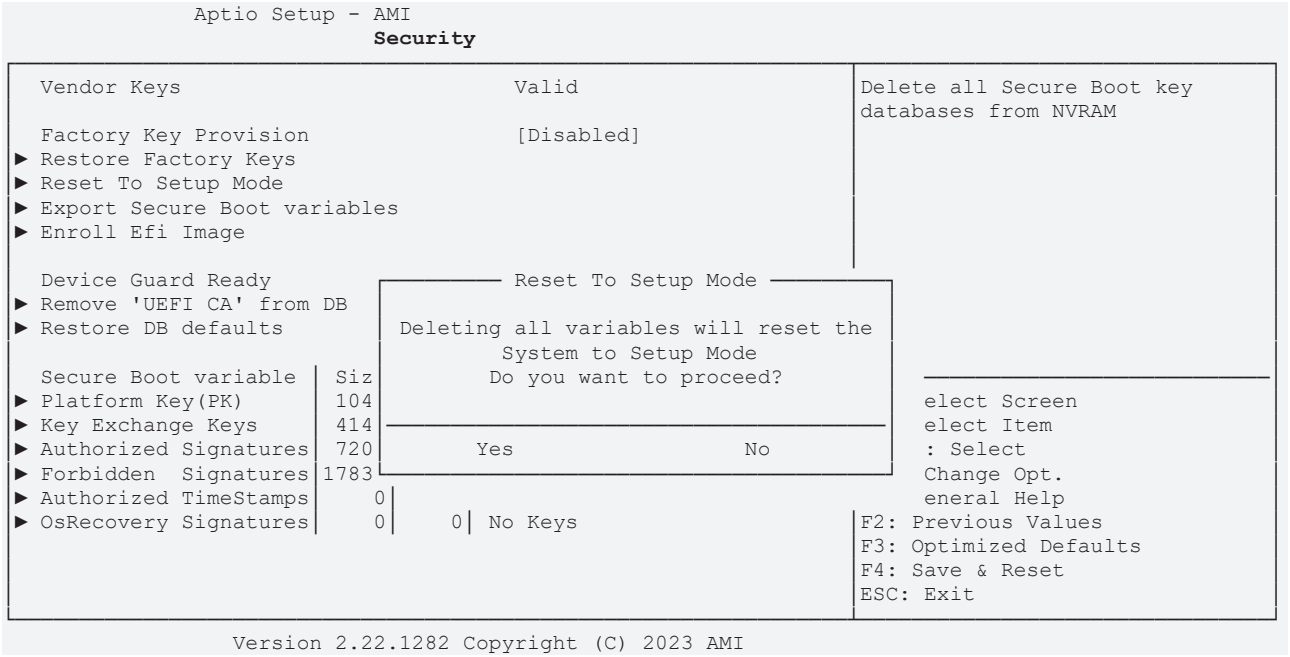
BIOS entry	Options
Vendor Keys	None
Factory Key Provision	Disabled / Enabled
Restore Factory Keys	Submenu see: Restore Factory Keys [▶ 109]
Reset To Setup Mode	Submenu see: Reset To Setup Mode [▶ 110]
Export Secure Boot variables	Submenu see: Export Secure Boot variables [▶ 111]
Enroll Efi Image	Submenu see: Enroll Efi Image [▶ 111]
Device Guard Ready	
Remove ’UEFI CA’ from DB	Submenu see: Remove 'UEFI CA' from DB [▶ 112]
Restore DB defaults	Submenu see: Restore DB defaults [▶ 113]
Secure Boot variables	
PlatformKey(PK)	Press enter key
Key Exchange Keys	Press enter key
Authorized Signatures	Press enter key
Forbidden Signatures	Press enter key
Authorized TimeStamps	Press enter key
OsRecovery Signatures	Press enter key

10.5.1.3.1 Restore Factory Keys



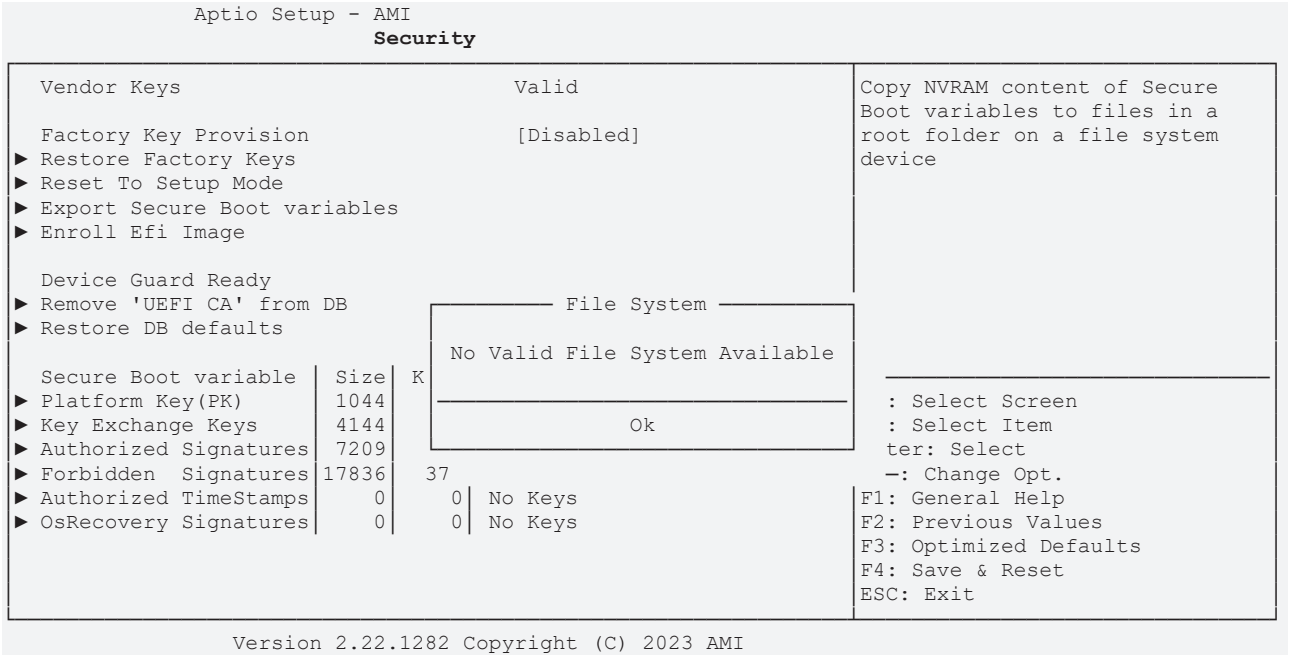
BIOS entry	Options
Vendor Keys	None
Restore Factory Keys	See box

10.5.1.3.2 Reset To Setup Mode



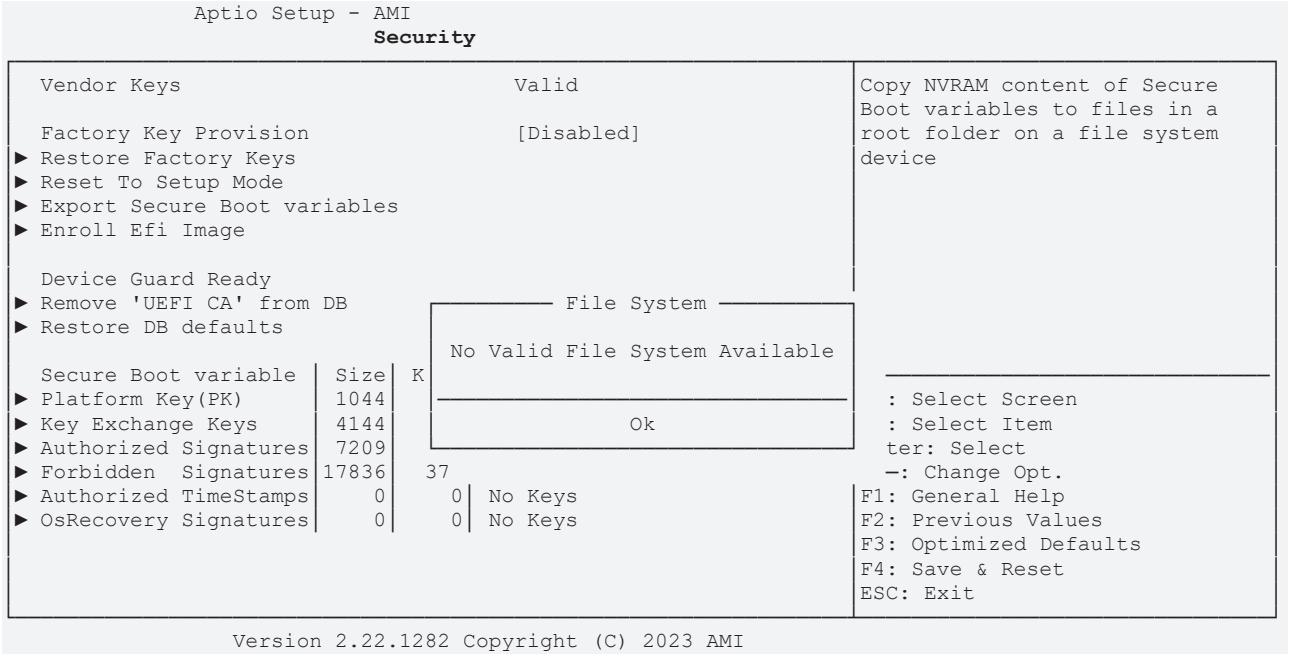
BIOS entry	Options
Vendor Keys	None
Reset To Setup Mode	See box

10.5.1.3.3 Export Secure Boot variables



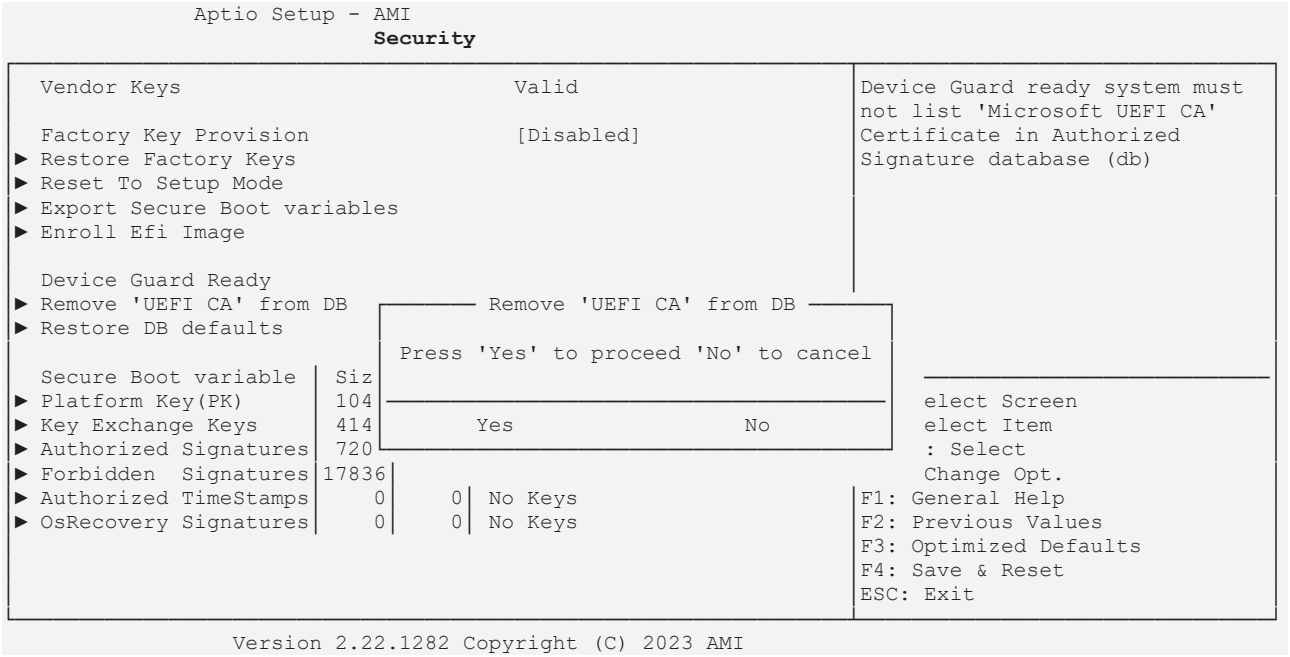
BIOS entry	Options
Vendor Keys	None
Export Secure Boot variables	See box

10.5.1.3.4 Enroll Efi Image



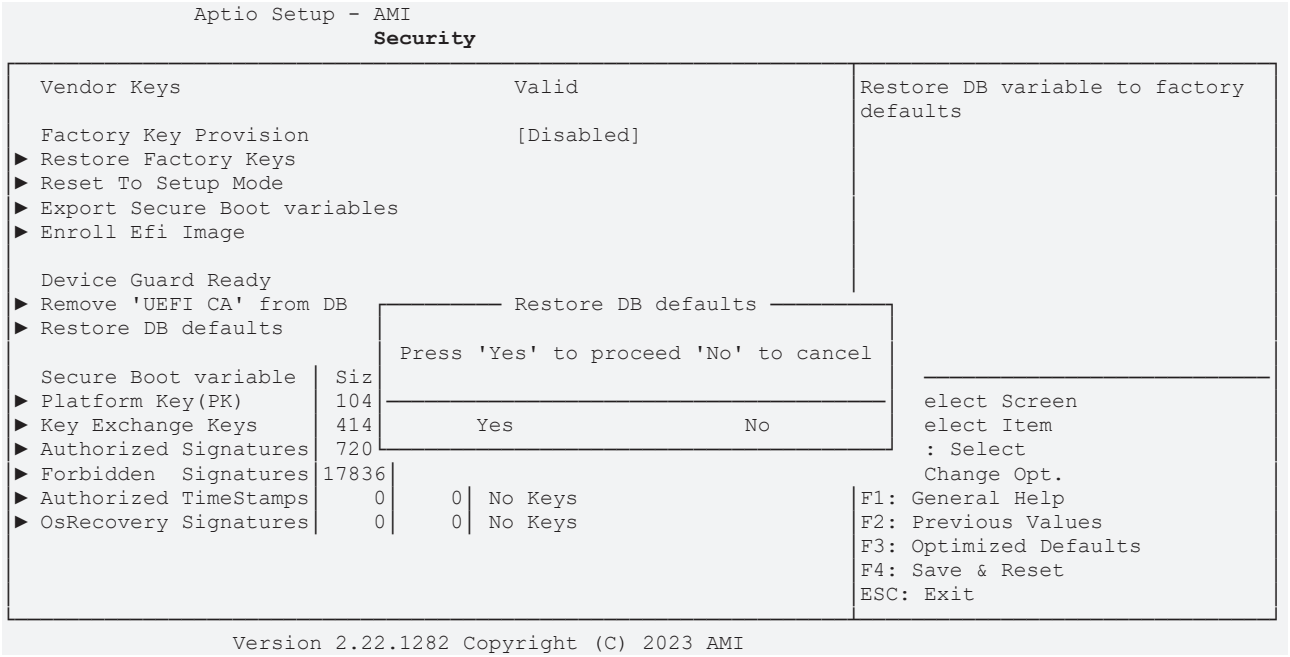
BIOS entry	Options
Vendor Keys	None
Enroll Efi Image	See box

10.5.1.3.5 Remove UEFI CA from DB



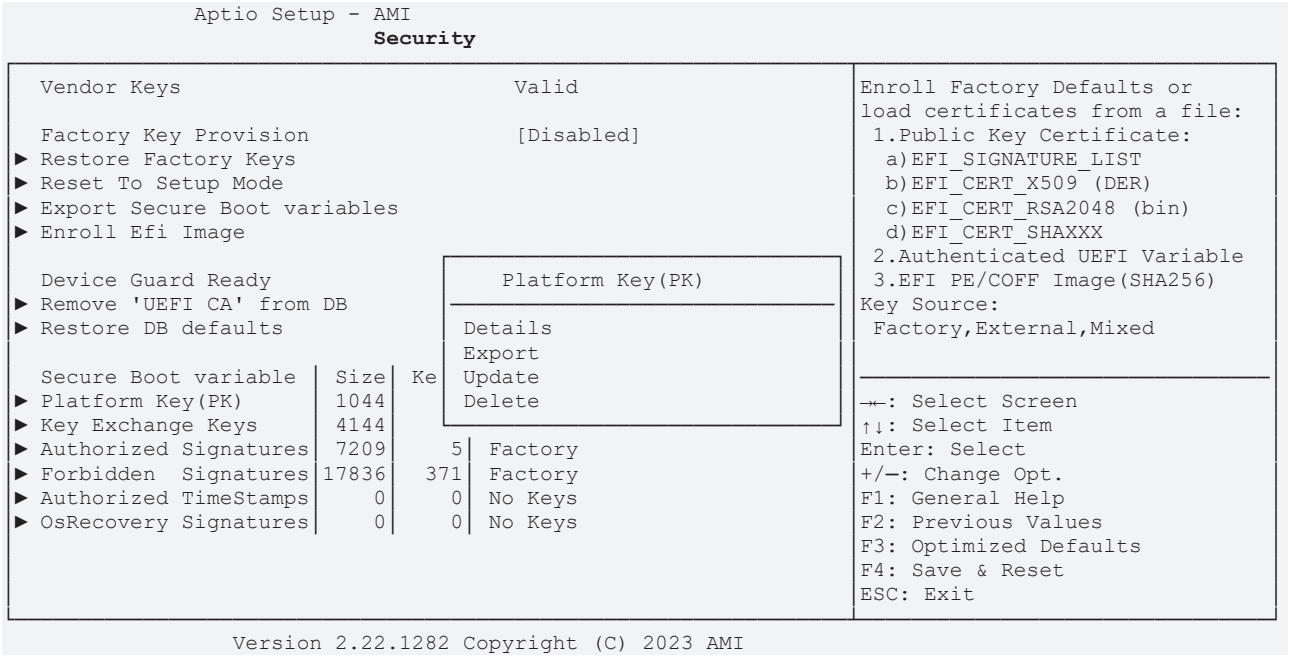
BIOS entry	Options
Vendor Keys	None
Remove ‘UEFI CA‘ from DB	See box

10.5.1.3.6 Restore DB defaults



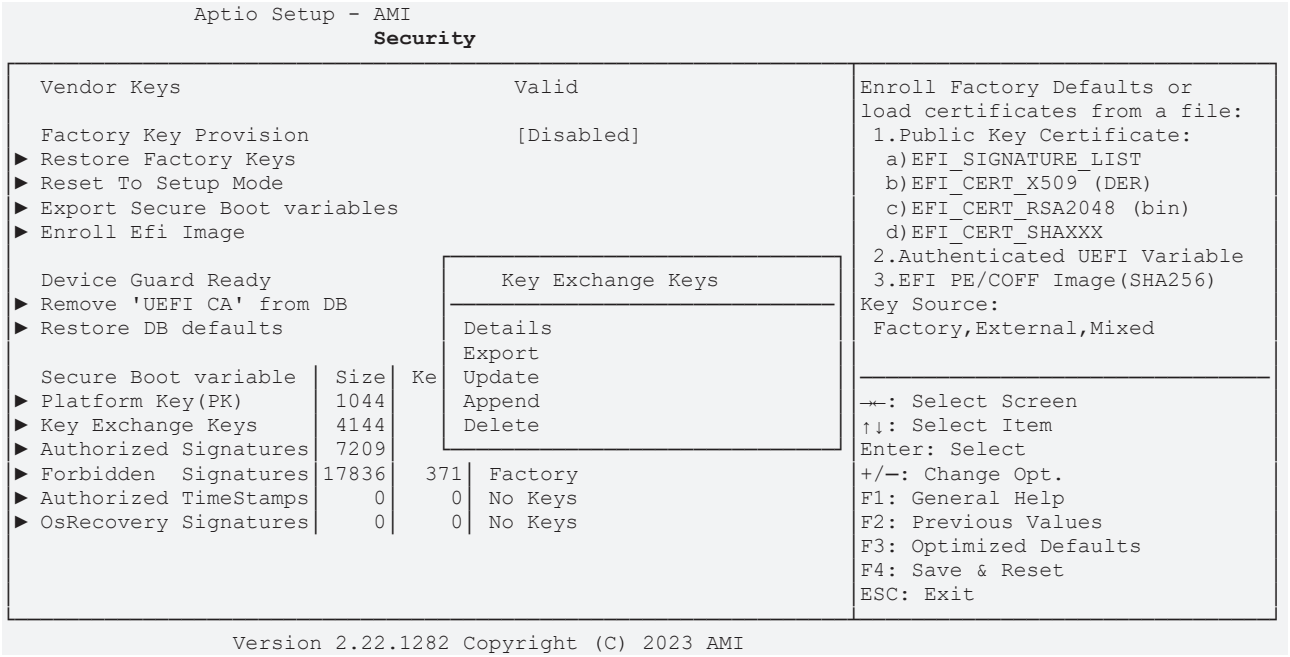
BIOS entry	Options
Vendor Keys	None
Restore DB Faults	See box

10.5.1.3.7 Platform Key (PK)



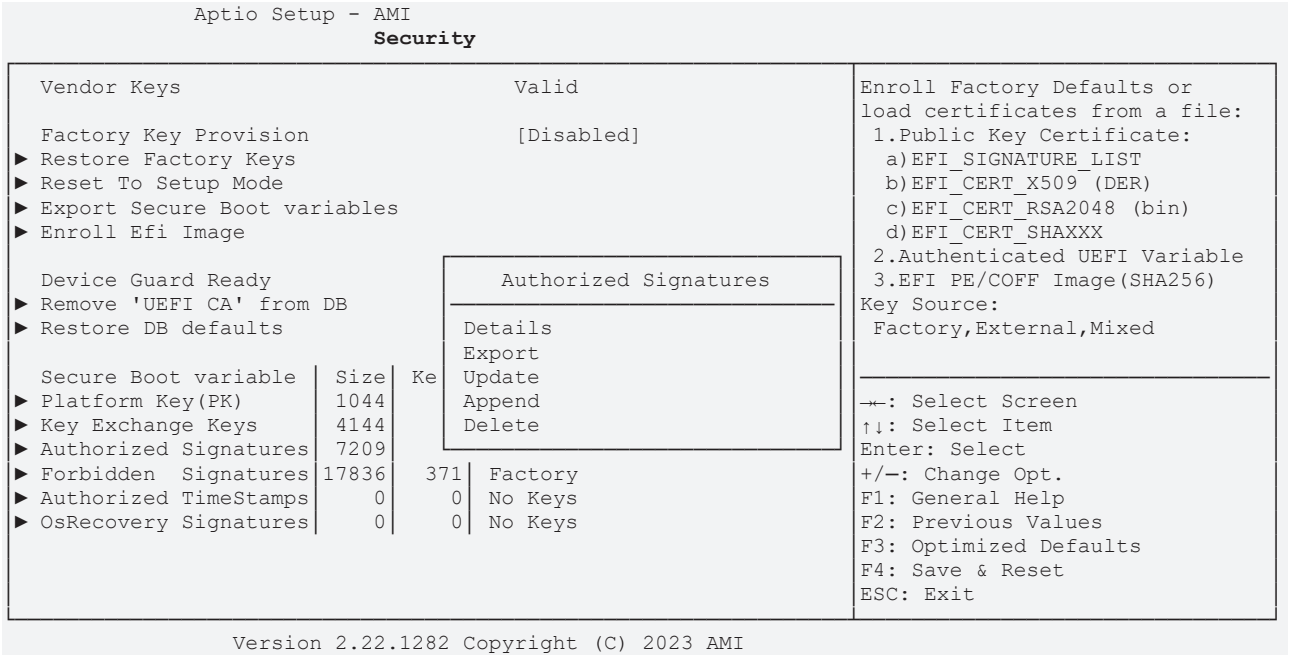
BIOS entry	Options
Vendor Keys	None
Platform Key (PK)	See box

10.5.1.3.8 Key Exchange Keys



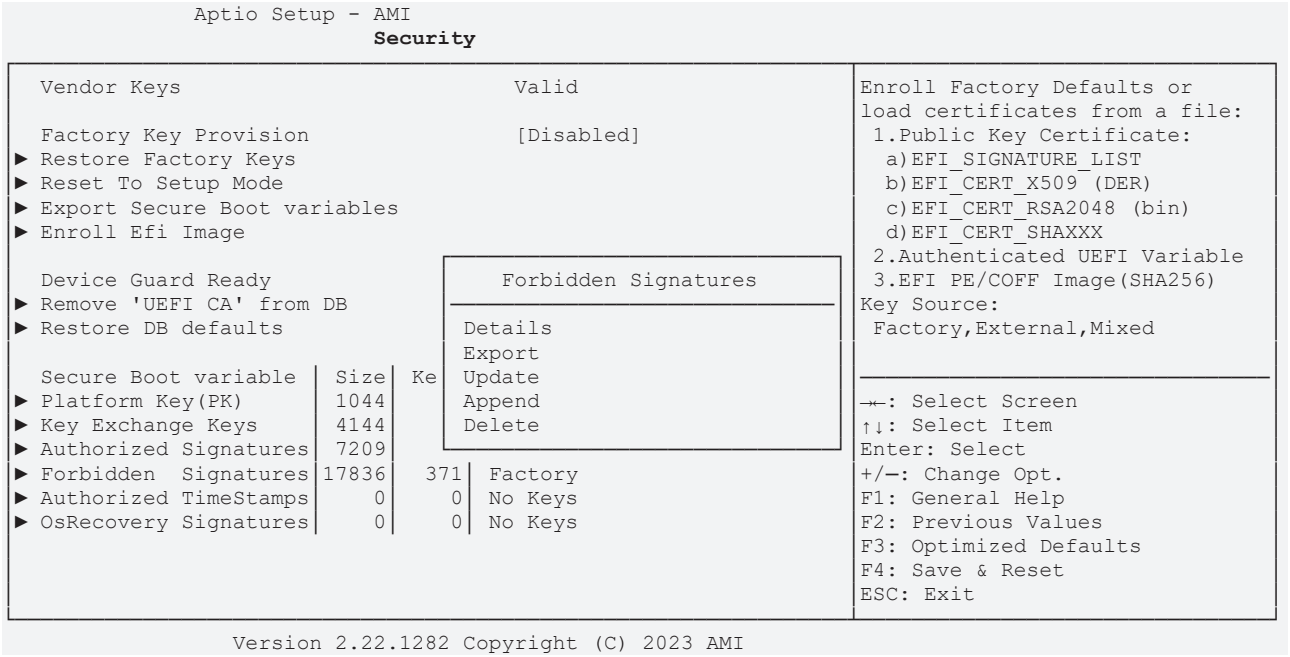
BIOS entry	Options
Vendor Keys	None
Key Exchange Keys	See box

10.5.1.3.9 Authorized Signatures



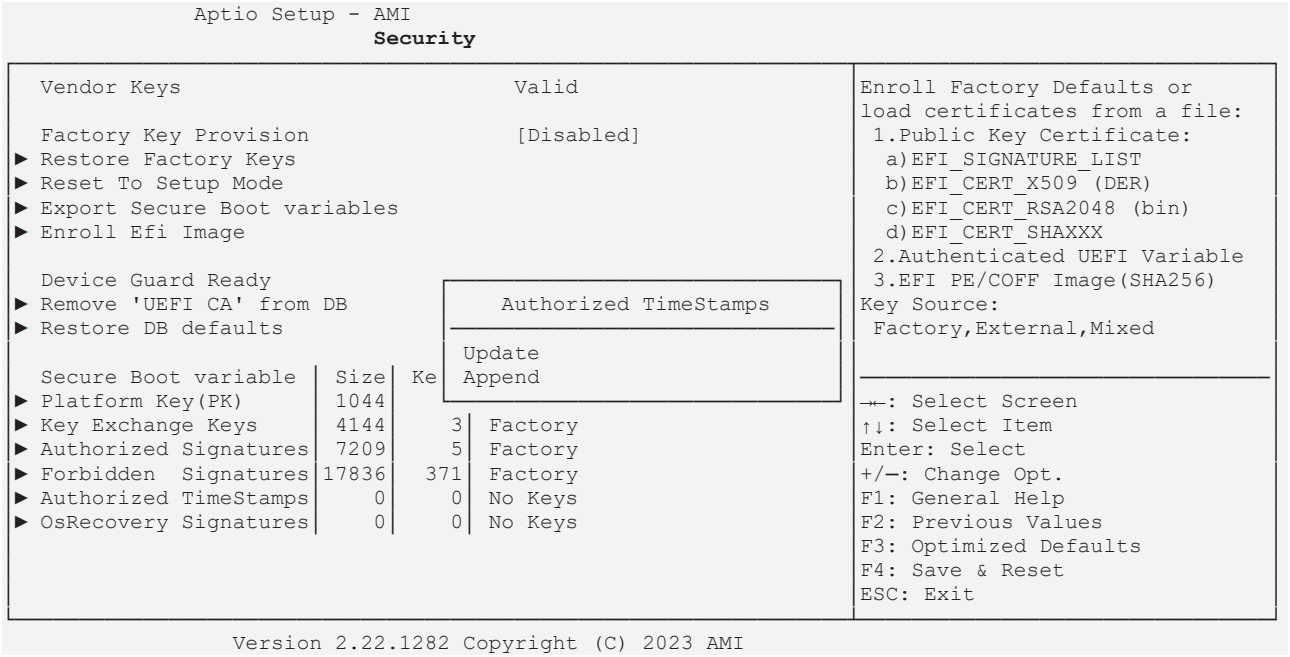
BIOS entry	Options
Vendor Keys	None
Authorized Signatures	See box

10.5.1.3.10 Forbidden Signatures



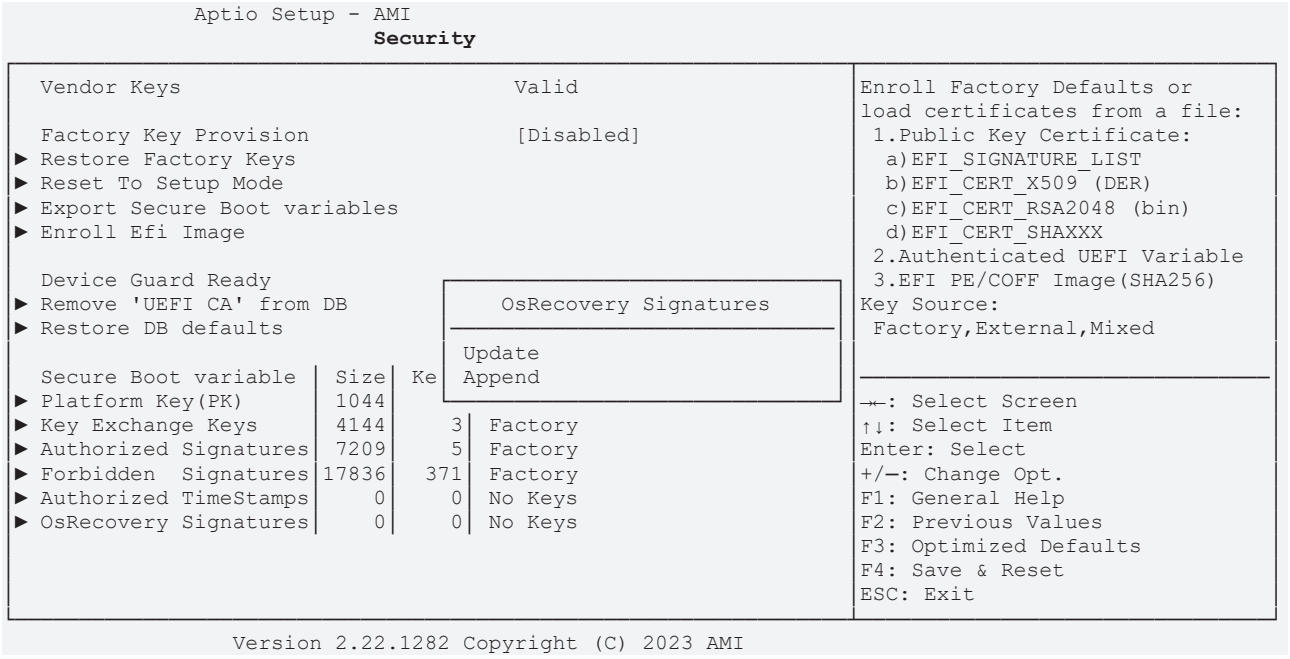
BIOS entry	Options
Vendor Keys	None
Forbidden Signatures	See box

10.5.1.3.11 Authorized TimeStamps



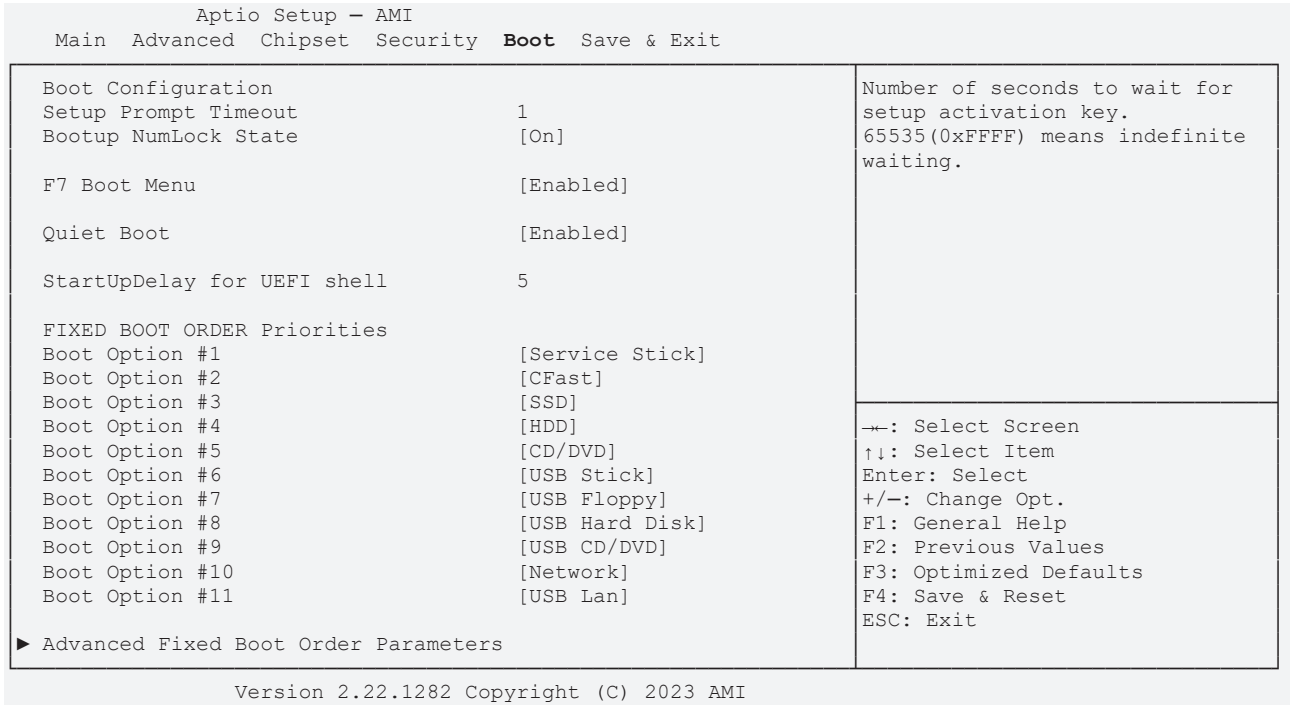
BIOS entry	Options
Vendor Keys	None
Authorized TimeStamps	See box

10.5.1.3.12 OsRecovery Signatures



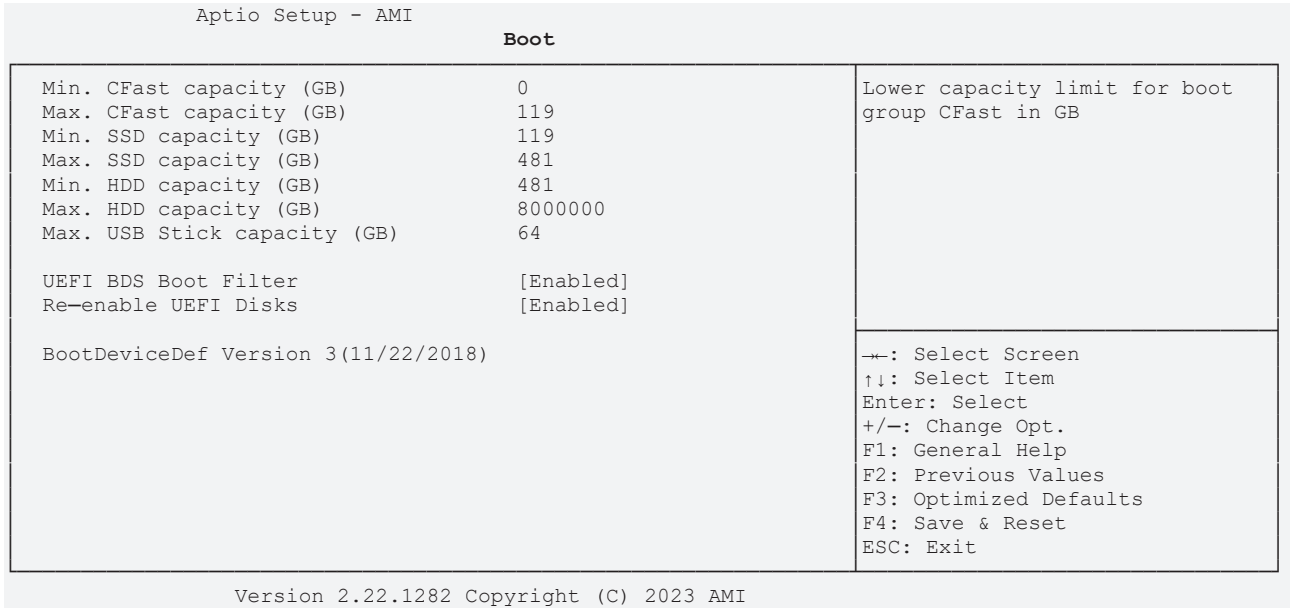
BIOS entry	Options
Vendor Keys	None
OsRecovery Signatures	See box

10.6 Boot CB6472



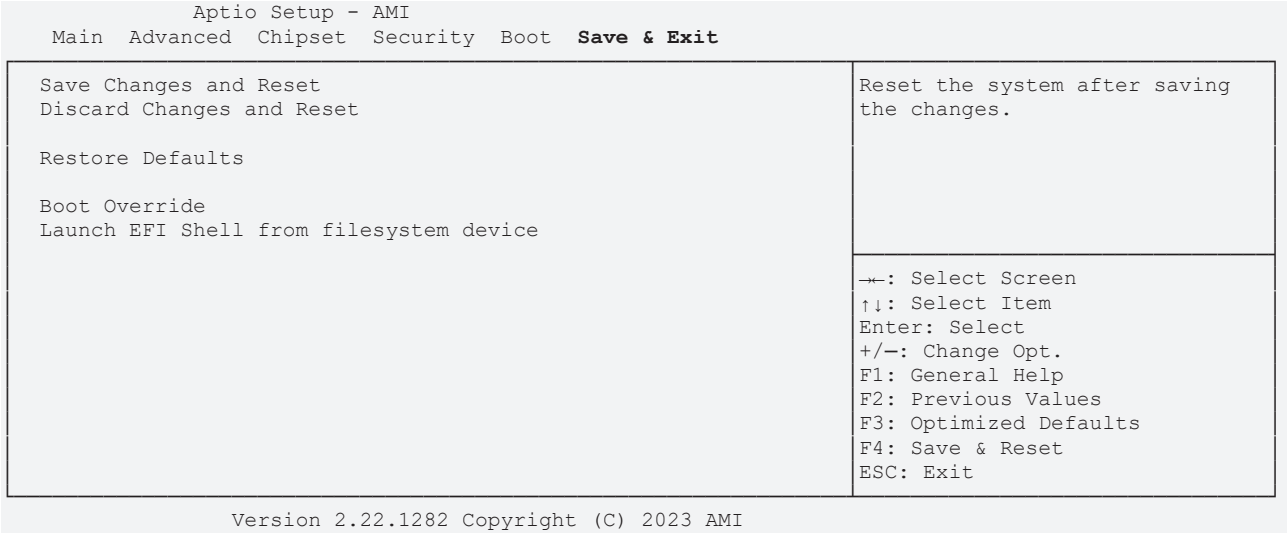
BIOS entry	Options
Boot Configuration	
Setup Prompt Timeout	None
Bootup NumLok State	On / Off
F7 Boot Menu	Enabled / Disabled
Quiet Boot	Enabled / Disabled
StartUpDelay for UEFI shell	None
Fixed Boot Order Priorities	
Boot Option #1 - 11	Here you can set the order of the boot media to be used.
▶Advanced Fixed Boot Order Parameters	Submenu see: Advanced Fixed Boot Order Parameters [▶ 121]

10.6.1 Advanced Fixed Boot Order Parameters



BIOS entry	Options
Min. CFast capacity (GB)	None
Max. CFast capacity (GB)	None
Min. SSD capacity (GB)	None
Max. SSD capacity (GB)	None
Min. HDD capacity (GB)	None
Max. HDD capacity (GB)	None
Max. USB Stick capacity (GB)	None
UEFI BDS Boot Filter	Enabled / Disabled
Re-enable UEFI Disks	Enabled / Disabled

10.7 Save & Exit CB6472



BIOS entry	Options
Save Changes and Reset	
Discard Changes and Reset	Press enter key
Restore Optimized Defaults	Press enter key
Boot Override	
Launch EFI Shell from filesystem device	Press enter key

10.8 BIOS update

The "DecdFlsh" program and a bootable medium with the latest BIOS version are used if the BIOS needs to be updated. When doing this it is important to start the program from a DOS environment without a virtual memory manager such as "EMM386.EXE". If such a memory manager is loaded, the program will abort with an error message or cause a crash.

DecdFlsh is a program for the automatic updating of the BIOS on all boards with AMI-BIOS. All files contained in the zip file must be unpacked into a directory, from where

```
DecdFlsh Bios-Dateiname
```

calling takes place. The name of the BIOS file and its length are checked. The BIOS will now be programmed.

The system must not be interrupted during the flashing process, as otherwise the update will abort and the BIOS on the board will be destroyed. The Flash procedure takes about 75 seconds. The necessary firmware update takes place automatically.

NOTICE

Risk of damage due to incorrect update procedure!

If the BIOS update is performed incorrectly, the board may become unusable. Therefore a BIOS update should only be done if the corrections / additions that the new BIOS version brings with it are really needed.

Before a planned BIOS update, it is essential to ensure that the BIOS file to be reloaded is really released for exactly this board and for exactly this board version. If an inappropriate file is used, the board will inevitably not boot afterwards.

11 Mechanical drawings

Dimensions

All dimensions are in mm.

11.1 PCB: Dimensions

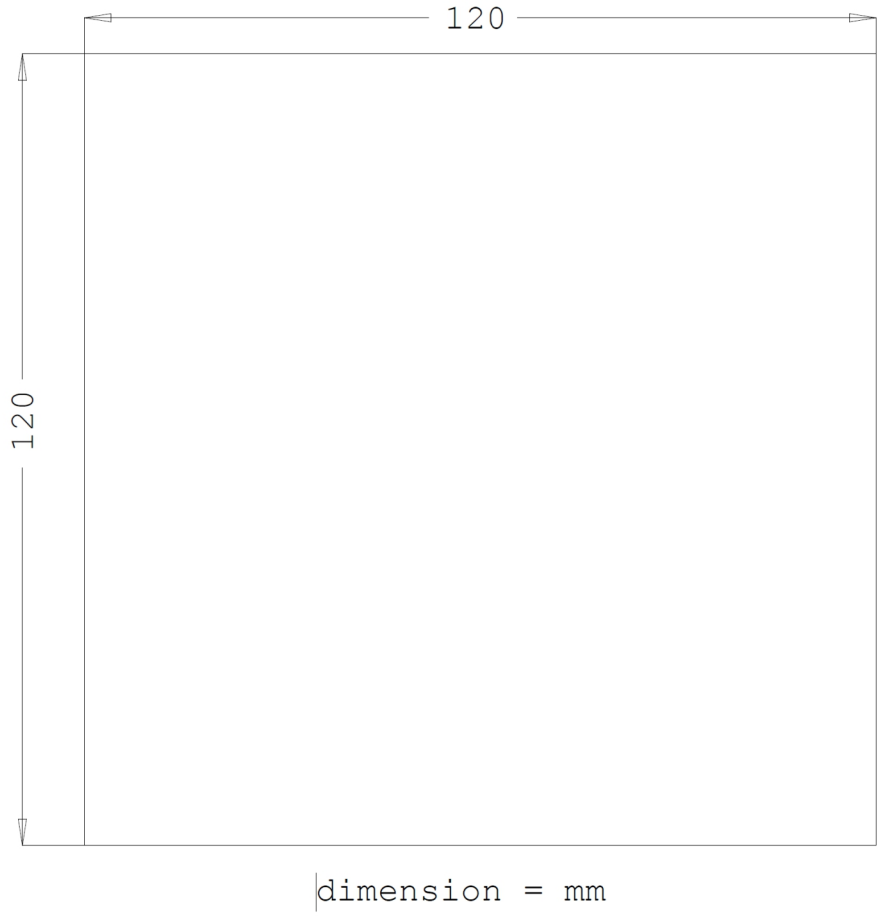


Fig. 12: CB6472-MZ

11.2 PCB: Holes

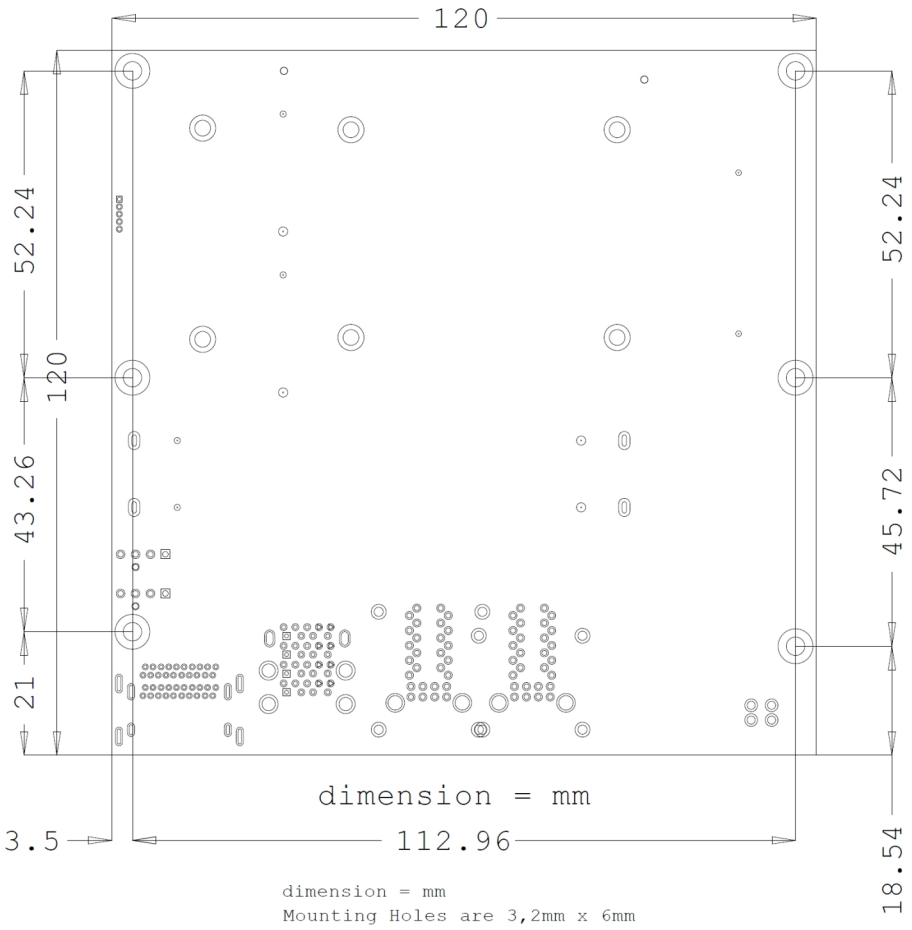


Fig. 13: CB6472-MZ MH

12 Technical data

12.1 Electrical data

Power supply	
Board	24 VDC power supply (+20 % / - 15 %)
RTC	≥3 A
Power	
Transformer	95 W continuous load 150 W peak load
Current consumption	
RTC	≤ 10 µm

12.2 Environmental conditions

Temperature range	
Operating	0 °C ... +60 °C (extended temperature range on request)
Storage	-25 °C ... +85 °C
Shipping	-25 °C ... +85 °C, for packed boards
Temperature changes	
Operating	0.5 °C per minute, 7.5 °C in 30 minutes
Storage	1.0 °C per minute
Shipping	1.0 °C per minute, for packed boards
Relative humidity	
Operating	5% ... 85% (non-condensing)
Storage	5% ... 95% (non-condensing)
Shipping	5% ... 100% (non-condensing), for packed boards
Impact	
Operating	150 m/s², 6 ms
Storage	400 m/s², 6 ms
Shipping	400 m/s², 6 ms, for packed boards
Vibration	
Operating	10 ... 58 Hz, amplitude 0.075 mm
Storage	5 ... 9 Hz, 3.5 mm amplitude 9 ... 500 Hz, 10 m/s²
Shipping	5 ... 9 Hz, 3.5 mm amplitude 9 ... 500 Hz, 10 m/s², for packed boards

Note on impact and vibration resistance

The specifications for impact and vibration resistance refer only to the motherboard itself without heat sink, memory module, cabling, etc.

12.3 Technical specifications

The board is specified for an ambient temperature range of 0 °C to +60 °C (extended temperature range on request). In addition, care must be taken that the temperature of the processor die does not exceed 100 °C. To ensure this a suitable cooling concept must be implemented that is oriented to the maximum power consumption of the processor/chipset. It must also be ensured that any existing controllers are included in the cooling concept. The power consumption of these function blocks may be of the same order of magnitude as the power consumption of the processor. The board is prepared with suitable holes for the use of modern cooling solutions. We have a series of compatible cooling components in our range. Your distributor will be pleased to assist you in selecting suitable solutions.

NOTICE

Prevent the maximum die temperature being exceeded!

It is the end customer's responsibility to ensure that the die temperature of the processor does not exceed 100 °C! Continuous overheating can destroy the board!

If the temperature exceeds 100 °C, the ambient temperature needs to be reduced. Ensure sufficient air circulation if necessary.

13 Support and Service

Beckhoff and their partners around the world offer comprehensive support and service, making available fast and competent assistance with all questions related to Beckhoff products and system solutions.

Beckhoff's branch offices and representatives

Please contact your Beckhoff branch office or representative for local support and service on Beckhoff products!

The addresses of Beckhoff's branch offices and representatives round the world can be found on our internet page: www.beckhoff.com

You will also find further documentation for Beckhoff components there.

Beckhoff Support

Support offers you comprehensive technical assistance, helping you not only with the application of individual Beckhoff products, but also with other, wide-ranging services:

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- design, programming and commissioning of complex automation systems
- and extensive training program for Beckhoff system components

Hotline:	+49 5246 963-157
e-mail:	support@beckhoff.com

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The Beckhoff Service Center supports you in all matters of after-sales service:

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- repair service
- spare parts service
- hotline service

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e-mail:	service@beckhoff.com

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14 Appendix I: Post Codes

During the boot phase, the BIOS generates a series of status messages (so-called "POST Codes"), which can be output with the help of a suitable reading device (POST Code card). The meanings of the POST Codes are explained in the document "Aptio™ 5.x Status Codes" from American Megatrends®, which is available from the website http://www.ami.com. In addition, the following OEM POST Codes are output:

Code	Description
87h	BIOS-API started
88h	PCA9535 started
89h	PWRCTRL firmware started

15 Appendix II: Resources

15.1 Interrupt CB6472

The system BIOS determines the interrupt requests (IRQs) for all devices that request interrupts. In the operating system, interrupts can be dynamically forwarded to IRQs and can support a reassignment of IRQs if there is a conflict with the current use of the interrupt.

Further information can be found in chipset manual. Specifications and documents

15.2 PCI-Devices CB6472

The PCI devices listed here all exist on the board, including those that are detected and configured by the BIOS. Due to the BIOS setup settings it may be the case that various PCI devices or functions of devices are not activated. If devices are deactivated, the bus numbers of other devices may change as a result.

Bus	Dev.	Fct.	Controller / Slot
00	00	00	Host bridge ID 3E35
00	02	00	VGA controller ID 3EA0
00	04	00	Data acquisition/signal processing controller ID 1903
00	08	00	System device ID 1911
00	12	00	Data acquisition/signal processing controller ID 9DF9
00	14	00	XHCI USB controller ID 9DED
00	14	02	RAM controller ID 9DEF
00	16	00	Communication device ID 9DE0
00	17	00	RAID controller ID 282A
00	1C	00	PCI-to-PCI bridge (PCIE) ID 9DB8
00	1C	07	PCI-to-PCI bridge (PCIE) ID 9DBF
00	1D	00	PCI-to-PCI bridge (PCIE) ID 9DB0
00	1D	03	PCI-to-PCI bridge (PCIE) ID 9DB3
00	1F	00	ISA bridge ID 9D84
00	1F	03	HD audio device ID 9DC8
00	1F	04	SMBus controller ID 9DA3
00	1F	05	Controller ID 9DA4
00	1F	06	Ethernet controller ID 15BD
02	00	00	Ethernet controller (PCIE) ID 1533
03	00	00	Mass storage controller (PCIE) ID 5008
04	00	00	Ethernet controller (PCIE) ID 1533

15.3 SMB-Devices CB6472

The following table lists the reserved SM-Bus device addresses in 8-bit notation.

NOTICE

These address ranges may not be used by external devices even if the component assigned in the table doesn't exist on the motherboard.

Address	Function
B0, B2, B8, BA	PWCTR3
70, 72	PostCode
34 (old B4)	CA2000-0021/23 (power supply unit)
40	PCA9535BS (16-bit I2C and SMBus, low power I/O port with interrupt)
..	SUSV

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