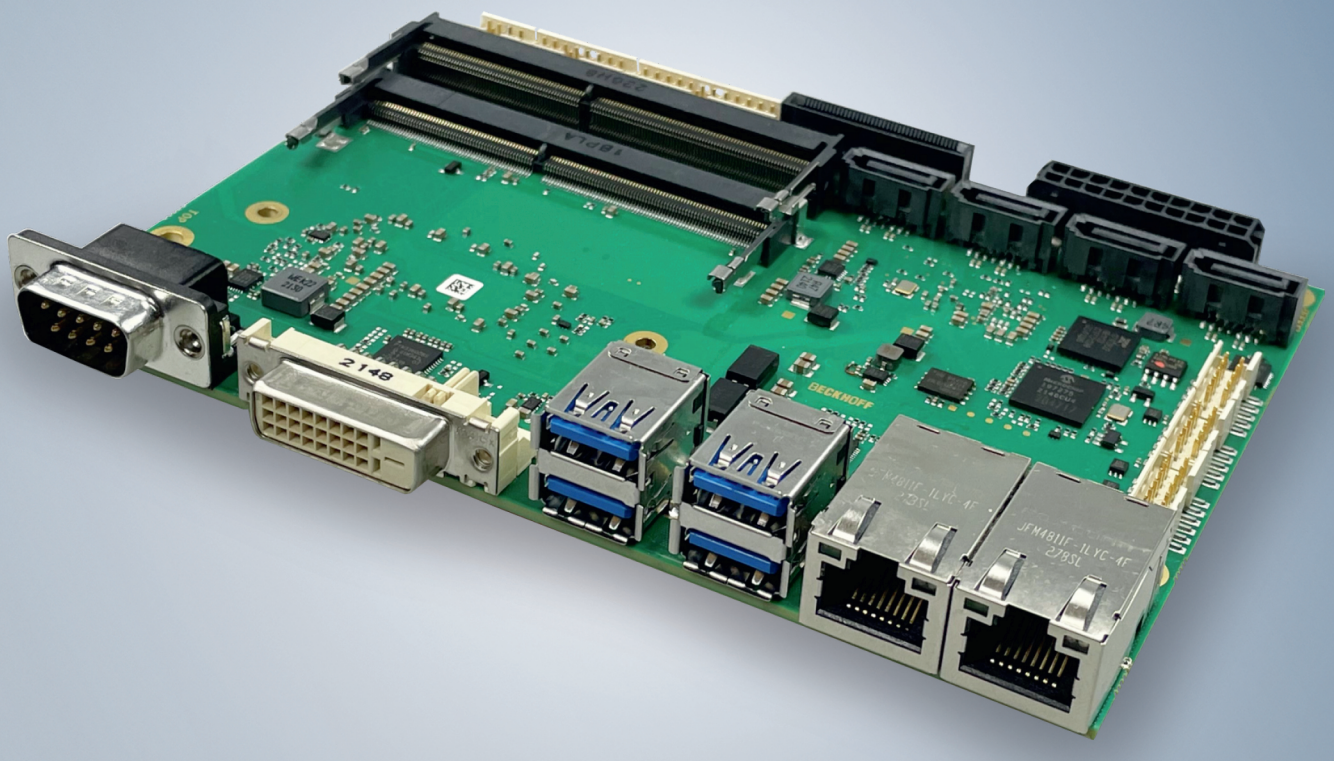
BECKHOFF New Automation Technology

Manual for | EN

CB3072

Computerboard



2024-08-13 | Version: 1.0

1 Documentation issue status

Version	Modifications
0.1	First preliminary version, G0
0.2	Block diagram and interfaces added
0.3	BIOS version 0.28 added
0.4	Cross-references and dimensional drawings added
0.5	Support and service page updated
1.0	First release, USB3.2, LAN controller i226-IT added, BIOS 0.48

2 Notes on the documentation

This description is intended exclusively for trained specialists in control and automation technology who are familiar with the applicable national standards.
For installation and commissioning of the components, it is absolutely necessary to comply with the documentation and the following notes and explanations.
It is the duty of the responsible staff to use the documentation published at the respective time of each installation and commissioning.

The responsible staff must ensure that the application or use of the products described satisfies all safety requirements, including all the relevant laws, regulations, guidelines, and standards.

Origin of the document

This documentation was originally written in German. All other languages are derived from the German original.

Disclaimer

The documentation has been prepared with care. The products described are, however, constantly under development.
We reserve the right to revise and change the documentation at any time and without notice.
No claims to modify products that have already been supplied may be made on the basis of the data, diagrams, and descriptions in this documentation.

Trademarks

Beckhoff®, TwinCAT®, TwinCAT/BSD®, TC/BSD®, EtherCAT®, EtherCAT G®, EtherCAT G10®, EtherCAT P®, Safety over EtherCAT®, TwinSAFE®, XFC®, XTS® and XPlanar® are registered and licensed trademarks of Beckhoff Automation GmbH.
Other designations used in this publication may be trademarks whose use by third parties for their own purposes could violate the rights of the owners.

Patents

The EtherCAT Technology is covered by the following patent applications and patents, without this constituting an exhaustive list:
EP1590927, EP1789857, EP1456722, EP2137893, DE102015105702
and similar applications and registrations in several other countries.

EtherCAT® is registered trademark and patented technology, licensed by Beckhoff Automation GmbH, Germany

Copyright

3 Safety instructions

Safety regulations

Please observe the following safety instructions and explanations!
Product-specific safety instructions can be found on following pages or in the mounting, wiring, commissioning areas, etc.

Exclusion of liability

All of the components are supplied in specific hardware and software configurations depending on the application requirements. Modifications to hardware or software configurations other than those described in the documentation are not permitted, and nullify the liability of Beckhoff Automation GmbH & Co. KG.

Personnel qualification

This description is only intended for trained specialists in control, automation, and drive technology who are familiar with the applicable national standards.

Description of symbols

In this documentation the following symbols are used with an accompanying safety instruction or note. The safety instructions must be read carefully and followed without fail!

⚠ DANGER

Serious risk of injury!

Failure to follow the safety instructions associated with this symbol directly endangers human life and health!

⚠ WARNING

Risk of injury!

Failure to follow the safety instructions associated with this symbol endangers human life and health!

⚠ CAUTION

Personal injuries!

Failure to follow the safety instructions associated with this symbol can lead to physical injuries!

NOTICE

Damage to the environment or devices

Failure to follow the instructions associated with this symbol can lead to damage to the environment or equipment.

Tip or pointer

This symbol indicates information that contributes to better understanding.

This symbol indicates important information regarding UL approval.

Intended use

The CB3072 Computer Board was designed and developed exclusively for configuration in automation processes. To that end the board is equipped with external and internal interfaces in order to acquire or output digital or analog signals or forward them to higher-level components.

Any other use is regarded as inappropriate.

The specified limits for electrical and technical data must be adhered to.

4 Notes on information security

The products of Beckhoff Automation GmbH & Co. KG (Beckhoff), insofar as they can be accessed online, are equipped with security functions that support the secure operation of plants, systems, machines and networks. Despite the security functions, the creation, implementation and constant updating of a holistic security concept for the operation are necessary to protect the respective plant, system, machine and networks against cyber threats. The products sold by Beckhoff are only part of the overall security concept. The customer is responsible for preventing unauthorized access by third parties to its equipment, systems, machines and networks. The latter should be connected to the corporate network or the Internet only if appropriate protective measures have been set up.

In addition, the recommendations from Beckhoff regarding appropriate protective measures should be observed. Further information regarding information security and industrial security can be found in our https://www.beckhoff.com/secguide.

Beckhoff products and solutions undergo continuous further development. This also applies to security functions. In light of this continuous further development, Beckhoff expressly recommends that the products are kept up to date at all times and that updates are installed for the products once they have been made available. Using outdated or unsupported product versions can increase the risk of cyber threats.

To stay informed about information security for Beckhoff products, subscribe to the RSS feed at https://www.beckhoff.com/secinfo.

5 Overview

5.1 Properties

The CB3072 is a highly complex 3.5-inch board. It is based on Intel®'s Tiger Lake-H processors of the Core™, Celeron™ family in connection with the RM590E chipset.

State-of-the-art, energy-saving DDR4 technology enables a memory extension of up to 64 GB (DDR4-3200) using SO-DIMM260. In addition to a PCI express bus, further peripheral devices are available, such as HDMI or DisplayPort via I-PEX, 4x SATA with up to 6 Gbit/s, DVI/HDMI, 11x USB (including 5x USB3.0), 1x 1Gbit-LAN, 1x 2.5Gbit-LAN, an external and an internal serial interface (RS232).

The input voltage is 5 V.

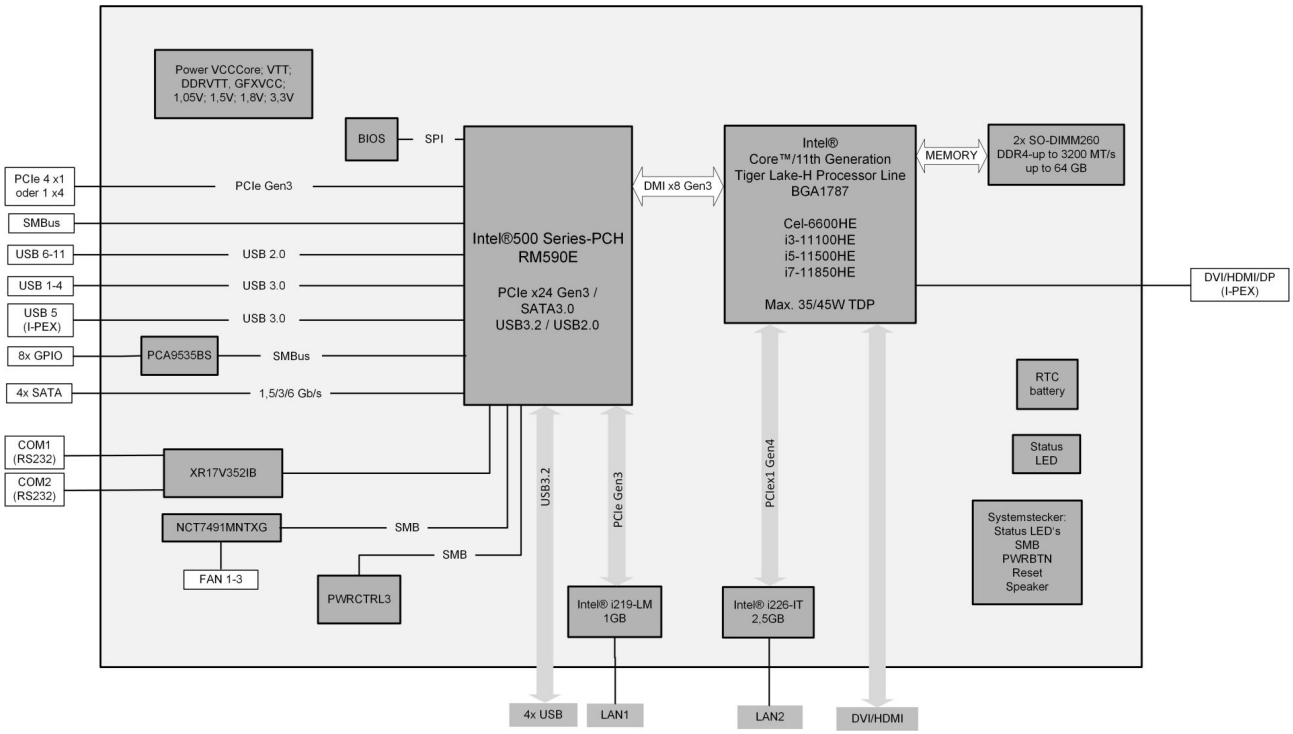


Fig. 1: Block diagram CB3072-TGL-H

5.2 List of features

CB3072	3.5-inch board
CPU	Intel® Celeron® Cel-6600HE Intel® Core™ i3-11100HE Intel®/Core™ i5-11500HE Intel®/Core™ i7-11850HE
Chipset	Intel® RM590E-PCH
Memory	2x SO-DIMM260 1.2 V DDR4-3200 Maximum memory capacity 64 GB
I/O external	1x DVI-D (DVI or HDMI 1.4) 1x LAN 1GBit, Intel® i219 1x LAN 2.5Gbit Intel® i226 4x USB3.2 1 x COM A (RS232)
I/O internal	1x I-PEX (HDMI1.4 or DP1.2 and USB3.0) 4x SATA 3.0, RAID 0/1/5/10 1x PCIe Gen3 (1x PCIe x4 or 4x PCIe x1) 6x USB2.0 8x GPIO 1x COM B (RS232)
Graphic resolution	DisplayPort: 4096x2304@60 Hz HDMI1.4: 4096x2304@60 Hz 4096x2160@24 Hz DVI: 1920x1200@60 Hz
RTC	External CMOS battery
BIOS	AMI® Aptio V
Power supply	5 V/S5 V/3.3 V/12 V
Format	102 x 147 mm

Availability of the processors

The list of features lists all the processors that can be ordered. Their actual availability depends on the manufacturer.

5.3 Specification and documents

The following documents, specifications, or webpages, in their current or most recent versions, have been used in the preparation of this manual or as additional technical documentation.

PCI specification

www.pcisig.com

PCI Express® Base Specification

www.pcisig.com

ACPI specification

www.acpi.info

ATA/ATAPI specification

www.t13.org

USB specifications

www.usb.org

SMBus specification

www.smbus.org

Intel® chip descriptions

Intel® Celeron™, Core™ Tiger Lake-H Processor Product Family datasheet

www.intel.com

Intel® chip description

i219 datasheet

i226 datasheet

www.intel.com

SMSC® chip description

SCH3114 datasheet (NDA required)

www.smsc.com

American Megatrends®

Aptio™ Text Setup Environment (TSE) User Manual

www.ami.com

American Megatrends®

Aptio™ Status Codes

www.ami.com

6 Interfaces

All the interfaces on the CB3072 are described on the following pages.

Requirement for the cabling!

The cables used must meet certain requirements for most interfaces. For example, twisted and shielded cables are necessary for a reliable USB 2.0 connection. Limitations in the maximum cable length are also no rarity. All of these interface-specific requirements can be found in the respective specifications and you should observe them accordingly.

6.1 Interface overview

The figure below shows the plug connections on the component side of the CB3072 board. The table below shows the function of the respective plug. The listed page in the manual provides you with further information on this connection. The interfaces are described clockwise, beginning with the Power Input (P1300).

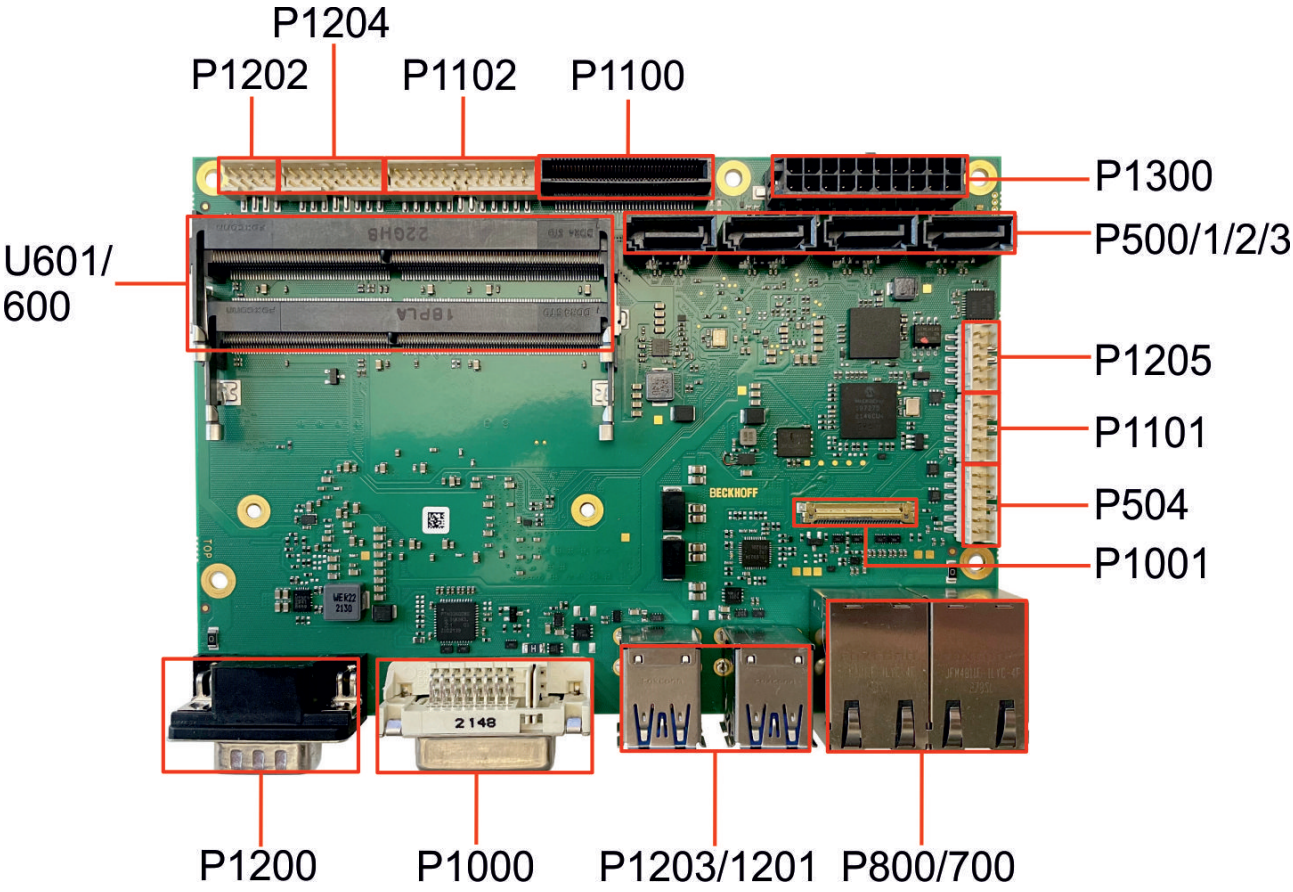


Fig. 2: CB3072 interfaces

Number	Function (designation)	Page
P1300	Power Input	See: Power input (P1300) [▶ 15]
P500/1/2/3	SATA interfaces	See: SATA interfaces (P500/1/2/3) [▶ 16]
P1205	Serial interface, internal	See: Serial interface COM2 internal (P1205) [▶ 16]
P1101	Fan connection, internal	See: Fan connections (P1101) [▶ 17]
P504	GPIO	See: GPIO (P504) [▶ 17]
P1001	Display Port IPEX	See: Display Port I-PEX (P1001) [▶ 18]
P700/800	1 Gbit LAN / 2.5 Gbit LAN	See: LAN 1 Gbit (P700) / LAN 2.5 Gbit (P800) [▶ 19]
P1201/1203	USB 3.2	See: USB 3.2 external (P1201/P1203) [▶ 21]
P1000	DVI-D	See: DVI-D (P1000) [▶ 22]
P1200	COM A, external	See: Serial interface COM1 (P1200) [▶ 23]
U600/601	2 x SODIMM 260 DDR4	See: Memory SO-DIMM260 (U601/U600) [▶ 24]
P1202	2 x USB 2.0, internal	See: USB 2.0 internal (P1202/P1204) [▶ 28]
P1204	4 x USB 2.0, internal	See: USB 2.0 internal (P1202/P1204) [▶ 28]
P1102	System, internal	See: System connector (P1102) [▶ 29]
P1100	PCIe x4	See: PCI express connector (P1100) [▶ 30]

6.2 Power input (P1300)

The connection for the power supply of the CB3072 is implemented as a 2x10-pin housing connector.

The 12 V supply is required for the operation of PCI express cards and the fan connections. COM RXD and TXD can also be used for your own power supply unit, e.g. for the UPS function.

Communication takes place via SMBus (SMB-CLK/SMB-DAT).

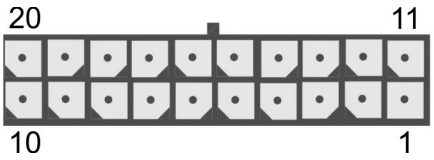


Fig. 3: CB3072 Power Input (P1300)

Pin assignment Power Input					
Description	**Name**	**Pin**		**Name**	**Description**
SMBus clock signal/ COM transmit data	SMB_CLK COM.TXD	1	11	SMB_DAT/ COM.RXD	SMBus data/ COM receive data
'Power Supply On' - Input for switching on the output voltages: Low(0 V) = switch on voltages High(5 V or open (contact) = switch off voltages	PS_ON	2	12	ATX PWRGOOD	'ATX Powergood' - output reports to the PC that all voltages are switched on: Low(0 V) = voltage not ok Open Drain = voltage ok
Power button output for switching the connected PC on and off	ATX PWRBTN#	3	13	SVCC	Supply voltage S5 V
Supply voltage 12 V	12 V	4	14	12 V	Supply voltage 12 V
Ground	GND	5	15	GND	Ground
Ground	GND	6	16	GND	Ground
Supply voltage 5 V	VCC	7	17	VCC	Supply voltage 5 V
Supply voltage 5 V	VCC	8	18	VCC	Supply voltage 5 V
S UPS active output: Low (0 V) = S UPS inactive High (3.3 V) = S UPS active	S UPS	9	19	GND	Ground
Supply voltage 3.3 V	3.3 V	10	20	3.3 V	Supply voltage 3.3 V

6.3 SATA interfaces (P500/1/2/3)

The CB3072 board is equipped with four SATA interfaces, which allow a data transfer rate of up to 6 Gbit per second. The interfaces are available as 7-pin standard SATA connectors. RAID 0/1/5/10 are supported.

The necessary settings are made via the BIOS setup.

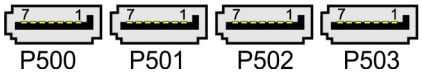


Fig. 4: CB3072 SATA (P500/1/2/3)

Pin assignment SATA interfaces (P500 – P503)		
Pin	**Name**	**Description**
1	GND	Ground
2	SATATX	SATA Transmit +
3	SATATX#	SATA Transmit -
4	GND	Ground
5	SATARX#	SATA Receive -
6	SATARX	SATA Receive +
7	GND	Ground

6.4 Serial interface COM2 internal (P1205)

The internal serial interface COM2 is implemented with a 2x5-pin connector. The signals are available according to the RS232 standard.

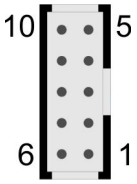


Fig. 5: CB3072 COM2 internal (P1205)

Pin assignment COM2 internal					
Description	**Name**	**Pin**		**Name**	**Description**
Data Carrier Detect	DCD	1	6	DSR	Data Set Ready
Receive Data	RXD	2	7	RTS	Request to Send
Transmit Data	TXD	3	8	CTS	Clear to Send
Data Terminal Ready	DTR	4	9	RI	Ring Indicator
Ground	GND	5	10	S3.3V	Supply voltage 3.3 V

6.5 Fan connections (P1101)

Three fans with a supply voltage of 12 V can be connected to the module. This takes place with a 2x5-pin connector. There are also signals for monitoring the fan speed.

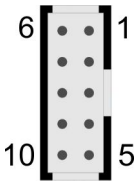


Fig. 6: CB3072 fan (P1101)

Pin assignment fan connection					
Description	**Name**	**Pin**		**Name**	**Description**
Ground switched Fan 1	FANON1	1	6	FANON2	Ground switched Fan 2
Supply voltage 12 V	12 V	2	7	12 V	Supply voltage 12 V
Monitoring fan 1	FANCTRL1	3	8	FANCTRL2	Monitoring fan 2
Supply voltage 12 V	12 V	4	9	FANCTRL3	Monitoring fan 3
Ground switched Fan 3	FANON3	5	10	GND	Ground

6.6 GPIO (P504)

The board has a General Purpose Input/Output interface that is fed out via a 2x6-pin connector. By programming the associated chip (PCA9535BS) accordingly, I/O functions can be created here in a very flexible manner. Ask your distributor about appropriate software support.

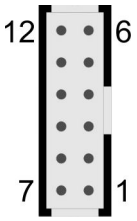


Fig. 7: CB3072-GPIO (P504)

Pin assignment GPIO					
Description	**Name**	**Pin**		**Name**	**Description**
Supply voltage 5 V	VCC	1	7	VCC	Supply voltage 5 V
GP Input/Output1	GPIO0	2	8	GPIO4	GP Input/Output5
GP Input/Output2	GPIO1	3	9	GPIO5	GP Input/Output6
GP Input/Output3	GPIO2	4	10	GPIO6	GP Input/Output7
GP Input/Output4	GPIO3	5	11	GPIO7	GP Input/Output8
Ground	GND	6	12	GND	Ground

6.7 Display Port I-PEX (P1001)

The CB3072 has a further DVI connection, which is implemented in the form of a 30-pin ribbon cable connector. There are no analog VGA signals on this connection, but an HDMI or DisplayPort screen can be connected. In addition, a further USB channel is fed out via this connector. This USB channel supports the specification 3.0. It supplies up to 900 mA current and is electronically protected.

When cabling, be sure to connect receive cables with transmit cables and vice versa. The current drawn from VCC must not exceed 2 A in total (0.5 A per contact); for 3.3 V, the maximum current is 1 A (0.5 A per contact).

NOTICE

Use I-PEX cable!

Use a special I-PEX cable for this interface.

Fig. 8: CB3072 Display Port I-PEX (P1001)

Pin assignment Display Port IPEX		
Pin	**Name**	**Description**
1	TMDS0#/DP2#	DVI Data 0 - / DP Lane 2 -
2	TMDS0/DP2	DVI Data 0 + / DP Lane 2 +
3	TMDS1#/DP1#	DVI Data 1 - / DP Lane 1 -
4	TMDS1/DP1	DVI Data 1 + / DP Lane 1 +
5	TMDS2#/DP0#	DVI Data 2 - / DP Lane 0 -
6	TMDS2/DP0	DVI Data 2 + / DP Lane 0 +
7	TMDSCLK#/DP3#	DVI Clock - / DP Lane 3 -
8	TMDSCLK/DP3	DVI Clock + / DP Lane 3 +
9	N/C	Not connected
10	SEL_DVI/DP#	DVI DisplayPort Select
11	DDCK/DPAUX	EDID Clock / DP Aux +
12	DDDA/DPAUX#	EDID Data / DP Aux -
13	VCC	Supply voltage 5 V
14	GND	Ground
15	HPD	Hot Plug Detect
16	USBVCC	USB supply 5 V
17	USBVCC	USB supply 5 V
18	N/C	Not connected
19	N/C	Not connected
20	SSRX-	SuperSpeed Receive -
21	SSRX+	SuperSpeed Receive +
22	USB-	USB minus data channel
23	USB+	USB plus data channel
24	SSTX-	SuperSpeed Transmit-
25	SSTX+	SuperSpeed Transmit+
26	3.3 V	Supply voltage 3.3 V
27	3.3 V	Supply voltage 3.3 V
28	VCC	Supply voltage 5 V
29	VCC	Supply voltage 5 V
30	VCC	Supply voltage 5 V

6.8 LAN 1 Gbit (P700) / LAN 2.5 Gbit (P800)

The board has three Gigabit-LAN connections. (10BaseT-, 100BaseT-. 1000BaseT and 2500BaseT - compatible network components can be connected. The required speed is selected automatically. Auto-Cross and Auto-Negotiate are available as well as PXE and RPL functionality. Controller is Intel®'s i219 for LAN1 and i226 for LAN 2.

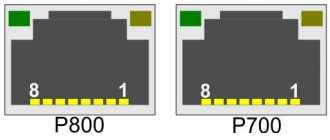


Fig. 9: CB3072-LAN (P700-800)

Pin assignment LAN socket i219 (P700)		
Pin	**Name**	**Description**
1	LAN10	LAN line 1 +
2	LAN10#	LAN line 1 -
3	LAN11	LAN line 2 +
4	LAN11#	LAN line 2 -
5	LAN12	LAN line 3 +
6	LAN12#	LAN line 3 -
7	LAN13	LAN line 4 +
8	LAN13#	LAN line 4 -

Pin assignment LAN socket i226 (P800)		
Pin	**Name**	**Description**
1	LAN20	LAN line 1 +
2	LAN20#	LAN line 1 -
3	LAN21	LAN line 2 +
4	LAN21#	LAN line 2 -
5	LAN22	LAN line 3 +
6	LAN22#	LAN line 3 -
7	LAN23	LAN line 4 +
8	LAN23#	LAN line 4 -

The LEDs of the LAN interface (P700) indicate the activity and speed of the data transmission (Mbit/s). The left LED lights up when there is a connection and activity, and the right LED during data transmission:

Left LED Steadily lit when there is a connection, flashing during data transmission	**Right LED Steadily lit during data transmission**	**Mbit/s**
Green	Green	1000
Green	Orange	100
Green	Off	10

The LEDs of the LAN interface (P800) indicate the activity and speed of the data transmission (Mbit/s). The left LED lights up when there is a connection and activity, and the right LED during data transmission:

Left LED Steadily lit when there is a connection, flashing during data transmission	Right LED Steadily lit during data transmission	Mbit/s
Green	Green	2500
Green	Orange	1000
Green	Off	100/10

Real-time applications

The Ethernet port connected via PCIe is usually suitable for cycle times <= 1 ms and for distributed clock applications with EtherCAT.
The Ethernet port integrated in the chipset is usually suitable for real-time Ethernet applications with cycle times > 1 ms (without distributed clocks).

6.9 USB 3.2 external (P1201/P1203)

USB 3.2 channels 1 to 4 are fed out in the form of standard USB connectors.

The USB channels support the USB specification 3.x. All necessary settings for USB can be made by the BIOS.

NOTICE

Functionality of USB mouse and keyboard

Note that the "USB Mouse and Keyboard" functionality of the BIOS setup is only required if the operating system does not provide USB support. Do not select this function for settings in the setup and for booting Windows with a connected USB mouse and keyboard, because this would result in significant performance limitations.

The individual USB interfaces can supply a current of up to 900 mA and are electronically protected.

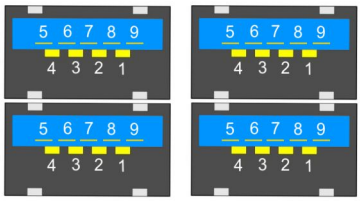


Fig. 10: CB3072 USB3.0 (P1201+1203)

Pin assignment USB3.0 (P1201+P1203)		
Pin	**Name**	**Description**
1	VCC	5 V for USBX
2	USB3-1D#	Minus data channel USB3
3	USB3-1D	Plus data channel USBX3
4	GND	Ground
5	USB3-1SSRX-	SuperSpeed Receiver -
6	USB3-1SSRX+	SuperSpeed Receiver +
7	GND	Ground
8	USB3-1SSTX-	SuperSpeed Transmitter -
9	USB3-1SSTX+	SuperSpeed Transmitter +

6.10 DVI-D (P1000)

The board has a DVI-D connection for DVI-capable displays. Analog displays cannot be connected.

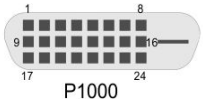


Fig. 11: CB3072 DVI (P1000)

Pin assignment DVI-D		
Pin	**Name**	**Description**
1	TMDS#2	DVI data 2 -
2	TMDS2	DVI data 2 +
3	GND	Ground
4	N/C	Not connected
5	N/C	Not connected
6	DDCCLK	DDC Clock (DVI/VGA)
7	DDCDAT	DDC Data (DVI/VGA)
8	N/C	Not connected
9	TMDS#1	DVI data 1 -
10	TMDS1	DVI data 1 +
11	GND	Ground
12	N/C	Not connected
13	N/C	Not connected
14	VCC	Supply voltage 5 V
15	GND	Ground
16	HPD	Hot Plug Detect
17	TMDS#0	DVI data 0 -
18	TMDS0	DVI data 0 +
19	GND	Ground
20	N/C	Not connected
21	N/C	Not connected
22	GND	Ground
23	TMDSCLK	DVI-Clock +
24	TMDSCLK#	DVI-Clock -

6.11 Serial interface COM1 (P1200)

The COM1 serial interface is fed out via a 9-pin standard DSUB connector (male). The signals are available according to the RS232 standard.

The port address and the interrupt used are set with the help of the BIOS setup.

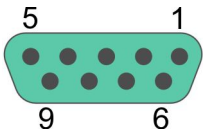


Fig. 12: CB3072 COM1 (P1200)

Pin assignment COM1					
Description	**Name**	**Pin**		**Name**	**Description**
Data Carrier Detect -	DCD#	1	6	DSR#	Data Set Ready -
Receive Data	RXD	2	7	RTS#	Request to Send -
Transmit Data	TXD	3	8	CTS#	Clear to Send -
Data Terminal Ready -	DTR#	4	9	RI#	Ring Indicator -
Ground	GND	5			

6.12 Memory SO-DIMM260 (U601/U600)

On the CB3072 board there are two SO-DIMM260 memory slots for DDR4-3200 RAM. For technical and mechanical reasons, it is possible that certain memory modules cannot be used. Information regarding the recommended memory modules can be obtained from your distributor.

With two slots, a memory extension up to 64 GB is possible with currently available modules. When populating both memory slots, make sure that you use identical memory modules.

All timing parameters for the different makes and versions are automatically set by the BIOS.

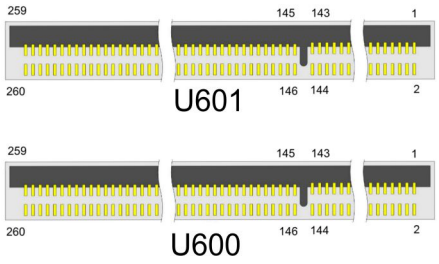


Fig. 13: CB3072 SoDimm260 (U601-600)

Pin assignment SO-DIMM260 (U601 + U600)					
Description	**Name**	**Pin**		**Name**	**Description**
Ground	GND	1	2	GND	Ground
Data line 5	DQ5	3	4	DQ4	Data line 4
Ground	GND	5	6	GND	Ground
Data line 1	DQ1	7	8	DQ0	Data line 0
Ground	GND	9	10	GND	Ground
Data Strobe 0 -	DQS0#	11	12	NC	Not connected
Data Strobe 0 +	DQS0	13	14	GND	Ground
Ground	GND	15	16	DQ6	Data line 6
Data line 7	DQ7	17	18	GND	Ground
Ground	GND	19	20	DQ2	Data line 2
Data line 3	DQ3	21	22	GND	Ground
Ground	GND	23	24	DQ12	Data line 12
Data line 13	DQ13	25	26	GND	Ground
Ground	GND	27	28	DQ8	Data line 8
Data line 9	DQ9	29	30	GND	Ground
Ground	GND	31	32	DQS1#	Data Strobe 1 -
Data Mask 1	DQM1	33	34	DQS1	Data Strobe 1 +
Ground	GND	35	36	GND	Ground
Data line 15	DQ15	37	38	DQ14	Data line 14
Ground	GND	39	40	GND	Ground
Data line 10	DQ10	41	42	DQ11	Data line 11
Ground	GND	43	44	GND	Ground
Data line 21	DQ21	45	46	DQ20	Data line 20
Ground	GND	47	48	GND	Ground
Data line 17	DQ17	49	50	DQ16	Data line 16
Ground	GND	51	52	GND	Ground
Data Strobe 2 -	DQS2#	53	54	DQM2	Data Mask 2
Data Strobe 2 +	DQS2	55	56	GND	Ground
Ground	GND	57	58	DQ22	Data line 22
Data line 23	DQ23	59	60	GND	Ground
Ground	GND	61	62	DQ18	Data line 18
Data line 19	DQ19	63	64	GND	Ground
Ground	GND	65	66	DQ28	Data line 28
Data line 29	DQ29	67	68	GND	Ground
Ground	GND	69	70	DQ24	Data line 24
Data line 25	DQ25	71	72	GND	Ground
Ground	GND	73	74	DQS3#	Data Strobe 3 -
Data Mask 3	DQM3	75	76	DQS3	Data Strobe 3 +
Ground	GND	77	78	GND	Ground
Data line 30	DQ30	79	80	DQ31	Data line 31
Ground	GND	81	82	GND	Ground
Data line 26	DQ26	83	84	DQ27	Data line 27
Ground	GND	85	86	GND	Ground
Not connected	CB5/NC	87	88	CB4/NC	Not connected
Ground	GND	89	90	GND	Ground
Not connected	CB1/NC	91	92	CB0/NC	Not connected
Ground	GND	93	94	GND	Ground

Pin assignment SO-DIMM260 (U601 + U600)					
Description	**Name**	**Pin**		**Name**	**Description**
Data Strobe 8 -	DQS8#	95	96	DQM8	Data Mask 8
Data Strobe 8 +	DQS8	97	98	GND	Ground
Ground	GND	99	100	CB6/NC	Not connected
Not connected	CB2/NC	101	102	GND	Ground
Ground	GND	103	104	CB7/NC	Not connected
Not connected	CB3/NC	105	106	GND	Ground
Ground	GND	107	108	RESET_n	Reset
Clock Enable 0	CKE0	109	110	CKE1	Clock Enable 1
Supply voltage 1.2 V	VCC	111	112	VCC	Supply voltage 1.2 V
Bank Group Input 1	BG1	113	114	ACT_n	Activation Command Input
Bank Group Input 0	BG0	115	116	ALERT_n	Alert
Supply voltage 1.2 V	VCC	117	118	VCC	Supply voltage 1.2 V
Address line 12	A12	119	120	A11	Address line 11
Address line 9	A9	121	122	A7	Address line 7
Supply voltage 1.2 V	VCC	123	124	VCC	Supply voltage 1.2 V
Address line 8	A8	125	126	A5	Address line 5
Address line 6	A6	127	128	A4	Address line 4
Supply voltage 1.2 V	VCC	129	130	VCC	Supply voltage 1.2 V
Address line 3	A3	131	132	A2	Address line 2
Address line 1	A1	133	134	EVENT_n	Event
Supply voltage 1.2 V	VCC	135	136	VCC	Supply voltage 1.2 V
Clock Signal 0 +	CK0	137	138	CK1	Clock 1 +
Clock Signal 0 -	CK0#	139	140	CK1#	Clock 1 -
Supply voltage 1.2 V	VCC	141	142	VCC	Supply voltage 1.2 V
Even parity check	PAR	143	144	A0	Address line 0
SDRAM Bank 2	BA1	145	146	A10/AP	Address line10/ Autoprecharge
Supply voltage 1.2 V	VCC	147	148	VCC	Supply voltage 1.2 V
Chip Select 0	CS0_n	149	150	BA0	 Bank Adress 0
Address line 14/Write Enable	A14/WE_n	151	152	A16/RAS_n	Address line 16/ Row Address Strobe
Supply voltage 1.2 V	VCC	153	154	VCC	Supply voltage 1.2 V
On Die Termination 0	ODT0	155	156	A15/CAS_n	Address line 15/ Column Address Strobe
Chip Select 1	CS1_n	157	158	A13	Address line 13
Supply voltage 1.2 V	VCC	159	160	VCC	Supply voltage 1.2 V
On Die Termination 1	ODT1	161	162	S2/NC	Not connected
Supply voltage 1.2 V	VCC	163	164	VREFCA	Reference voltage
Not connected	S3/NC	165	166	SA2	SPD Address 2
Ground	GND	167	168	GND	Ground
Data line 37	DQ37	169	170	DQ36	Data line 36
Ground	GND	171	172	GND	Ground
Data line 33	DQ33	173	174	DQ32	Data line 32
Ground	GND	175	176	GND	Ground
Data Strobe 4 -	DQS4#	177	178	DQM4	Data Mask 4
Data Strobe 4 +	DQS4	179	180	GND	Ground
Ground	GND	181	182	DQ39	Data line 39

Pin assignment SO-DIMM260 (U601 + U600)					
Description	**Name**	**Pin**		**Name**	**Description**
Data line 38	DQ38	183	184	GND	Ground
Ground	GND	185	186	DQ35	Data line 35
Data line 34	DQ34	187	188	GND	Ground
Ground	GND	189	190	DQ45	Data line 45
Data line 44	DQ44	191	192	GND	Ground
Ground	GND	193	194	DQ41	Data line 41
Data line 40	DQ40	195	196	GND	Ground
Ground	GND	197	198	DQS5#	Data Strobe 5 -
Not connected	NC	199	200	DQS5	Data Strobe 5 +
Ground	GND	201	202	GND	Ground
Data line 46	DQ46	203	204	DQ47	Data line 47
Ground	GND	205	206	GND	Ground
Data line 42	DQ42	207	208	DQ43	Data line 43
Ground	GND	209	210	GND	Ground
Data line 52	DQ52	211	212	DQ53	Data line 53
Ground	GND	213	214	GND	Ground
Data line 49	DQ49	215	216	DQ48	Data line 48
Ground	GND	217	218	GND	Ground
Data Strobe 6 -	DQS6#	219	220	DQM6	Data Mask 6
Data Strobe 6 +	DQS6	221	222	GND	Ground
Ground	GND	223	224	DQ54	Data line 54
Data line 55	DQ55	225	226	GND	Ground
Ground	GND	227	228	DQ50	Data line 50
Data line 51	DQ51	229	230	GND	Ground
Ground	GND	231	232	DQ60	Data line 60
Data line 61	DQ61	233	234	GND	Ground
Ground	GND	235	236	DQ57	Data line 57
Data line 56	DQ56	237	238	GND	Ground
Ground	GND	239	240	DQS7#	Data Strobe 7 -
Data Mask 7	DQM7	241	242	DQS7	Data Strobe 7 +
Ground	GND	243	244	GND	Ground
Data line 62	DQ62	245	246	DQ63	Data line 63
Ground	GND	247	248	GND	Ground
Data line 58	DQ58	249	250	DQ59	Data line 59
Ground	GND	251	252	GND	Ground
SMBus Clock	SCL	253	254	SDA	SMBus Data
I²C Power for SPD EEProm	VCCSPD	255	256	SA0	SPD Address 0
DRAM Activating Power	VPP	257	258	M_VTT	Termination voltage
DRAM Activating Power	VPP	259	260	SA1	SPD Address 1

6.13 USB 2.0 internal (P1202/P1204)

USB channels 6 to 11 are provided via two connectors.

Channels 6 to 9 are fed out via a 2x8-pin connector, channels 10 and 11 via a 2x4-pin connector.

The USB channels support the USB specification 2.0. All necessary settings for USB can be made by the BIOS. Note that the "USB mouse and keyboard" function in the BIOS setup is only required if the operating system does not offer USB support. This function should not be selected for settings in the setup and for booting Windows with a USB mouse and keyboard connected, because this would lead to considerable performance limitations.

The individual USB interfaces can supply a current of up to 500 mA and are electronically protected.

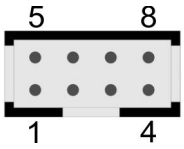


Fig. 14: CB3072 USB2.0 (P1202)

Pin assignment 2x4-pin connector USB 10/11 (P1202)					
Description	**Name**	**Pin**		**Name**	**Description**
5 V for USB13	VCC	1	5	VCC	5 V for USB14
Minus data channel USB10	USB10-	2	6	USB11-	Minus data channel USB11
Plus data channel USB10	USB10+	3	7	USB11+	Plus data channel USB11
Ground	GND	4	8	GND	Ground

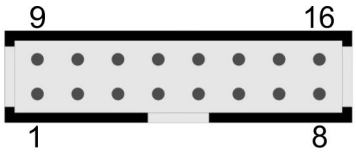


Fig. 15: CB3072 USB2.0 (P1204)

Pin assignment 2x8-pin connector USB 6 – 9 (P1204)					
Description	**Name**	**Pin**		**Name**	**Description**
5 V for USB6	VCC	1	9	VCC	5 V for USB7
Minus data channel USB6	USB6-	2	10	USB7-	Minus data channel USB7
Plus data channel USB6	USB6+	3	11	USB7+	Plus data channel USB7
Ground	GND	4	12	GND	Ground
Ground	GND	5	13	GND	Ground
Plus data channel USB8	USB8+	6	14	USB9+	Plus data channel USB9
Minus data channel USB8	USB8-	7	15	USB9-	Minus data channel USB9
5 V for USB8	VCC	8	16	VCC	5 V for USB9

6.14 System connector (P1102)

A 2x12-pin connector is used for the connection of signals that are typical of the system. Power button, reset, speaker, LEDs for hard disk and for Suspend mode are connected here along with three further status LEDs that are controlled via GPIOs. Of these three LEDs, LED1 and LED2 are already equipped with series resistors. The pin assignment is designed so that associated pins are located opposite or near to each other.

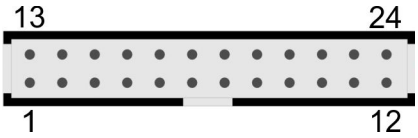


Fig. 16: CB3072 system (P1102)

Pin assignment system connector (P1102)					
Description	**Name**	**Pin**		**Name**	**Description**
Ground	GND	1	14	3.3 V	Supply voltage 3.3 V
Reset to ground	RSTBTTN#	2	14	PWRBTN#	On/Suspend button
LED Suspend/ACPI	S-LED	3	15	S3.3V	Standby supply 3.3 V
LED hard disk	SATALED#	4	16	TCLEDB	TwinCAT LED blue
TwinCAT LED red	TCLEDR	5	17	BATT	RTC battery
TwinCAT LED green	TCLEDG	6	18	SMBALERT#	SMB Alert
SMB Clock	SMBCLKEXT	7	19	SMBDATEXT	SMB Data
Speaker	SPEAKER	8	20	SVCC	Standby supply 5 V
Reserved	NC	9	21	NC	Reserved
Ground	GND	10	22	VCC	Supply voltage 5 V
Ground	GND	11	23	VCC	Supply voltage 5 V
Ground	GND	12	24	VCC	Supply voltage 5 V

6.15 PCI express connector (P1100)

The CB3072 is equipped with a vendor-specific 2x40-pin connector, via which PCI express devices can be connected. Either up to four PCIe1x devices or precisely one PCIe x4 device can be connected. Adapter cards with standard PCIe slots as well as with PCIe Mini-Card connectors are available as accessories. Please contact your distributor for this.

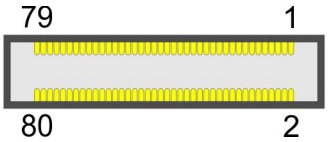


Fig. 17: CB3072 PCIE (P1100)

Pin assignment PCI express connector (P1100)					
Description	**Name**	**Pin**		**Name**	**Description**
Supply voltage 3.3 V	3.3 V	1	2	12 V	Supply voltage 12 V
Standby supply 3.3 V	S3.3V	3	4	SMCLK1	SMB Clock Slot 1
PCIe Reset 1 -	PERST1#	5	6	SMDAT1	SMB Dat Slot 1
Link Reactivation 1 -	WAKE1#	7	8	GND	Ground
Ground	GND	9	10	REFCLK1	PCIe Clock 1 +
Transmit Lane 1 +	PET1	11	12	REFCLK1#	PCIe Clock 1 -
Transmit Lane 1 -	PET1#	13	14	GND	Ground
Ground	GND	15	16	PER1	Receive Lane 1 +
Clock Enable 1 -	PRSNT1#	17	18	PER1#	Receive Lane 1 -
Ground	GND	19	20	GND	Ground
Supply voltage 3.3 V	3.3 V	21	22	12 V	Supply voltage 12 V
Standby supply 3.3 V	S3.3V	23	24	SMCLK2	SMB Clock Slot 2
PCIe Reset 2 -	PERST2#	25	26	SMDAT2	SMB Dat Slot 2
Link Reactivation 2 -	WAKE2#	27	28	GND	Ground
Ground	GND	29	30	REFCLK2	PCIe Clock 2 +
Transmit Lane 2 +	PET2	31	32	REFCLK2#	PCIe Clock 2 -
Transmit Lane 2 -	PET2#	33	34	GND	Ground
Ground	GND	35	36	PER2	Receive Lane 2 +
Clock Enable 2 -	PRSNT2#	37	38	PER2#	Receive Lane 2 -
Ground	GND	39	40	GND	Ground
Supply voltage 3.3 V	3.3 V	41	42	12 V	Supply voltage 12 V
Standby supply 3.3 V	S3.3V	43	44	SMCLK3	SMB Clock Slot 3
PCIe Reset 3 -	PERST3#	45	46	SMDAT3	SMB Dat Slot 3
Link Reactivation 3 -	WAKE3#	47	48	GND	Ground
Ground	GND	49	50	REFCLK3	PCIe Clock 3 +
Transmit Lane 3 +	PET3	51	52	REFCLK3#	PCIe Clock 3 -
Transmit Lane 3 -	PET3#	53	54	GND	Ground
Ground	GND	55	56	PER3	Receive Lane 3 +
Clock Enable 3 -	PRSNT3#	57	58	PER3#	Receive Lane 3 -
Ground	GND	59	60	GND	Ground
Supply voltage 3.3 V	3.3 V	61	62	12 V	Supply voltage 12 V
Standby supply 3.3 V	S3.3V	63	64	SMCLK4	SMB Clock Slot 4
PCIe Reset 4 -	PERST4#	65	66	SMDAT4	SMB Dat Slot 4
Link Reactivation 4 -	WAKE4#	67	68	GND	Ground
Ground	GND	69	70	REFCLK4	PCIe Clock 4 +
Transmit Lane 4 +	PET4	71	72	REFCLK4#	PCIe Clock 4 -
Transmit Lane 4 -	PET4#	73	74	GND	Ground
Ground	GND	75	76	PER4	Receive Lane 4 +
Clock Enable 4 -	PRSNT4#	77	78	PER4#	Receive Lane 4 -
PCIe configuration x1/x4	PECONF x1/x4	79	80	GND	Ground

7 BIOS

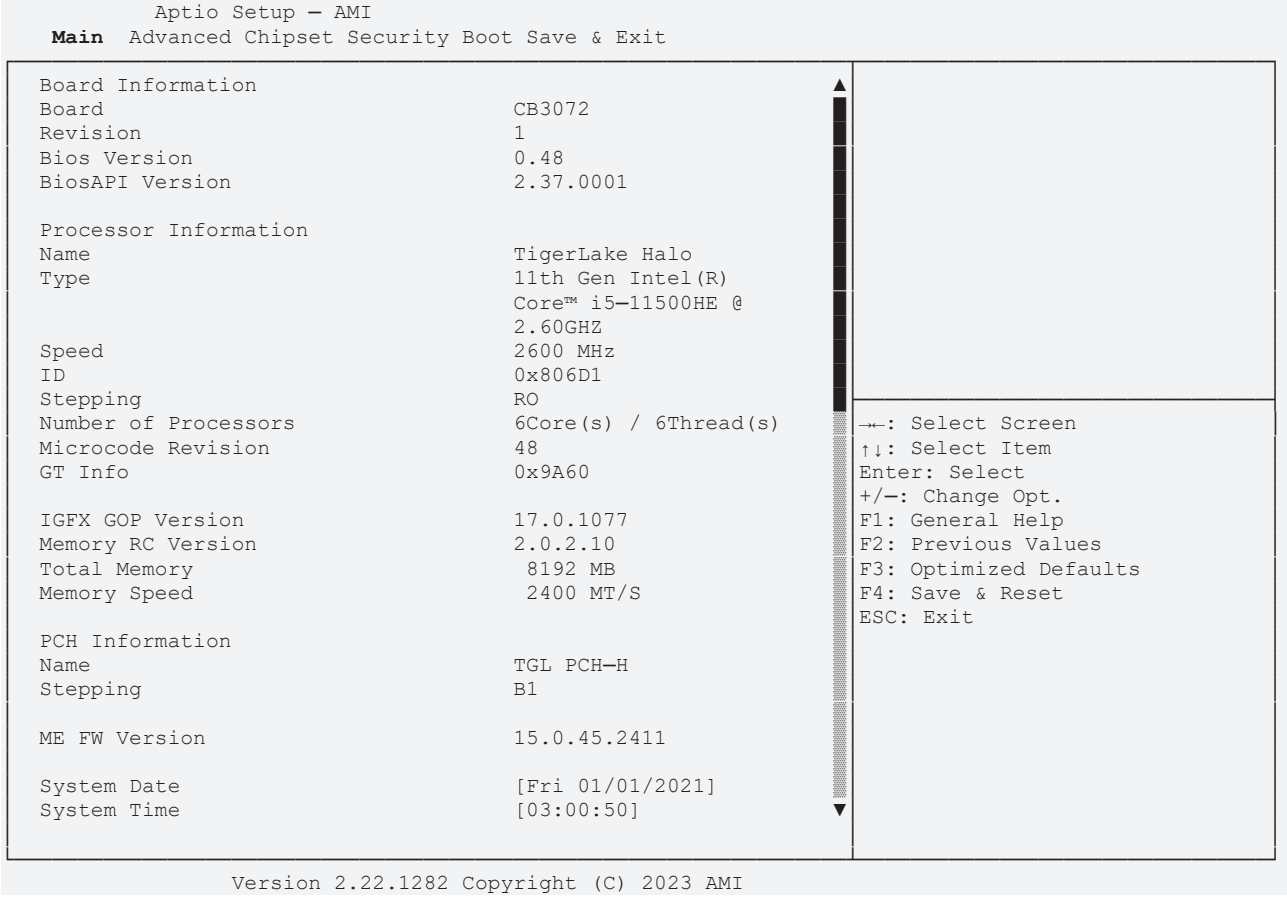
7.1 Using the setup

Within the individual setup pages the last saved settings can be restored can at any time with F2 ("Previous Values"). Use F3 ("Optimized Defaults") to load the factory defaults. Use F2/F3 to load the complete set of settings and F4 to save them (“Save & Reset”).

A "►" sign in front of the menu item indicates that a submenu is available. Use the arrow keys to navigate between menu items. Use the Enter key to select menu items and call submenus or selection dialogs.

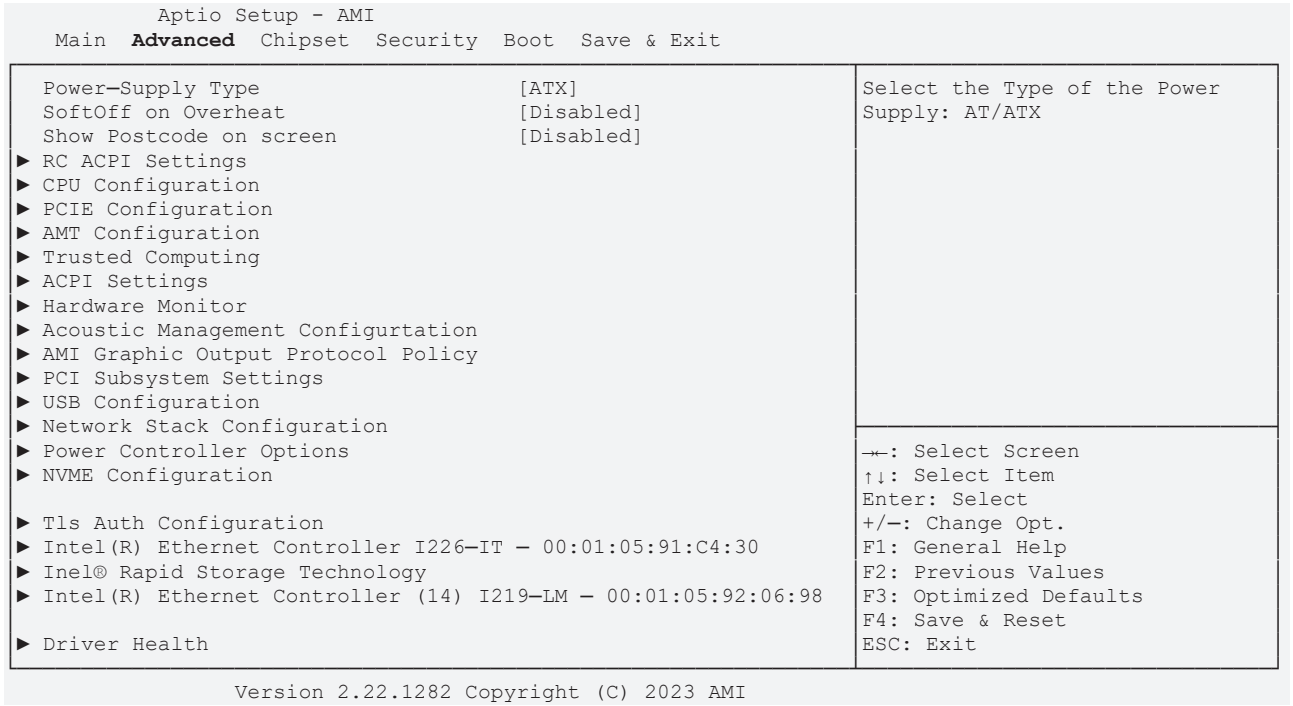
For each setup option a help text is displayed at the top right, which in many cases contains useful information about the option and permitted values, etc.

7.2 Main CB3072



BIOS entry	Options
Board	None
Revision	None
Bios version	None
Platform information	
TigerLake Halo, 11th Gen Intel® Core™ i5-11500HE @ 2.60GHz	
Speed	None
ID	None
Stepping	None
Number of Processors	None
Microcode Revision	None
GT Info	None
IGFX GOP Version	None
Memory RC version	None
Total Memory	None
Memory Speed	None
PCH information	None
Name	None
Stepping	None
ME FW version	None
System Date	Set the system date here.
System Time	Set the system time here.

7.3 Advanced CB3072

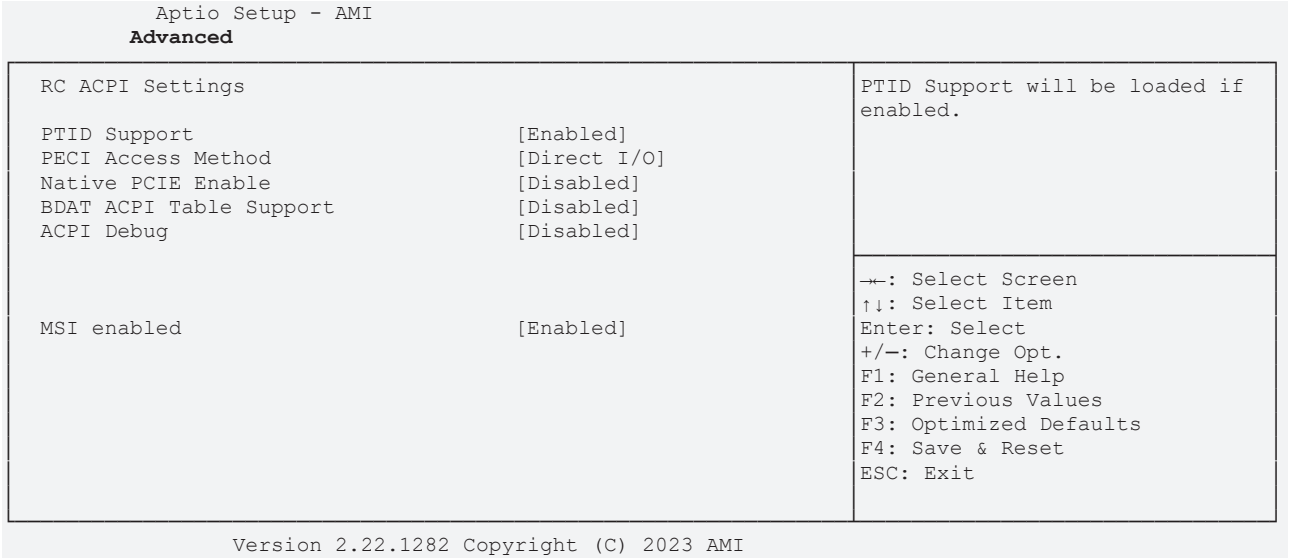


BIOS entry	Options
Power - Supply Type [ATX]	ATX / AT
SoftOff on Overheat	Disabled / Enabled
Show Postcode on screen	Disabled / Enabled
▶RC ACPI Settings	Submenu: see: RC ACPI Settings [▶ 37]
▶CPU Configuration	Submenu: see: CPU Configuration [▶ 38]
▶PCIE Configuration	Submenu: see: PCIE Configuration [▶ 40]
▶AMT Configuration	Submenu: see: AMT Configuration [▶ 41]
▶Trusted Computing	Submenu: see: Trusted Computing [▶ 45]
▶ACPI Settings	Submenu: see: ACPI Settings [▶ 46]
▶Hardware Monitor	Submenu: see: Hardware Monitor [▶ 47]
▶Acoustic Management Configuration	Submenu: see: Acoustic Management Configuration [▶ 48]
▶AMI Graphic Output Protocol Policy	Submenu: see: AMI Graphic Output Protocol Policy [▶ 48]
▶PCI Subsystem Settings	Submenu: see: PCI Subsystem Settings [▶ 49]
▶USB Configuration	Submenu: see: USB Configuration [▶ 50]
▶Network Stack Configuration	Disabled / Enabled
▶Power Controller Options	Submenu: see: Power Controller Options [▶ 52]
▶NVMe Configuration	Submenu: see: NVMe Configuration [▶ 53]
▶Tls Auth Configuration	Submenu: see: TLs Auth Configuration [▶ 53]
▶Intel® Ethernet Controller I226-IT - 00:01:05:91:C4:30	Submenu: see: Intel Ethernet Controller I226-IT [▶ 55]
▶Intel® Rapid Store Technology	None
▶Intel® Ethernet Controller (14) I219-LM - 00:01:05:92:06:98	Submenu: see: Intel Ethernet Controller I219-LM [▶ 56]
▶Driver Health	Submenu: see: Driver Health [▶ 56]

MAC address

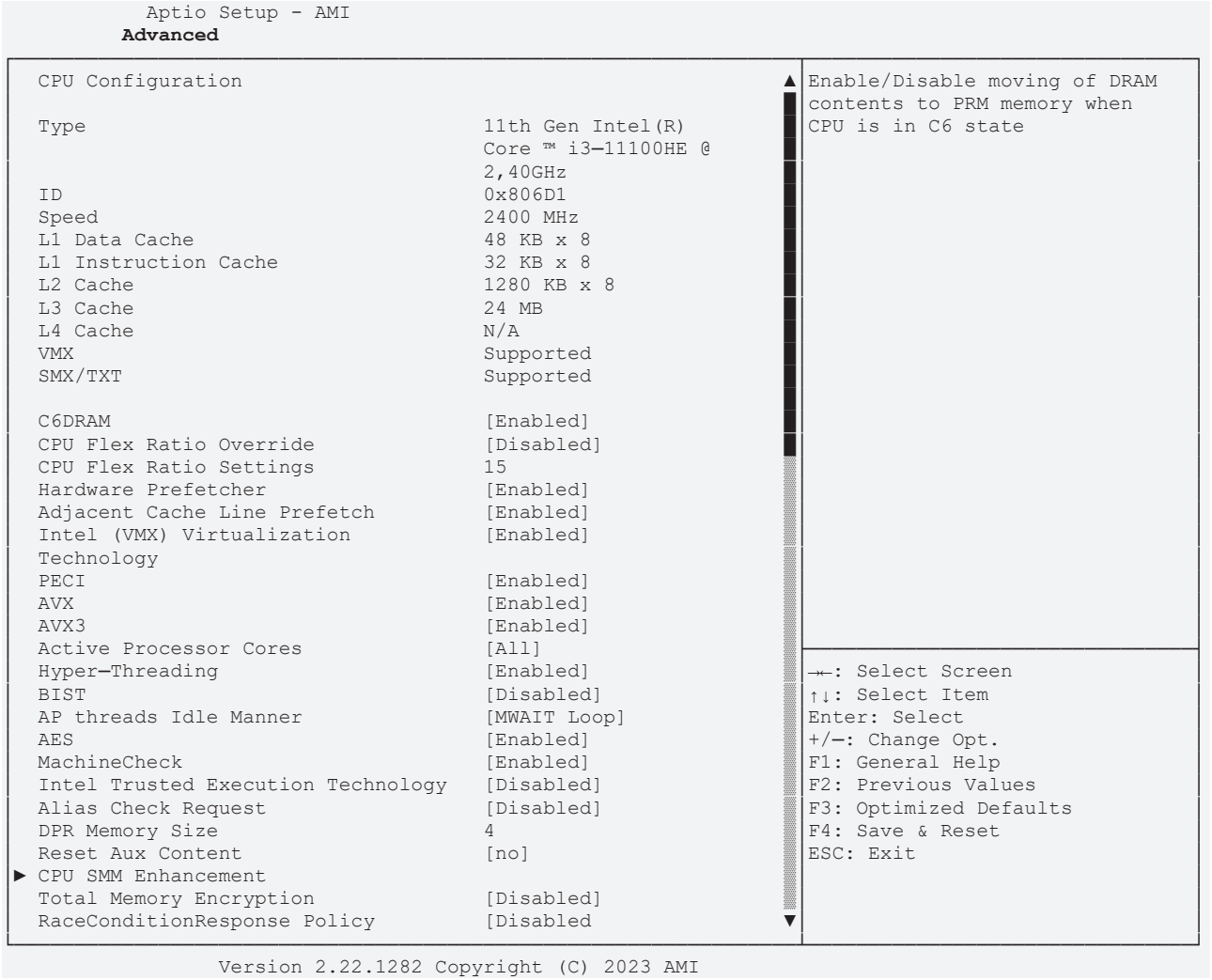
The MAC address is composed of the fixed Beckhoff part 00:01:05 and the board specific part XX:XX:XX.

7.3.1 RC ACPI Settings



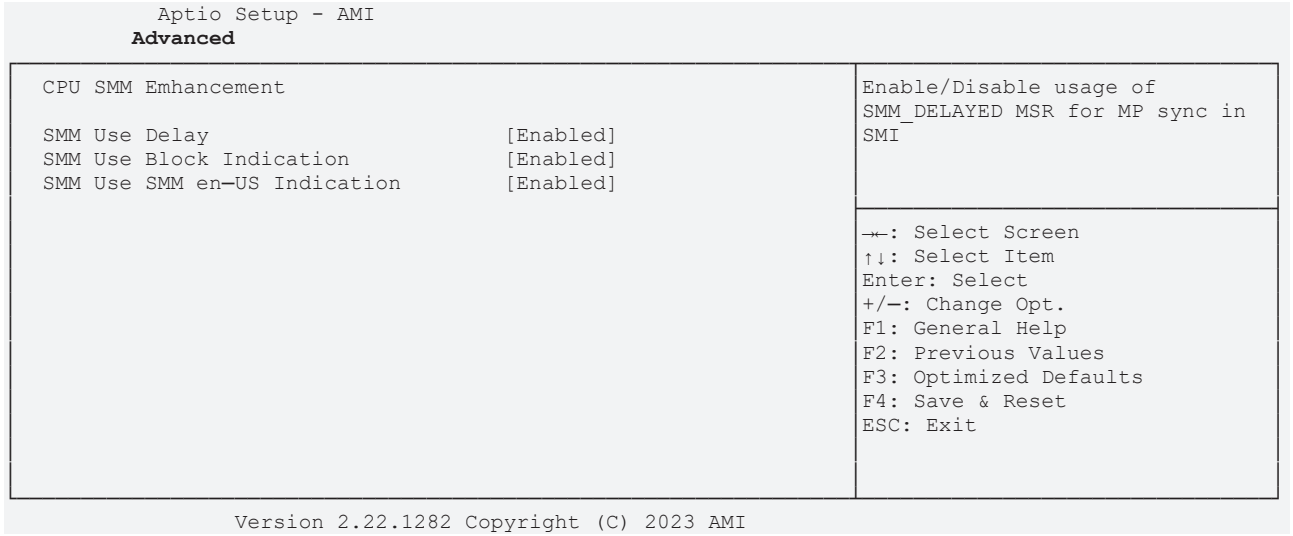
BIOS entry	Options
RC ACPI Settings	
PTID Support	Enabled / Disabled
PECI Access Method	Direct I/O / ACPI
Native PCIE Enable	Disabled / Enabled
BDAT ACPI Table Support	Disabled / Enabled
ACPI Debug	Disabled / Enabled
MSI enabled	Enabled / Disabled

7.3.2 CPU Configuration



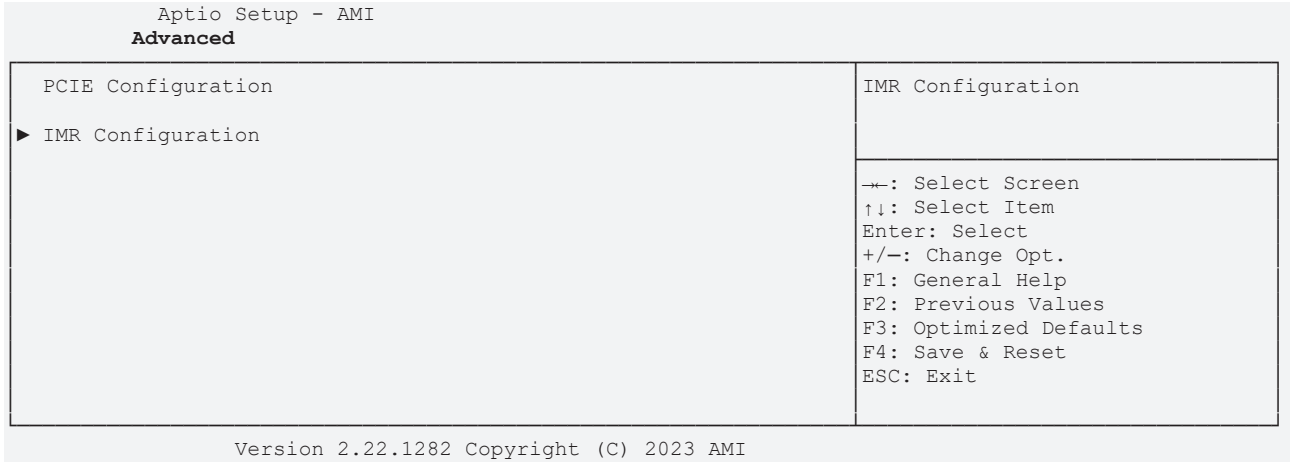
BIOS entry	Options
CPU Configuration	
Type	None
ID	None
Speed	None
L1 Data Cache	None
L1 Instruction Cache	None
L2 Cache	None
L3 Cache	None
L4 Cache	None
VMX	None
SMX/TXT	None
C6DRAM	Enabled / Disabled
CPU Flex Ratio Override	Enabled / Disabled
CPU Flex Ratio Settings	None
Hardware Prefetcher	Enabled / Disabled
Adjacent Cache Line Prefetch	Enabled / Disabled
Intel (VMX)Virtualization Technology	Enabled / Disabled
PECI	Enabled / Disabled
AVX	Enabled / Disabled
AVX3	Enabled / Disabled
Active Processor Cores	All / 1 – 7
Hyper-Threading	Enabled / Disabled
BIST	Disabled / Enabled
AP threads Idle Manner	HALT Loop / MWAIT Loop / Run Loop
AES	Enabled / Disabled
MachineCheck	Enabled / Disabled
Intel Trusted Execution	Disabled / Enabled
Alias Check Request	None
DPR Memory Size (MB)	None
Reset Aux Content	None
►CPU SMM Enhancement	Submenu: see CPU SMM Enhancement [▶ 40]
Total Memory Encryption	Disabled / Enabled
RaceConditionResponse Policy	Disabled / Enabled

7.3.2.1 CPU SMM Enhancement



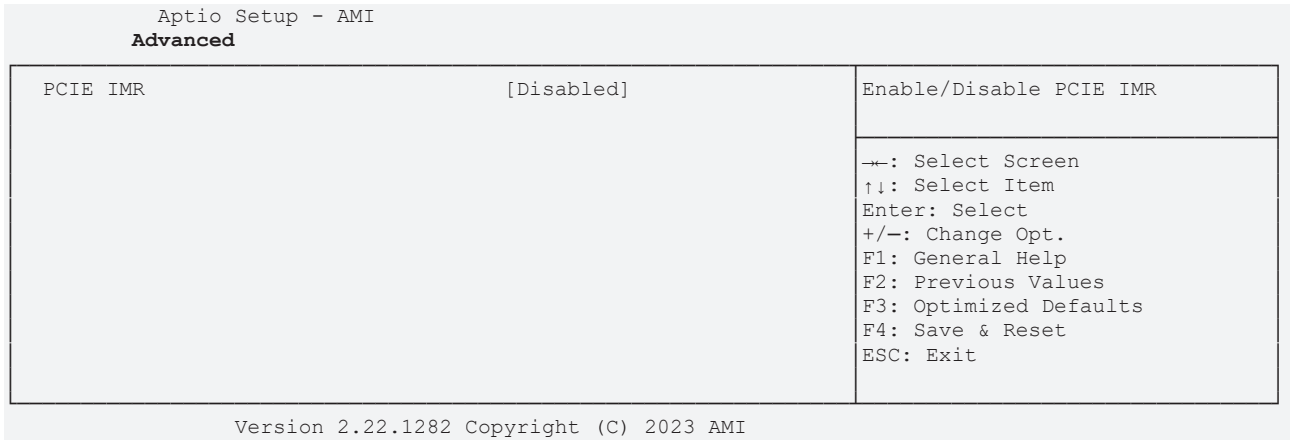
BIOS entry	Options
CPU SMM Enhancement	
SMM Use Delay Indication	Enabled / Disabled
SMM Use Block Indication	Enabled / Disabled
SMM Use SMM en-US Indication	Enabled / Disabled

7.3.3 PCIE Configuration



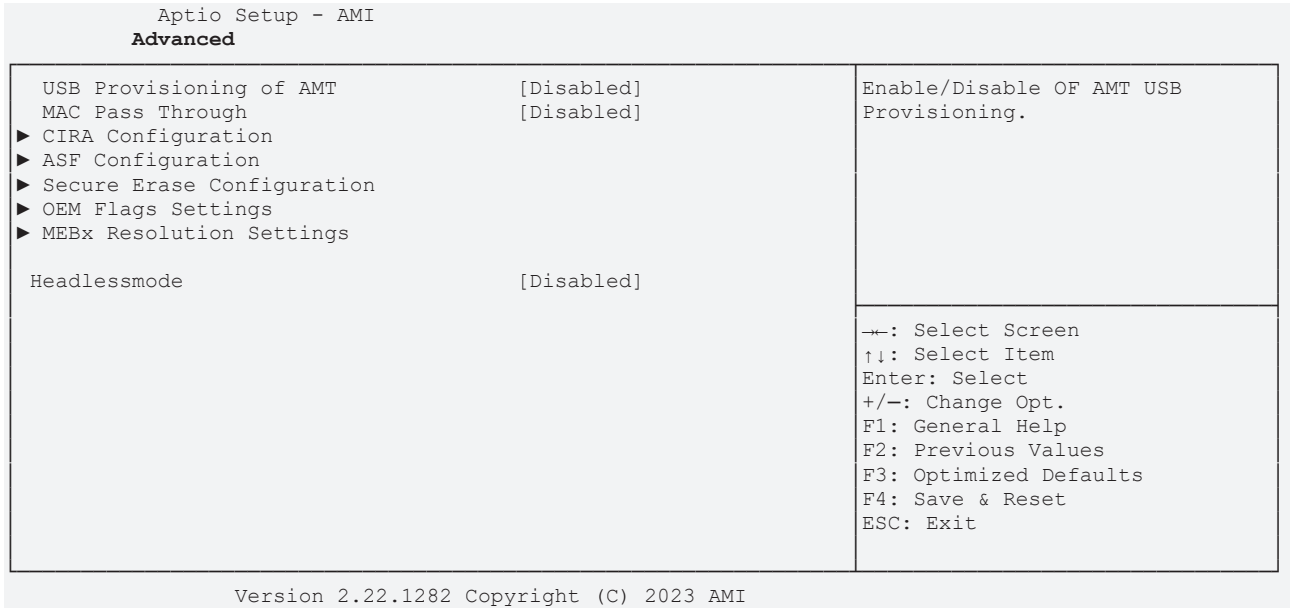
BIOS entry	Options
PCIE Configuration	
▶IMR Configuration	Submenu see: PCIe IMR [▶ 41]

7.3.3.1 PCIe IMR



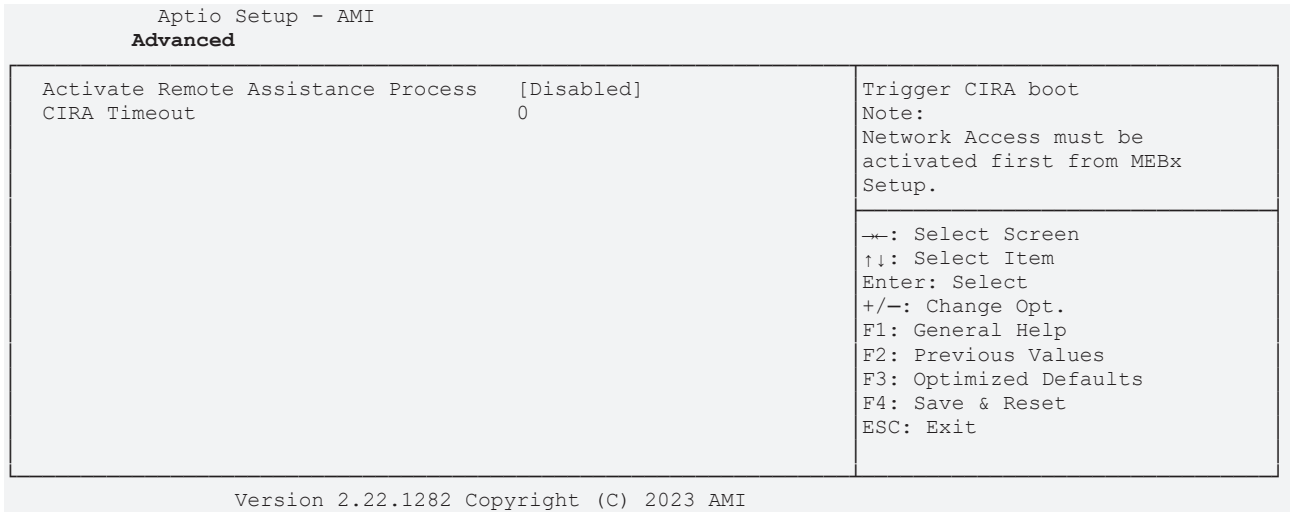
BIOS entry	Options
PCIE IMR	Enabled / Disabled

7.3.4 AMT Configuration



BIOS entry	Options
USB Provisioning of AMT	Disabled / Enabled
MAC Pass Through	Disabled / Enabled
▶CIRA Configuration	Submenu see: CIRA Configuration [▶ 42]
▶ASF Configuration	Submenu see: ASF Configuration [▶ 43]
▶Secure Erase Configuration	Submenu see: Secure Erase Configuration [▶ 43]
▶OEM Flags Settings	Submenu see: OEM Flags Settings [▶ 44]
▶MEBx Resolution Settings	Submenu see: MEBx Resolution Settings [▶ 44]
Headlessmode	Disabled / Enabled

7.3.4.1 CIRA Configuration

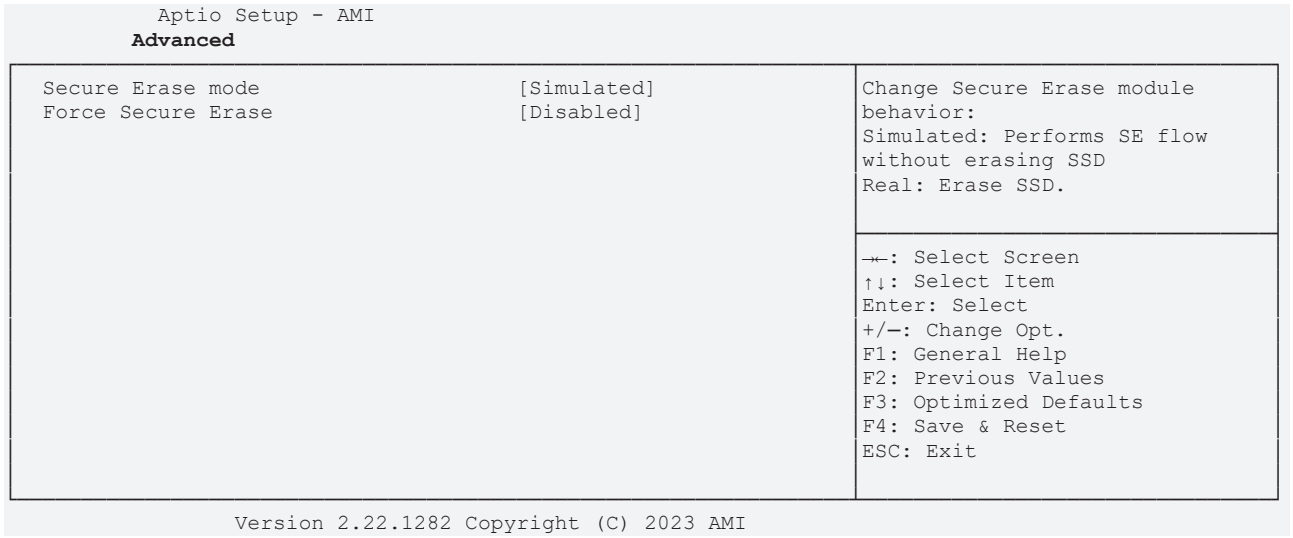


BIOS entry	Options
Activate Remote Assistance Process	Disabled / Enabled
CIRA Timeout	None

7.3.4.2 ASF Configuration

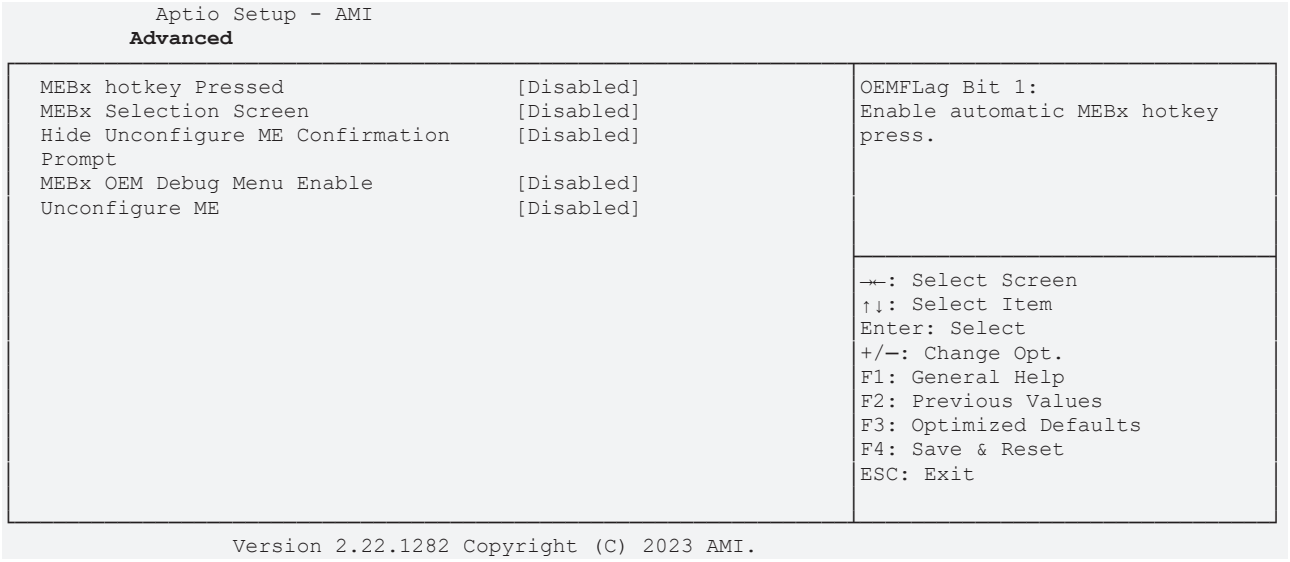
BIOS entry	Options
PET Progress	Enabled / Disabled
WatchDog	Disabled / Enabled
OS Timer	None
BIOS Timer	None
ASF Sensors Table	Disabled / Enabled

7.3.4.3 Secure Erase Configuration



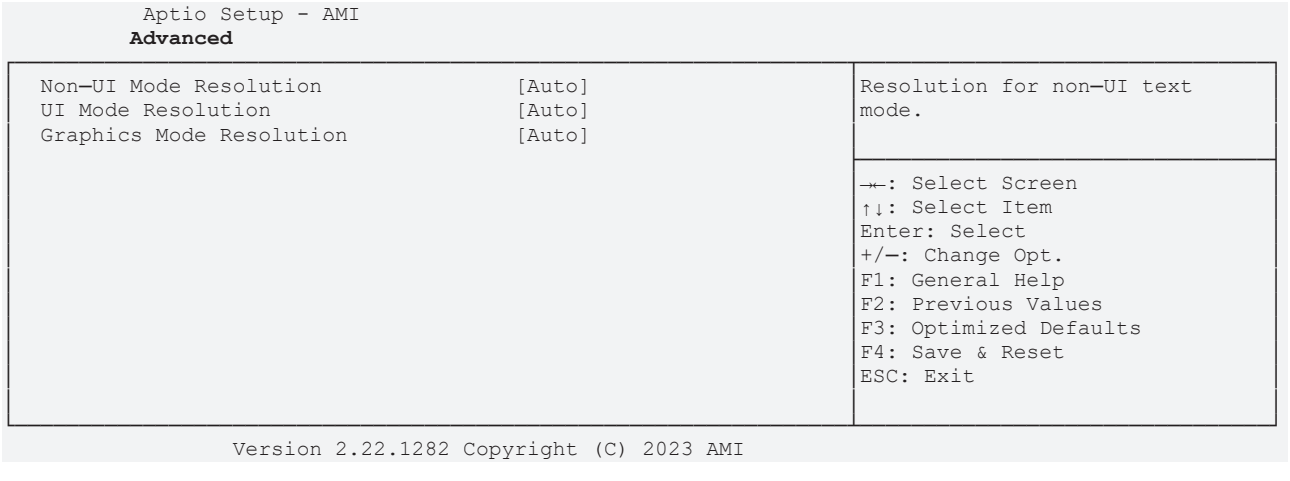
BIOS entry	Options
Secure Erase mode	Simulated / Real
Force Secure Erase	Disabled / Enabled

7.3.4.4 OEM Flags Settings



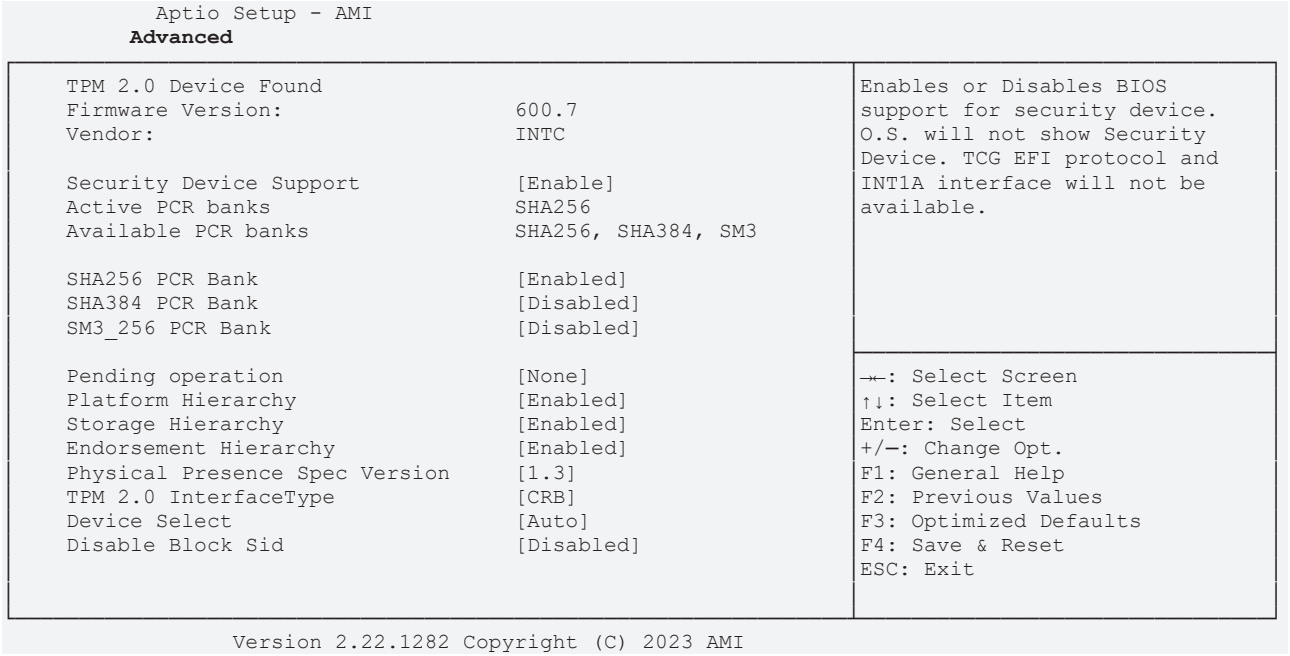
BIOS entry	Options
MBEx hotkey Pressed	Disabled / Enabled
MBEx Selection Screen	Disabled / Enabled
Hide Unconfigure ME Confirmation Prompt	Disabled / Enabled
MBEx OEM Debug Menu Enable	Disabled / Enabled
Unconfigure ME	Disabled / Enabled

7.3.4.5 MEBx Resolution Settings



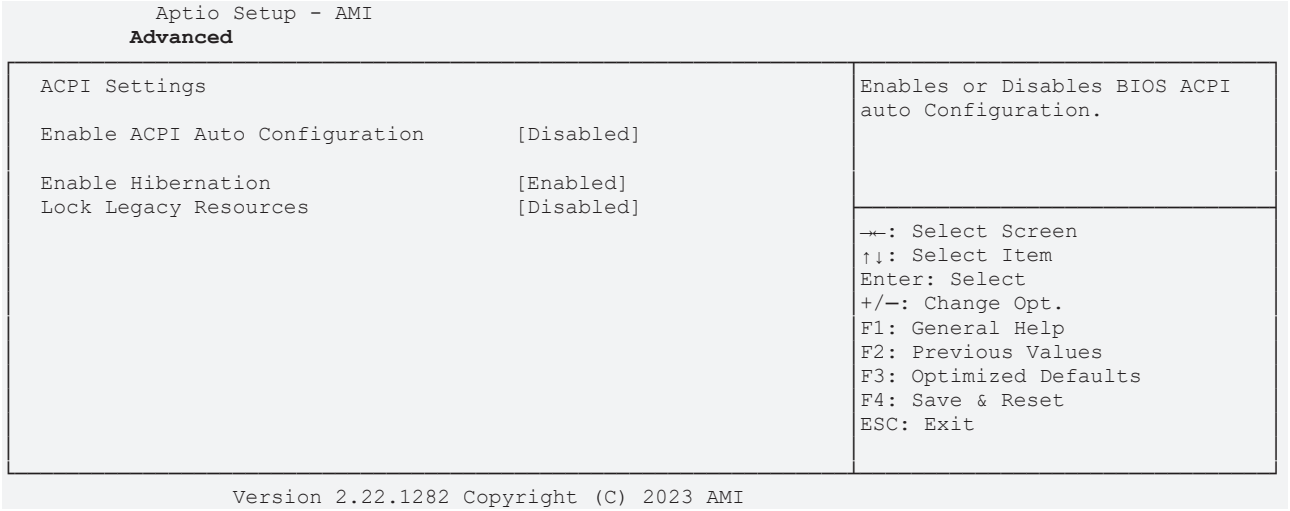
BIOS entry	Options
Non-UI Resolution	Auto / 80x25 / 100x31
UI Mode Resolution	Auto / 80x25 / 100x31
Graphics Mode Resolution	Auto / 640x480 / 800x600 / 1024x768

7.3.5 Trusted Computing



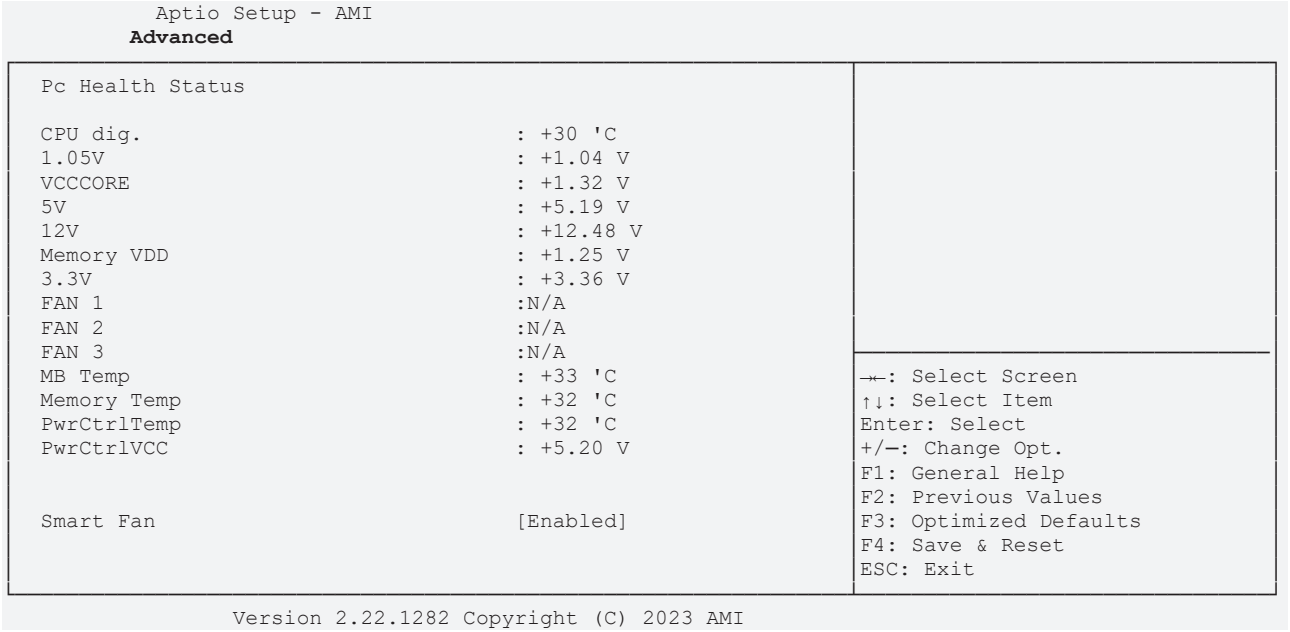
BIOS entry	Options
TPM 2.0 Device Found	
Firmware version:	600.7
Vendor:	INTC
Security Device Support	Enable / Disable
Active PCR banks	None
Available PCR banks	None
SHA256 PCR Bank	Enabled / Disabled
SHA384 PCR Bank	Disabled / Enabled
SM3_256 PCR Bank	Disabled / Enabled
Pending operation	None / TPM clear
Platform Hierarchy	Enabled / Disabled
Storage Hierarchy	Enabled / Disabled
Endorsement Hierarchy	Enabled / Disabled
Physical Presence Spec Version	1.3 / 1.2
TPM 2.0 InterfaceType	None
Device Select	Auto / TPM 1.2 / TPM 2.0
Disable Block Sid	Disabled / Enabled

7.3.6 ACPI Settings



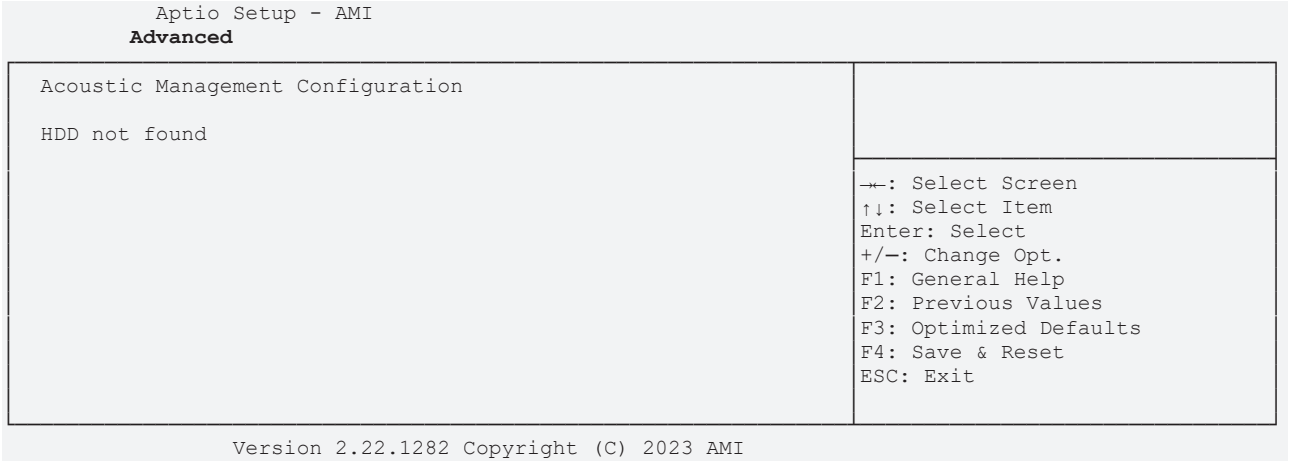
BIOS entry	Options
ACPI Settings	
Enable ACPI Auto Configuration	Disabled / Enabled
Enable Hibernation	Enabled / Disabled
Lock Legacy Resources	Disabled / Enabled

7.3.7 Hardware Monitor



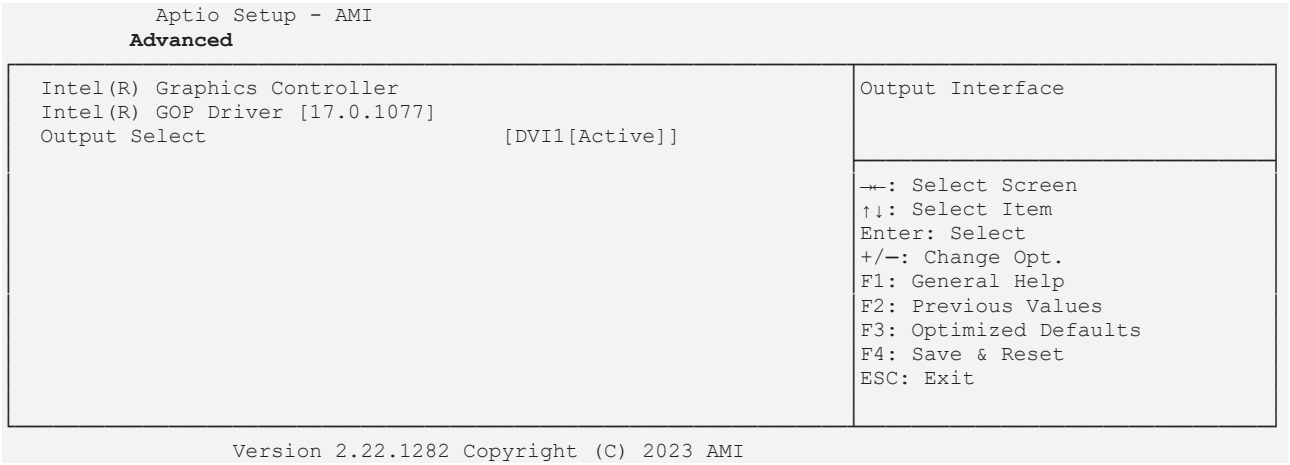
BIOS entry	Options
PC Health Status	None
CPU dig.	None
1.05V	None
VCCCORE	None
5 V	None
12 V	None
Memory VDD	None
3.3 V	None
FAN 1	None
FAN 2	None
FAN 3	None
MB Temp	None
Memory Temp	None
PwrCtrlTemp	None
PwrCtrlVCC	None
Smart Fan	Enabled / Disabled

7.3.8 Acoustic Management Configuration



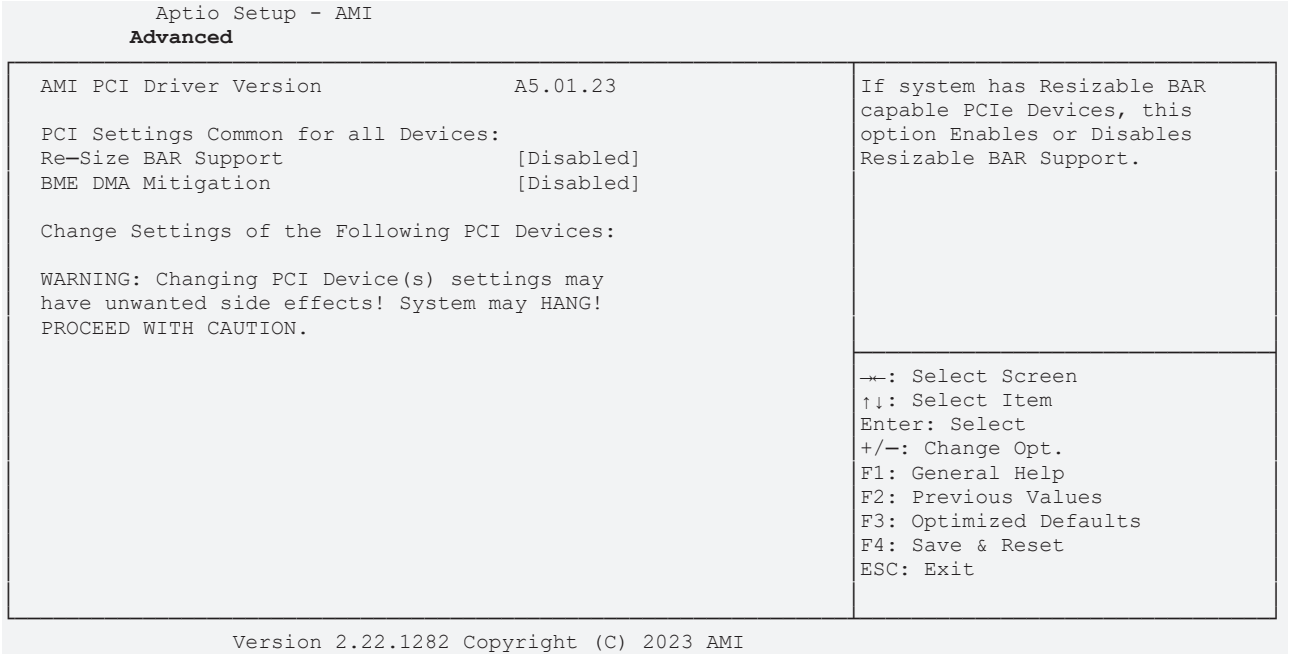
BIOS entry	Options
Acoustic Management Configuration	
HDD not found	

7.3.9 AMI Graphic Output Protocol Policy



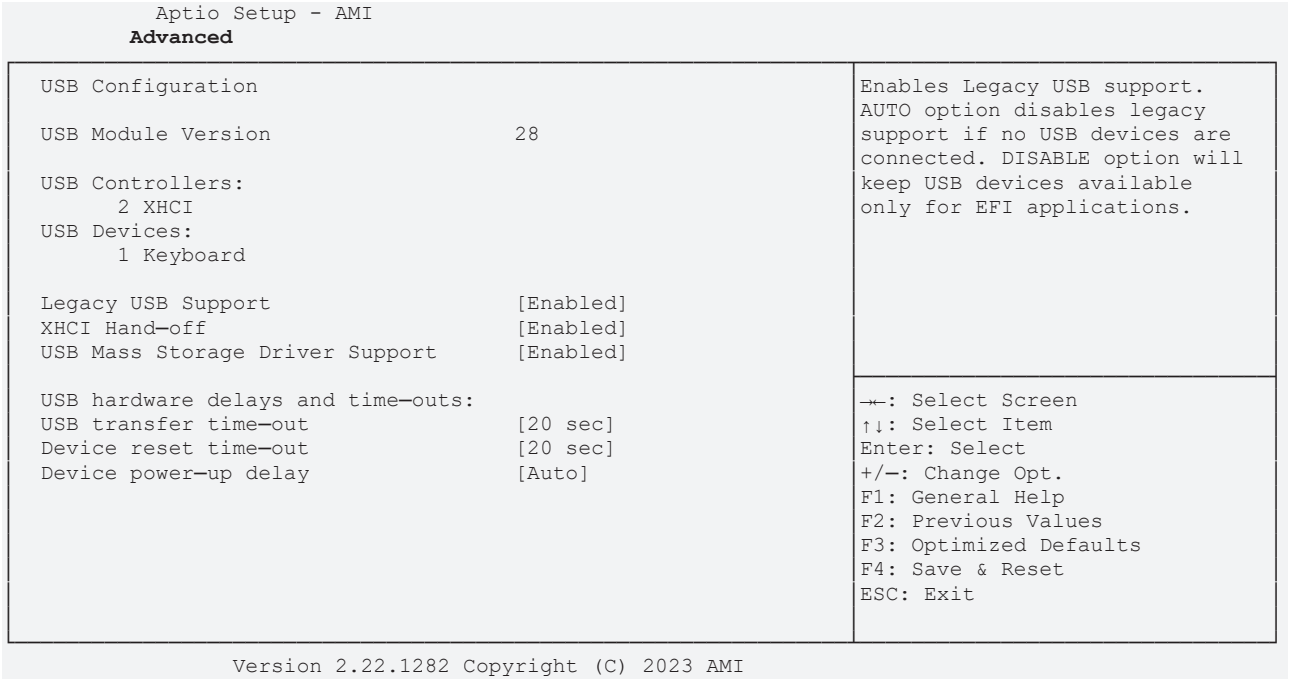
BIOS entry	Options
Intel® Graphics Controller Intel® GOP Driver [17.0.1077]	
Output Select	None

7.3.10 PCI Subsystem Settings



BIOS entry	Options
AMI PCI Driver Version: A5.01.23	
PCI Settings Common for all Devices:	
Re-Size BAR Support	Disabled / Enabled
BME DMA Mitigation	Disabled / Enabled
Change Settings of the Following PCI Devices:	
WARNING: Changing PCI Device(s) settings may have unwanted side effects! System may HANG! PROCEED WITH CAUTION.	

7.3.11 USB Configuration

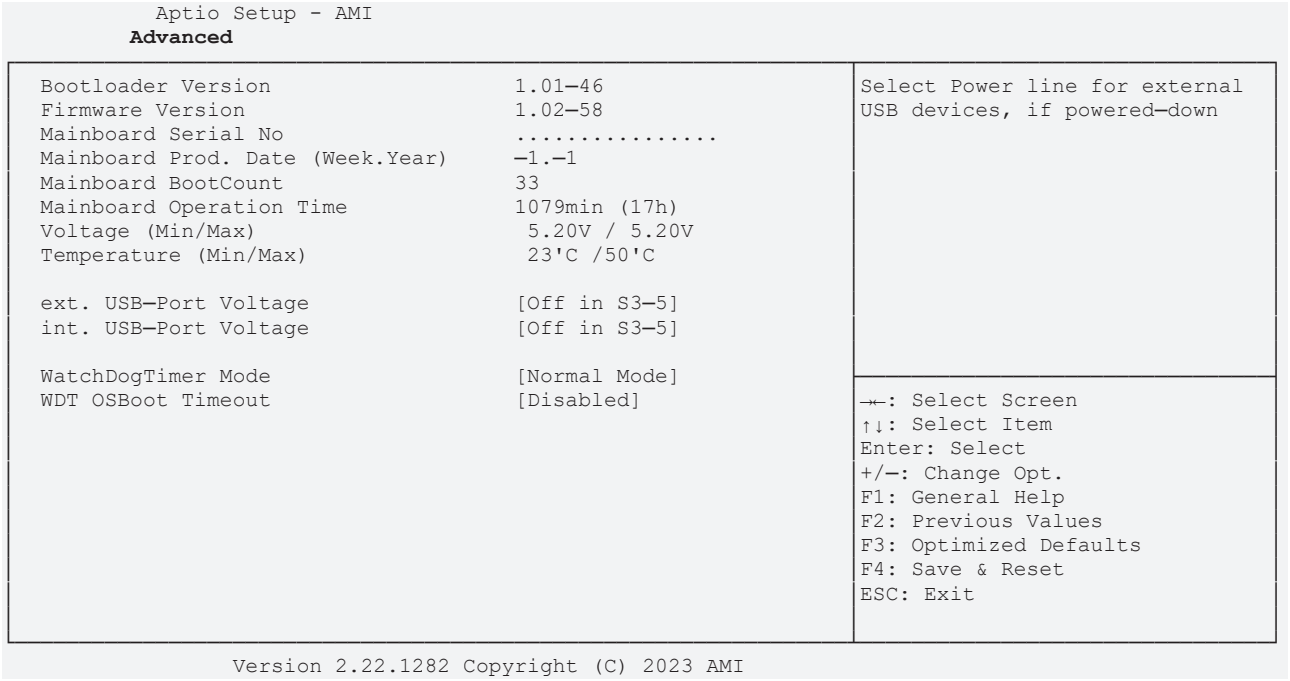


BIOS entry	Options
USB Configuration	
USB Module Version	None
USB Controllers: 2 XHCI	None
USB Devices: 1 Keyboard	None
Legacy USB Support	Enabled / Disabled
XHCI Hand-off	Enabled / Disabled
USB Mass Storage Driver Support	Enabled / Disabled
USB hardware delays and time-outs:	None
USB transfer time-out	20 sec (1, 5, 10, 20 sec)
Device reset time-out	20 sec (10, 20, 30, 40 sec)
Device power-up delay	Auto / Manual

7.3.12 Network Stack Configuration

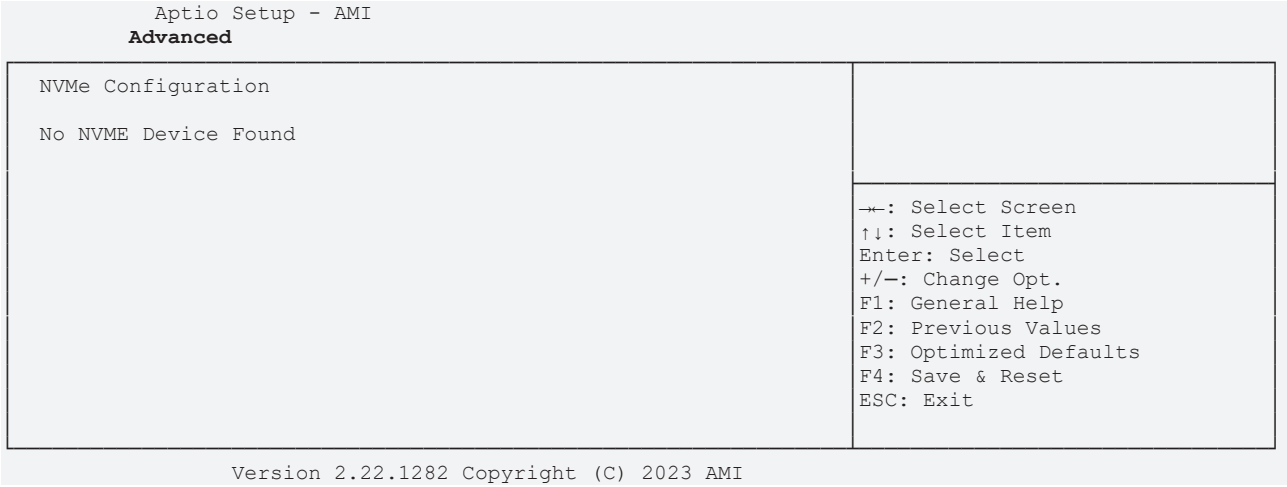
BIOS entry	Options
Network Stack	Enabled
Ipv4 PXE Support	Disabled / Enabled
Ipv4 HTTP Support	Disabled / Enabled
Ipv6 PXE Support	Disabled / Enabled
Ipv6 HTTP Support	Disabled / Enabled
PXE boot wait time	None
Media detect count	None

7.3.13 Power Controller Options



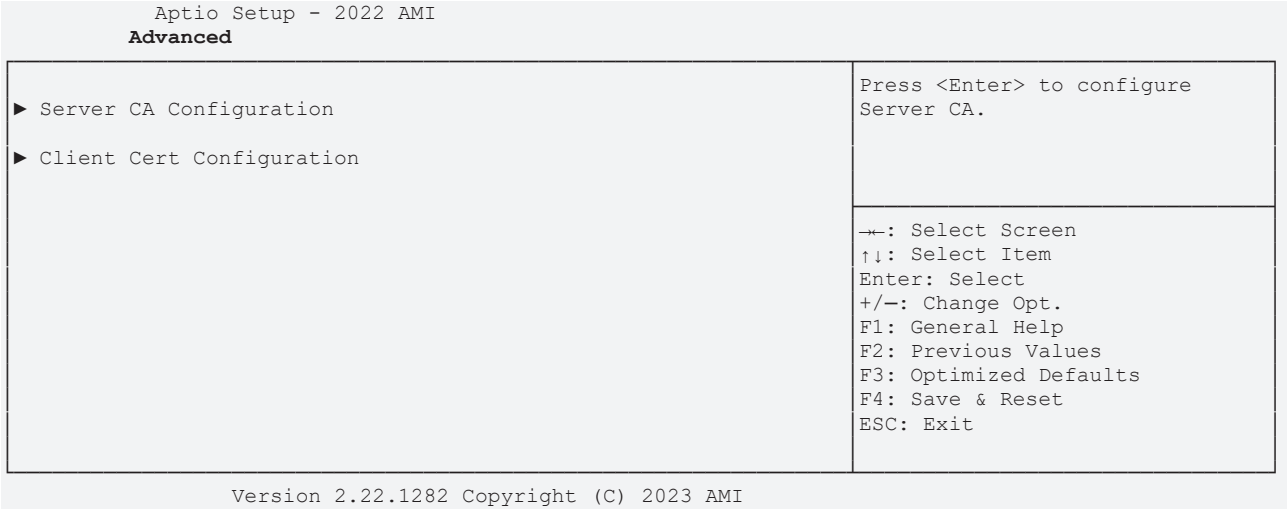
BIOS entry	Options
Bootloader version	None
Firmware version	None
Mainboard Serial No	None
Mainboard Prod. Date (Week.Year)	None
Mainboard BootCount	None
Mainboard Operation Time	None
Voltage (Min/Max)	None
Temperature (Min/Max)	None
ext. USB-Port Voltage	Off in S3-5 / by SVCC
int. USB-Port Voltage	Off in S3-5 / by SVCC
WatchDogTimer Mode	Normal Mode / Compatibility Mode
WDT OSBoot Timeout	Disabled / 45…255 Seconds (in steps +15)

7.3.14 NVMe Configuration



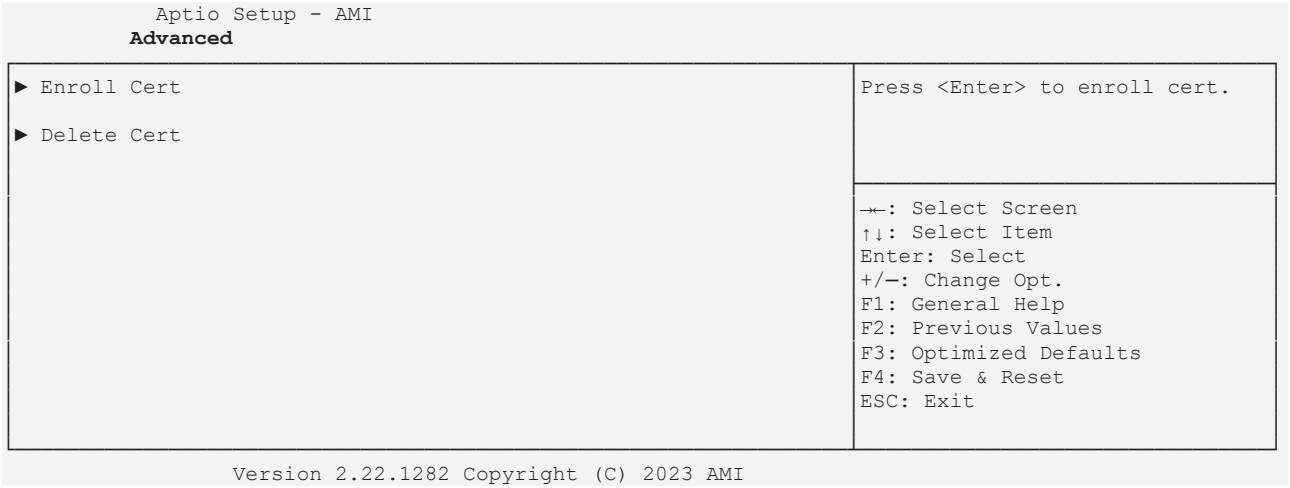
BIOS entry	Options
NVMe Configuration	
No NVME Device Found	None

7.3.15 TLs Auth Configuration



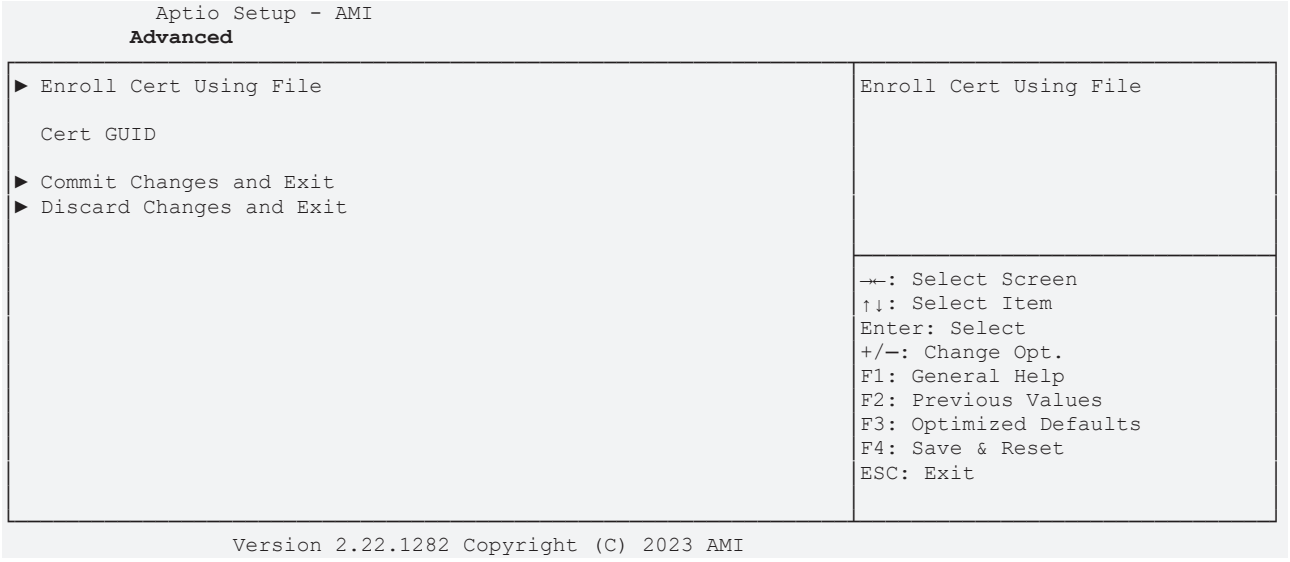
BIOS entry	Options
►Server CA Configuration	
►Client Cert Configuration	

7.3.15.1 Server CA Configuration



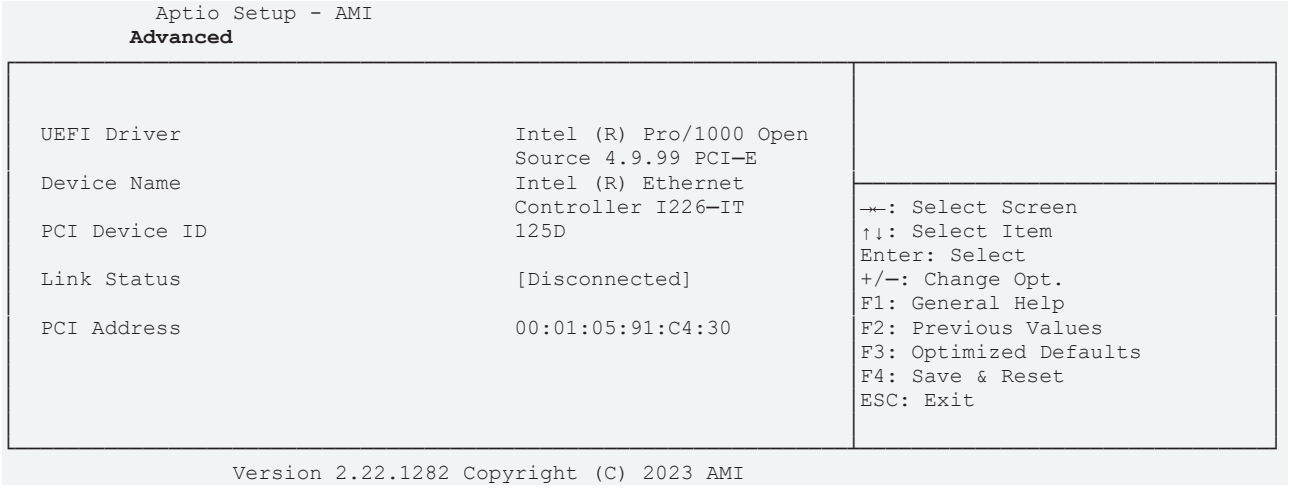
BIOS entry	Options
►Enroll Cert	Submenu see: Enroll Cert [▶ 54]
►Delete Cert	None

7.3.15.1.1 Enroll Cert



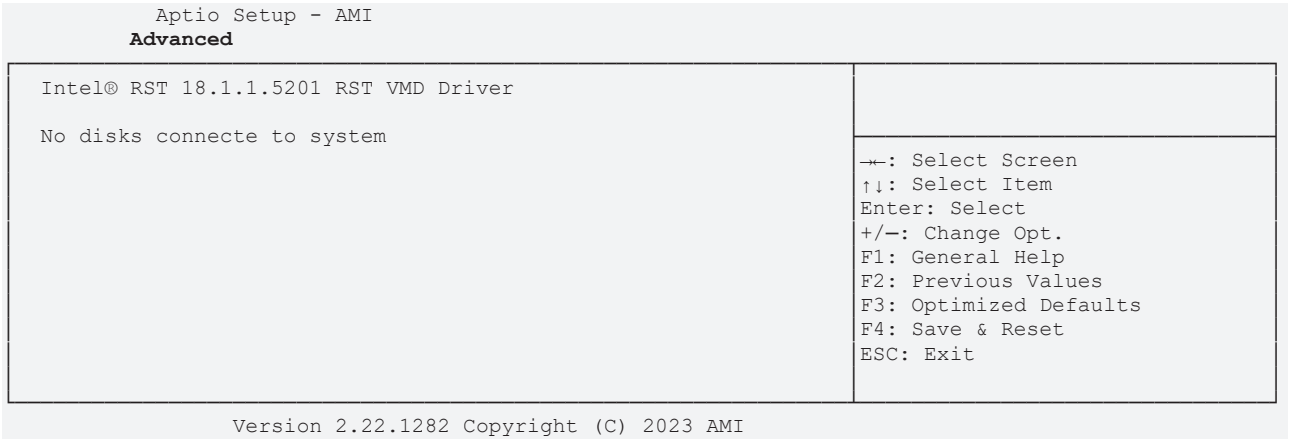
BIOS entry	Options
►Enroll Cert Using File	None
Cert GUID	None
►Commit Changes and Exit	None
►Discard Changes and Exit	None

7.3.16 Intel Ethernet Controller I226-IT



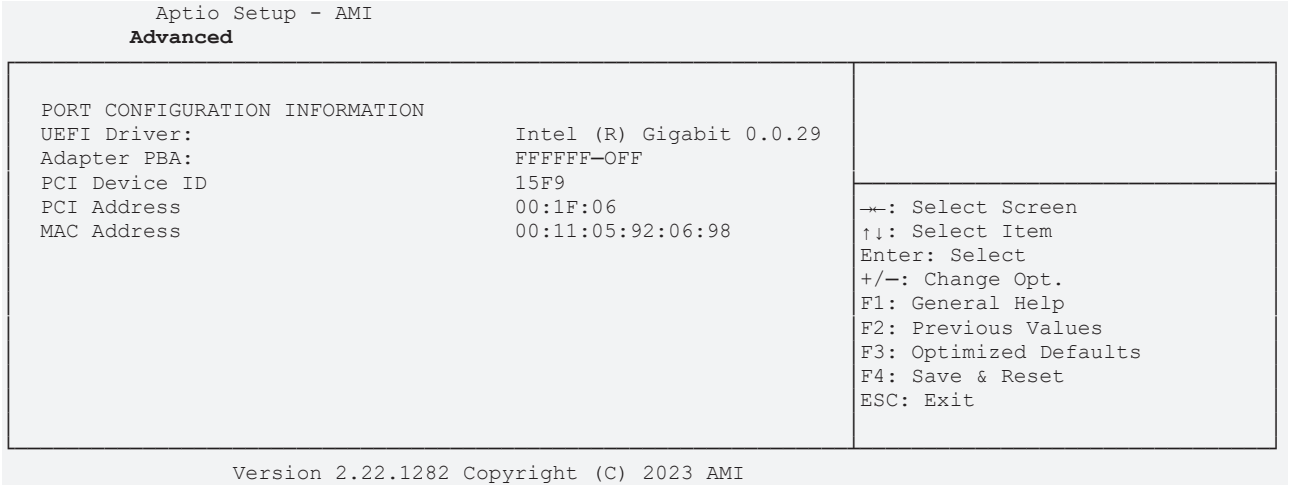
BIOS entry	Options
UEFI Driver	None
Device Name	None
PCI Device ID	None
Link Status	None
PCI Address	None

7.3.17 Intel Rapid Storage Technology



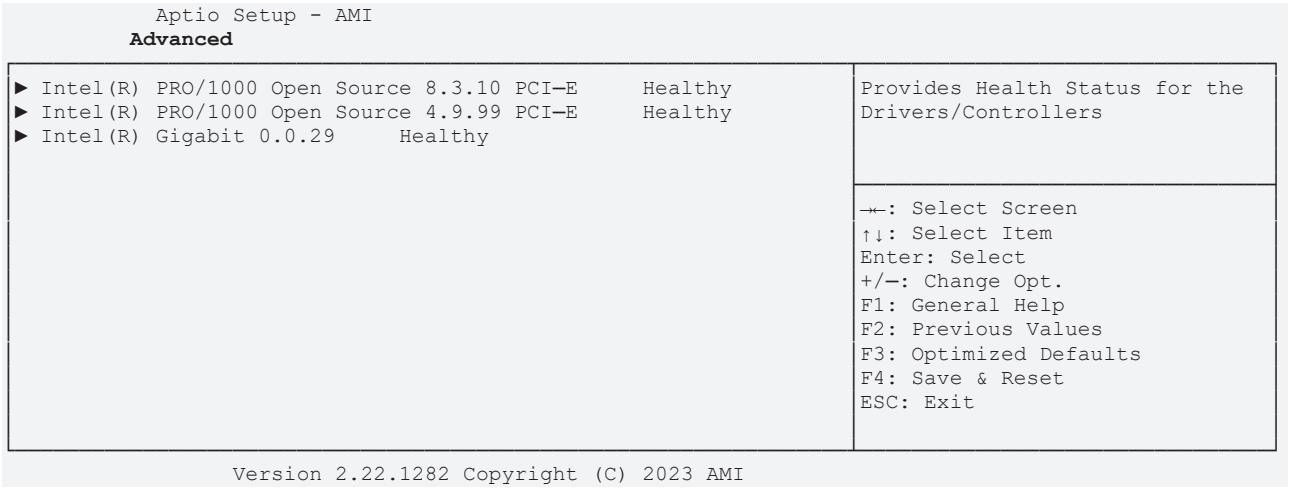
BIOS entry	Options
Intel® RST 18.1.15201 RST VMD Driver	None

7.3.18 Intel Ethernet Controller I219-LM



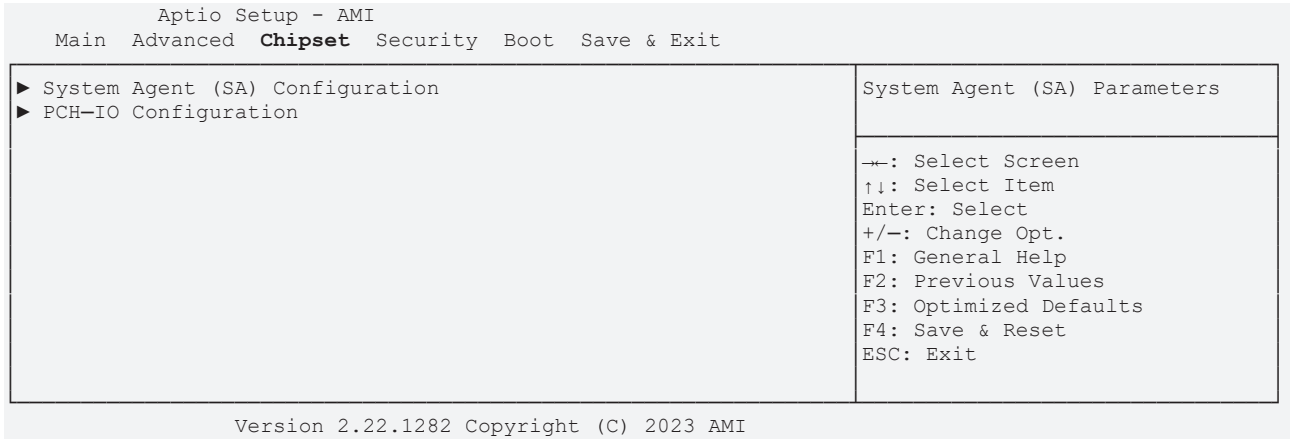
BIOS entry	Options
UEFI Driver	None
Device Name	None
PCI Device ID	None
Link Status	None
PCI Address	None

7.3.19 Driver Health



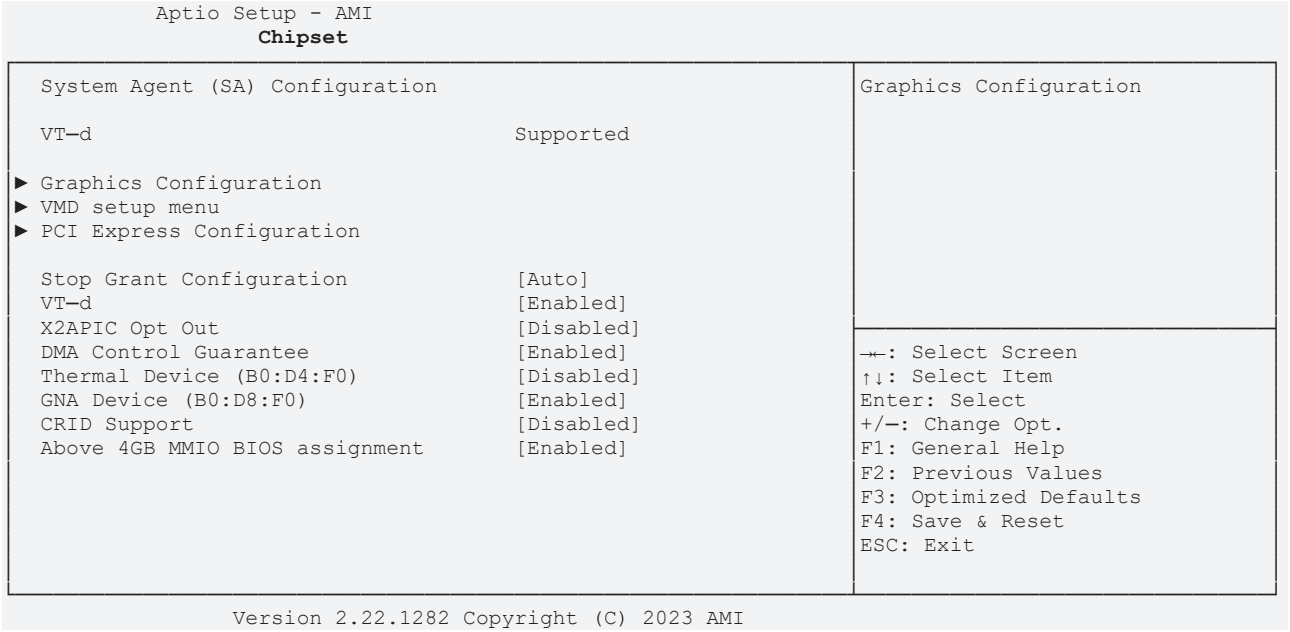
BIOS entry	Options
►Intel® PRO/1000 Open Source 8.3.10 PCI-E	None
►Intel® PRO/1000 Open Source 4.9.99 PCI-E	None
►Intel® Gigabit 0.0.29	None

7.4 Chipset CB3072



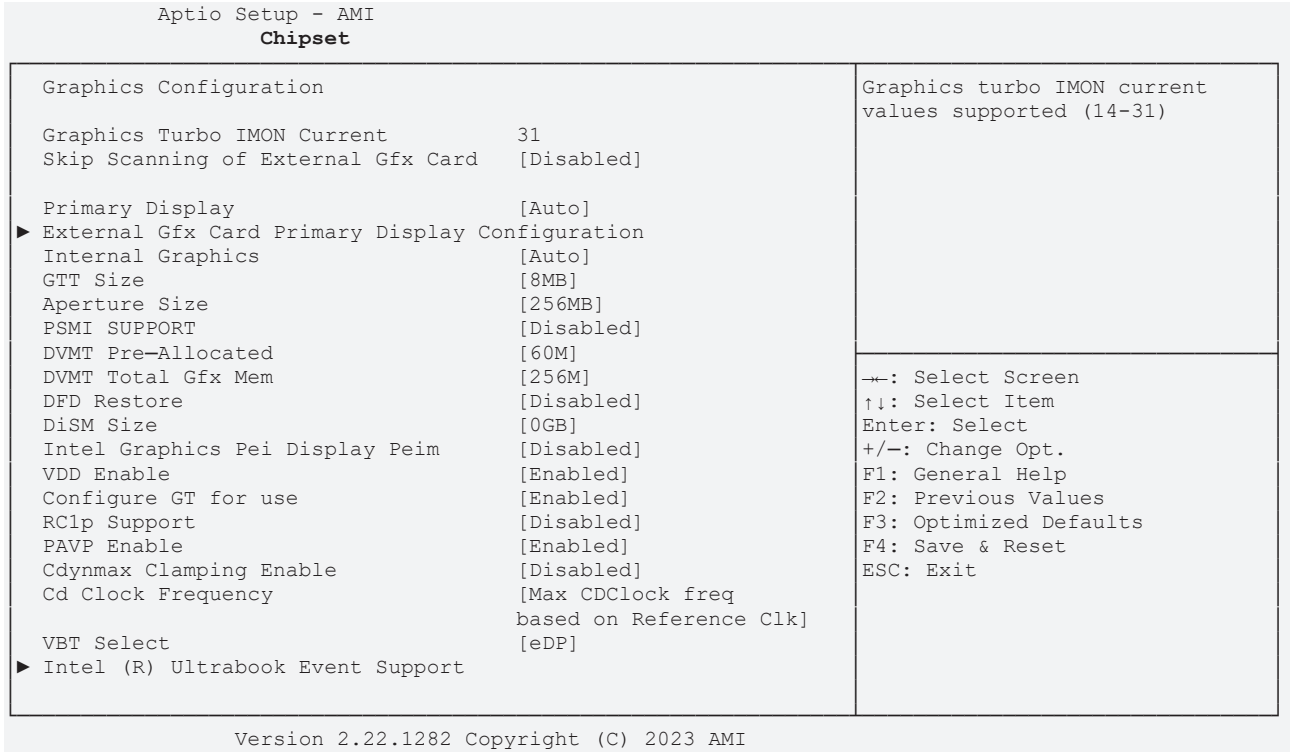
BIOS entry	Options
►System Agent (SA) Configuration	Submenu see: System Agent (SA) Configuration [▶ 58]
►PCH-IO Configuration	Submenu see: PCI Express Configuration [▶ 62]

7.4.1 System Agent (SA) Configuration



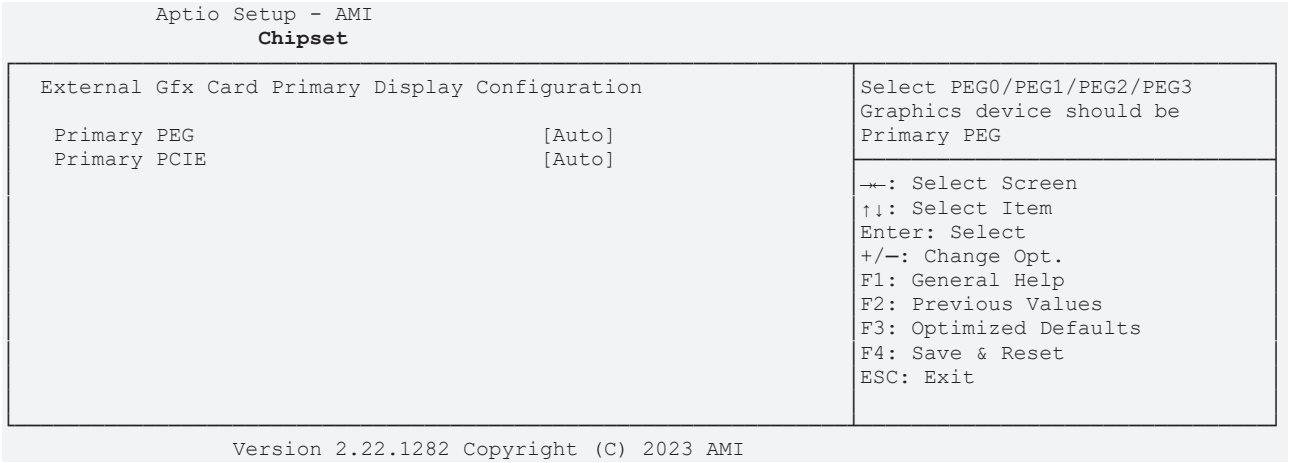
BIOS entry	Options
System Agent (SA) Configuration	
VT-d	None
▶Graphics Configuration	Submenu see: Graphics Configuration [▶ 59]
▶VMD setup menu	Submenu see: VMD setup menu [▶ 61]
▶PCI Express Configuration	Submenu see: PCI Express Configuration [▶ 62]
Stop Grant Configuration	Auto / Manual
VT-d	Enabled / Disabled
X2APIC Opt Out	Disabled / Enabled
DMA Control Guarantee	Enabled / Disabled
Thermal Device (B0:D4:F0)	Disabled / Enabled
GNA Device (B0:D8:F0)	Enabled / Disabled
CRID Support	Disabled / Enabled
Above 4GB MMIO BIOS assignment	Enabled / Disabled

7.4.1.1 Graphics Configuration



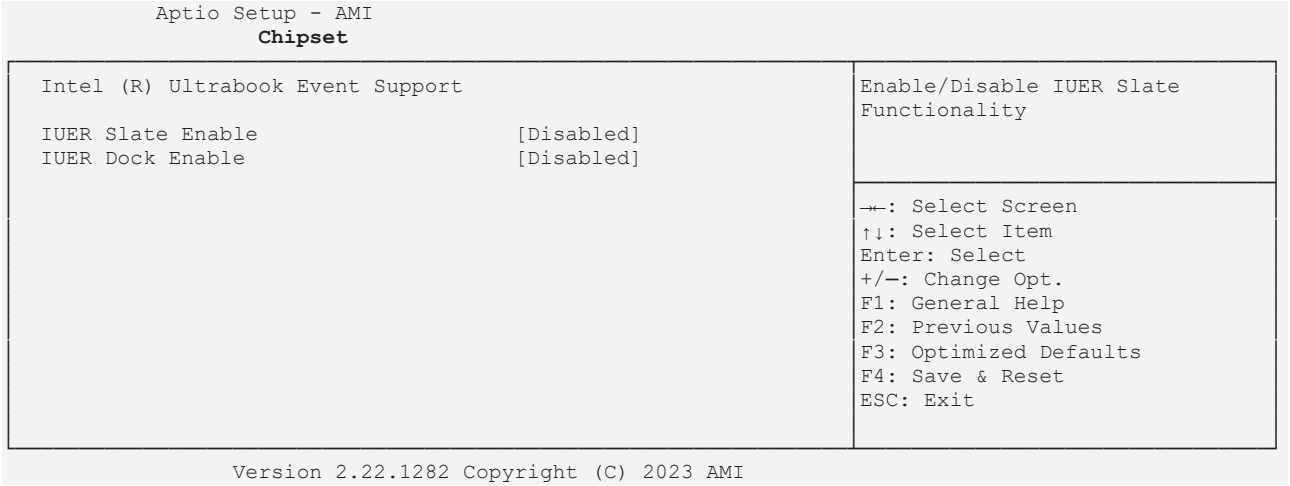
BIOS entry	Options
Graphics Configuration	
Graphics Turbo IMON Current	None
Skip Scanning of External Gfx Card	Disabled / Enabled
Primary Display	Auto / IGFX / PEG Slot / PCH PCI / HG
►External Gfx Card Primary Display Configuration	Submenu see: External Gfx Card Primary Display Configuration [▶ 60]
Internal Graphics	Auto / Disabled / Enabled
GTT Size	2 / 4 / 8 MB
Aperture Size	128 / 256 / 512 / 1024 MB
PSMI SUPPORT	Disabled / Enabled
DVMT Pre-Allocated	0M, 32M…64M, 96M, 128M, 160M
DVMT Total Gfx Mem	128M / 256M / MAX
DFD Restore	Disabled / Enabled
DiSM Size	0 – 7 GB
Intel Graphics Pei Display Peim	Disabled / Enabled
VDD Enable	Enabled / Disabled
Configure GT for use	Enabled / Disabled
RC1p Support	Disabled / Enabled
PAVP Enable	Enabled / Disabled
Cdynmax Clamping Enable	Enabled / Disabled
Cd Clock Frequency	192 / 307.2 / 326.4 / 556.8 / 652.8 Mhz Max CdClock freq based on Reference Clk
VBT Select	eDP / MIPI / eDP & HDMI / eDP & HDMI for TGLH
►Intel® Ultrabook Event Support	Submenu see: Intel Ultrabook Event Support [▶ 60]

7.4.1.1.1 External Gfx Card Primary Display Configuration



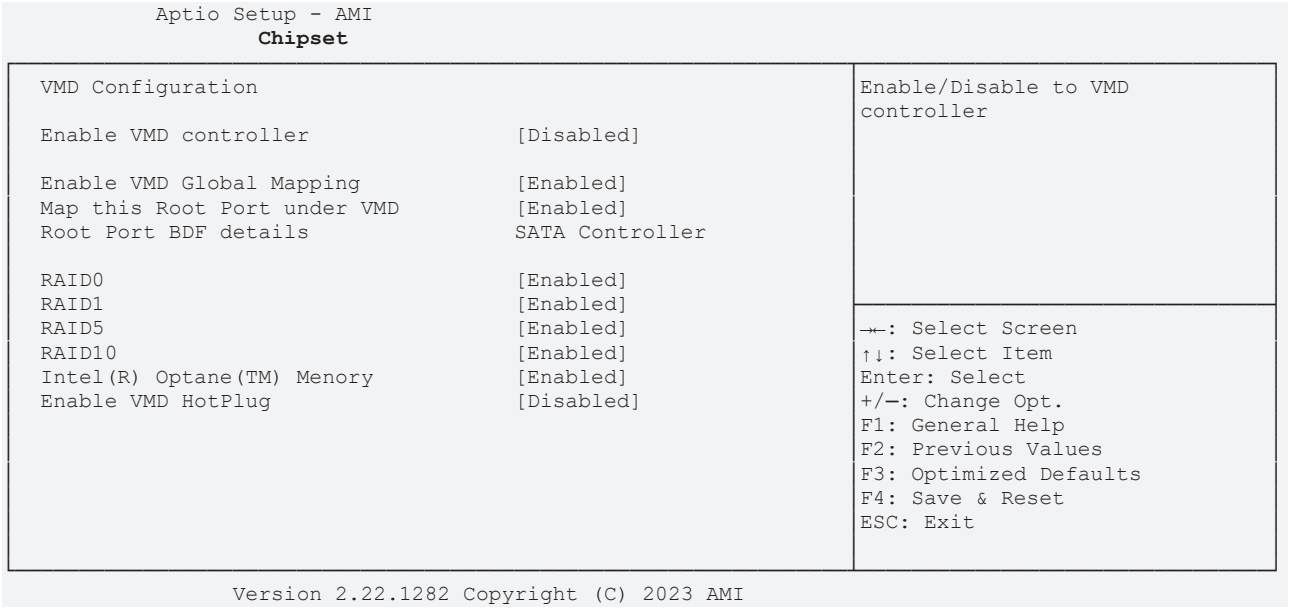
BIOS entry	Options
External Gfx Card Primary Display Configuration	
Primary PEG	Auto / PEG11 / PEG 12
Primary PCIE	Auto / PCI1 - PCIE19

7.4.1.1.2 Intel Ultrabook Event Support



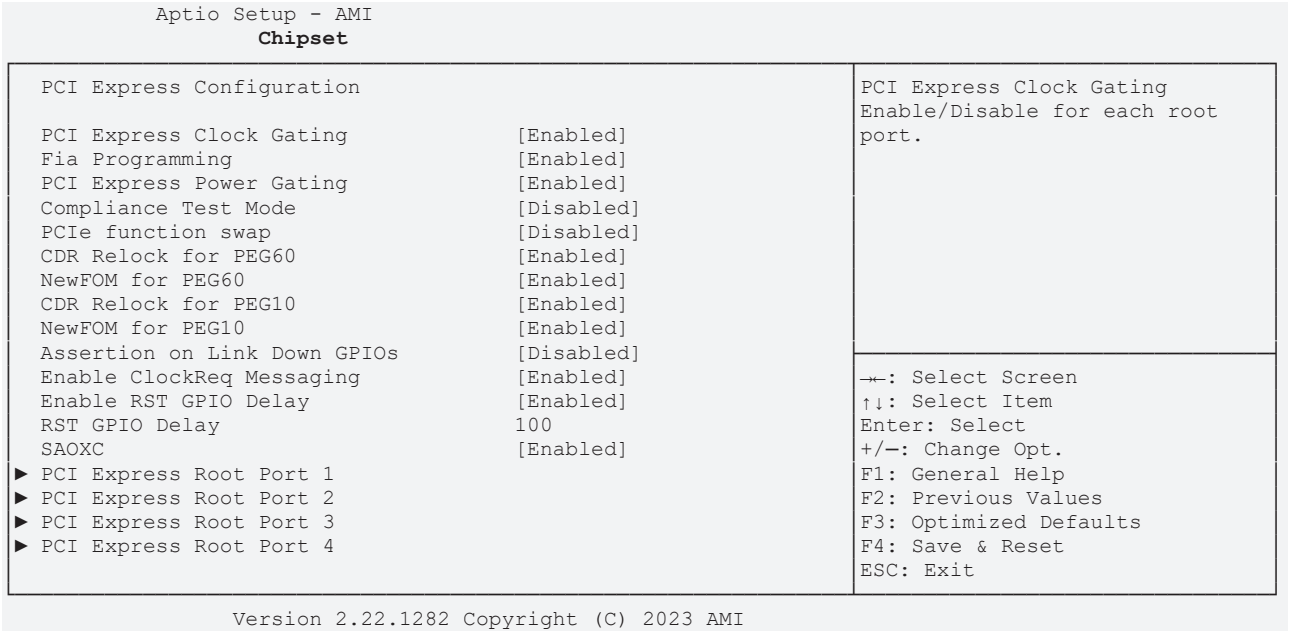
BIOS entry	Options
Intel® Ultrabook Event Support	
IUER Slate Enable	Disabled / Enabled
IUER Dock Enable	Disabled / Enabled

7.4.1.2 VMD setup menu



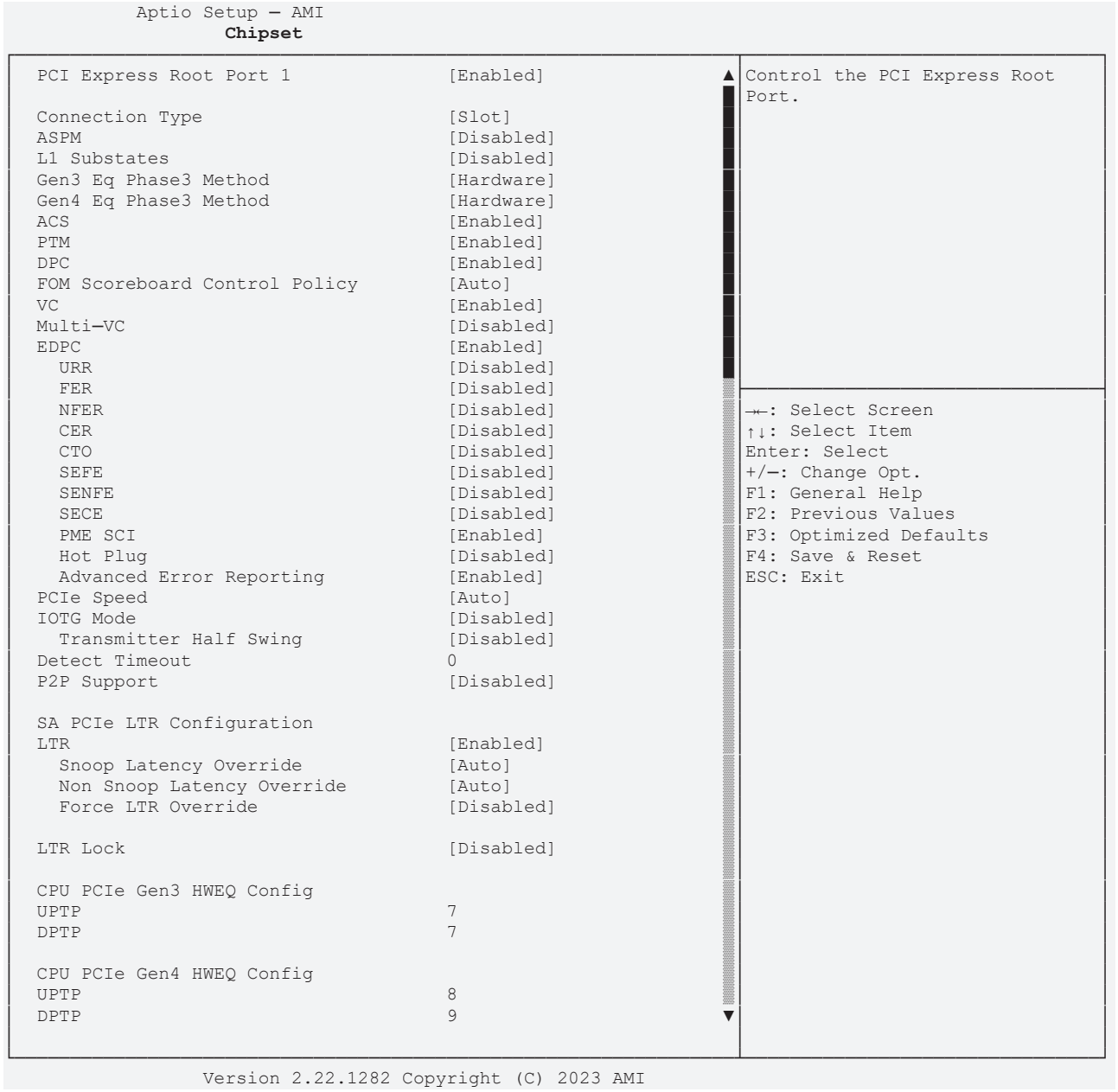
BIOS entry	Options
VMD Configuration	
Enable VMD controller	Enabled / Disabled
Enable VMD Global Mapping	Enabled / Disabled
Map this Root Port under VMD	Enabled / Disabled
Root Port BDF details	None
RAID0	Enabled / Disabled
RAID1	Enabled / Disabled
RAID5	Enabled / Disabled
RAID10	Enabled / Disabled
Intel® Optane™ Memory	Enabled / Disabled
Enable VMD HotPlug	Disabled / Enabled

7.4.1.3 PCI Express Configuration



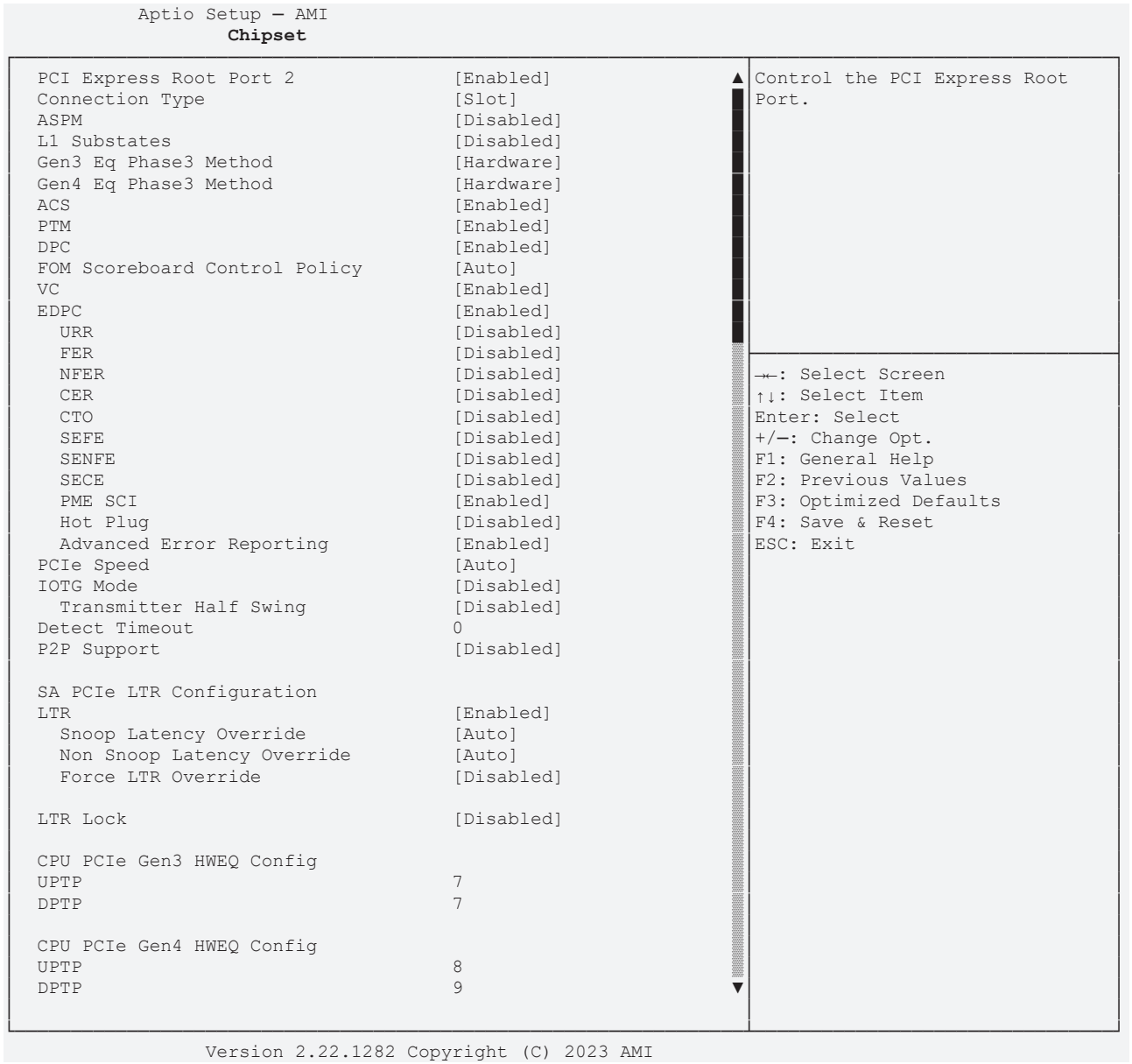
BIOS entry	Options
PCI Express Configuration	
PCI Express Clock Gating	Enabled / Disabled
Fia Programming	Enabled / Disabled
PCI Express Power Gating	Enabled / Disabled
Compliance Test Mode	Disabled / Enabled
PCIe function swap	Disabled / Enabled
CDR Relock for PEG60	Enabled / Disabled
NewFOM for PEG60	Enabled / Disabled
CDR Relock for PEG10	Enabled / Disabled
NewFOM for PEG10	Enabled / Disabled
Assertion on Link Down GPIOs	Disabled / Enabled
Enable ClockReq Messaging	Enabled / Disabled
Enable RST GPIO Delay	Enabled / Disabled
RST GPIO Delay	None
SAOXC	Enabled / Disabled
▶PCI Express Root Port 1	Submenu see: PCI Express Root Port 1 [▶ 63]
▶PCI Express Root Port 2	Submenu see: PCI Express Root Port 2 [▶ 65]
▶PCI Express Root Port 3	Submenu see: PCI Express Root Port 3 [▶ 67]
▶PCI Express Root Port 4	Submenu see: PCI Express Root Port 4 [▶ 69]

7.4.1.3.1 PCI Express Root Port 1



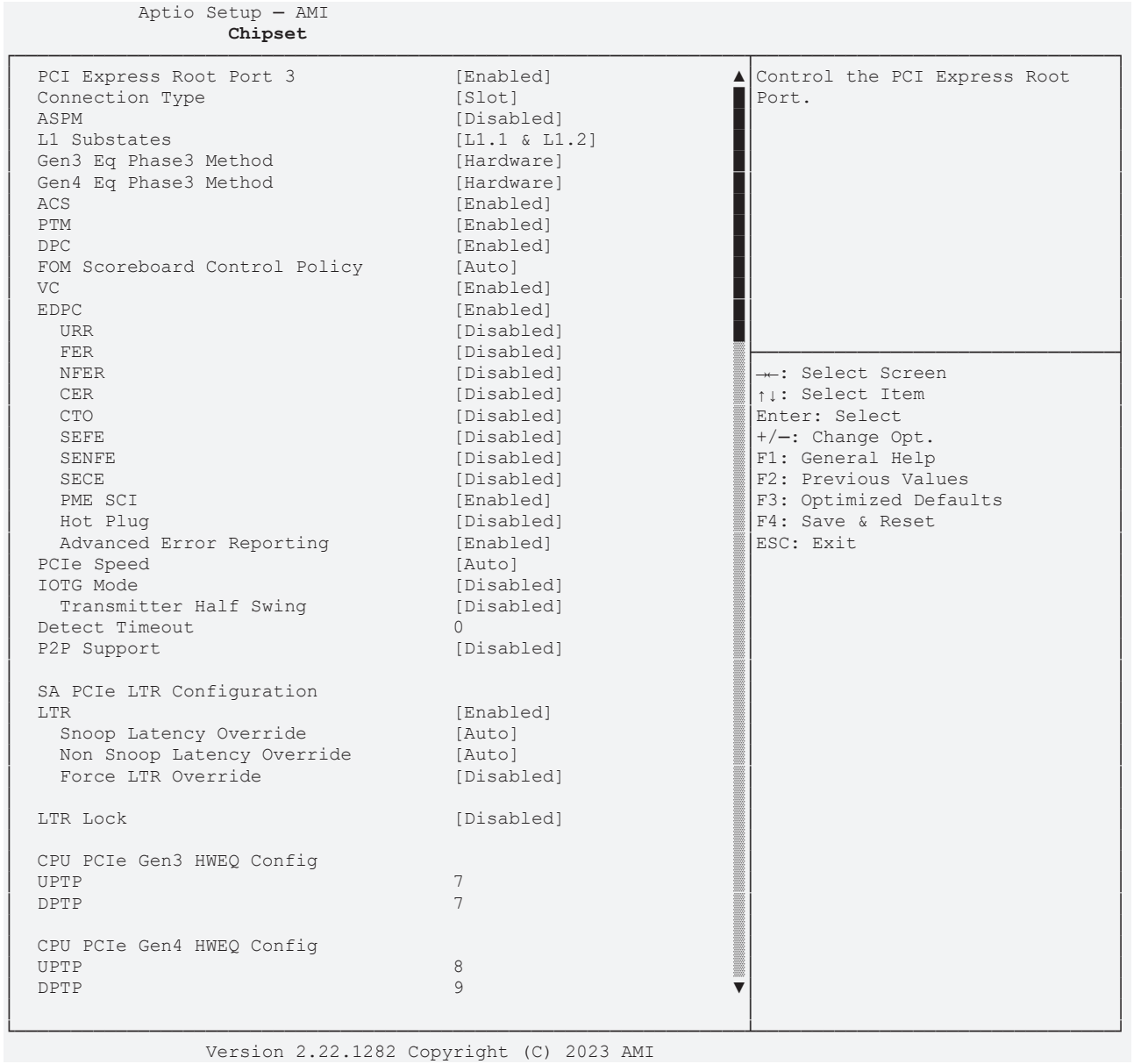
BIOS entry	Options
PCI Express Root Port 1	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
Gen3 Eq Phase3 Method	Hardware / Static Coeff.
Gen4 Eq Phase3 Method	Hardware / Static Coeff.
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
FOM Scoreboard Control Policy	Auto / Gen3 / Gen4 / Gen3 / Gen4
VC	Disabled / Enabled
Multi-VC	Disabled / Enabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
CTO	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Enabled / Disabled
Hot Plug	None
Advanced Error Reporting	Disabled / Enabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3 / Gen4
IOTG Mode	Disabled / Enabled
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
PSP Support	Disabled / Enabled
SA PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled
CPU PCIe Gen3 HWEQ Config	
UPTP	None
DPTP	None
CPU PCIe Gen HWEQ Config	
UPTP	None
DPTP	None

7.4.1.3.2 PCI Express Root Port 2



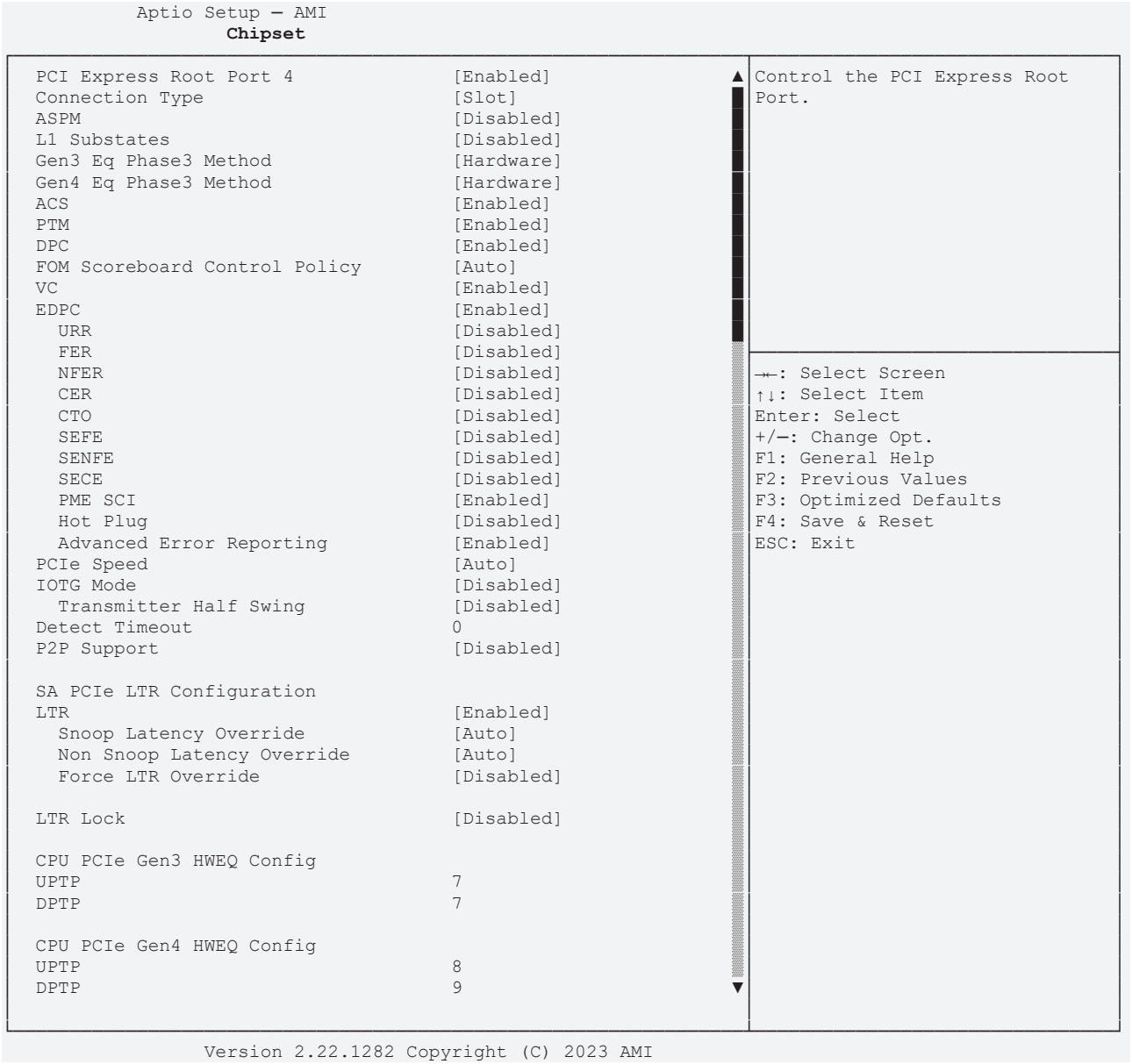
BIOS entry	Options
PCI Express Root Port 2	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
Gen3 Eq Phase3 Method	Hardware / Static Coeff.
Gen4 Eq Phase3 Method	Hardware / Static Coeff.
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
FOM Scoreboard Control Policy	Auto / Gen3 / Gen4 / Gen3 / Gen4
VC	Disabled / Enabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
CTO	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Enabled / Disabled
Hot Plug	None
Advanced Error Reporting	Disabled / Enabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3 / Gen4
IOTG Mode	Disabled / Enabled
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
PSP Support	Disabled / Enabled
SA PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled
CPU PCIe Gen3 HWEQ Config	
UPTP	None
DPTP	None
CPU PCIe Gen HWEQ Config	
UPTP	None
DPTP	None

7.4.1.3.3 PCI Express Root Port 3



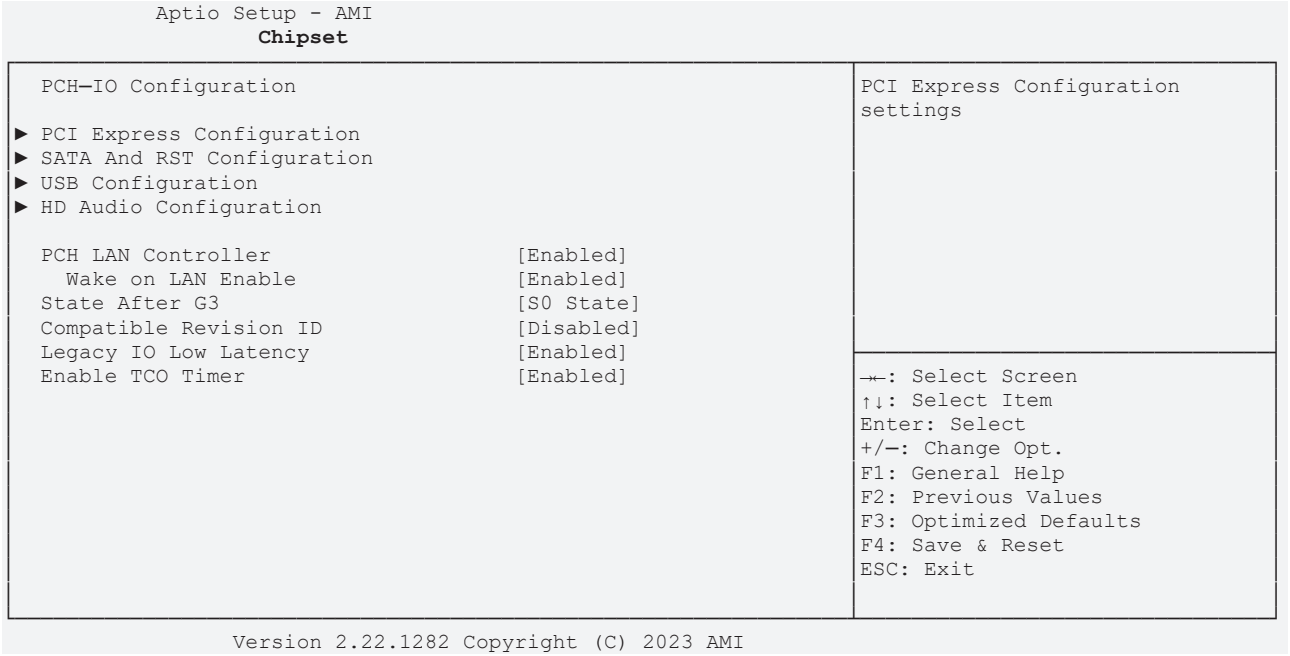
BIOS entry	Options
PCI Express Root Port 3	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
Gen3 Eq Phase3 Method	Hardware / Static Coeff.
Gen4 Eq Phase3 Method	Hardware / Static Coeff.
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
FOM Scoreboard Control Policy	Auto / Gen3 / Gen4 / Gen3 / Gen4
VC	Disabled / Enabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
CTO	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Enabled / Disabled
Hot Plug	None
Advanced Error Reporting	Disabled / Enabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3 / Gen4
IOTG Mode	Disabled / Enabled
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
PSP Support	Disabled / Enabled
SA PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled
CPU PCIe Gen3 HWEQ Config	
UPTP	None
DPTP	None
CPU PCIe Gen HWEQ Config	
UPTP	None
DPTP	None

7.4.1.3.4 PCI Express Root Port 4



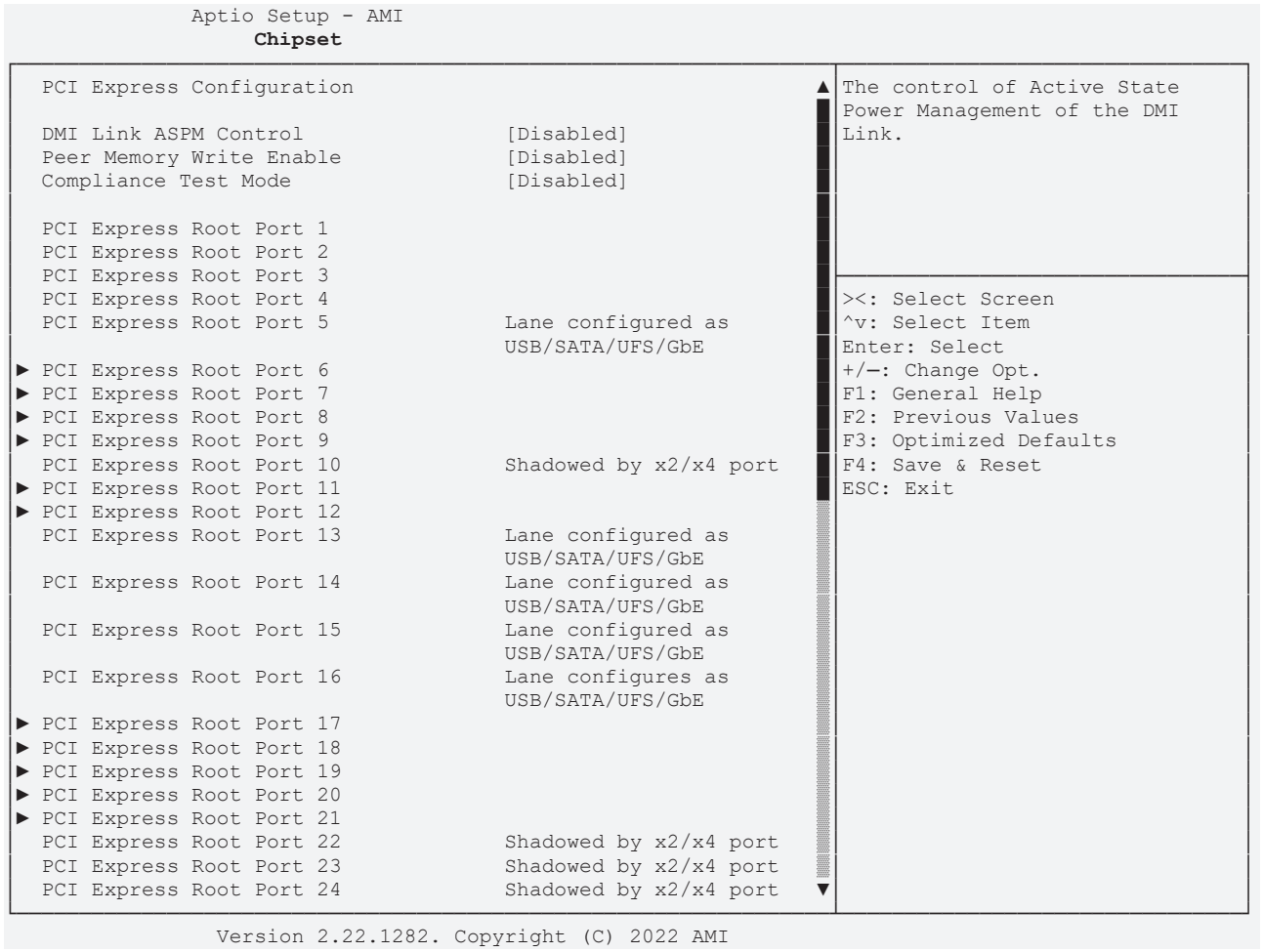
BIOS entry	Options
PCI Express Root Port 4	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
Gen3 Eq Phase3 Method	Hardware / Static Coeff.
Gen4 Eq Phase3 Method	Hardware / Static Coeff.
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
FOM Scoreboard Control Policy	Auto / Gen3 / Gen4 / Gen3 / Gen4
VC	Disabled / Enabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
CTO	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Enabled / Disabled
Hot Plug	None
Advanced Error Reporting	Disabled / Enabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3 / Gen4
IOTG Mode	Disabled / Enabled
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
PSP Support	Disabled / Enabled
SA PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled
CPU PCIe Gen3 HWEQ Config	
UPTP	None
DPTP	None
CPU PCIe Gen HWEQ Config	
UPTP	None
DPTP	None

7.4.2 PCH-IO Configuration



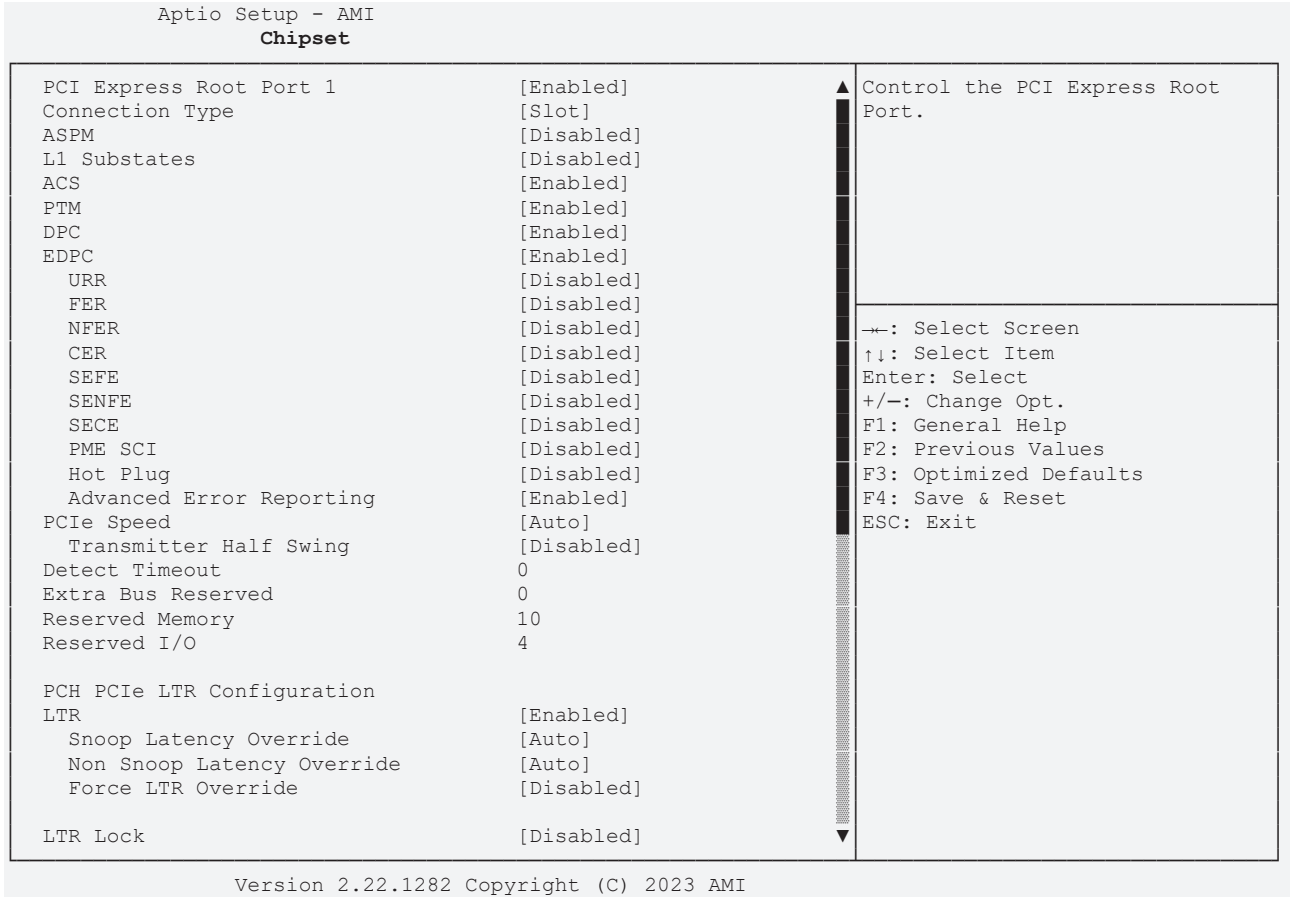
BIOS entry	Options
PCH-IO Configuration	
▶PCI Express Configuration	Submenu see: PCI Express Configuration [▶ 72]
▶SATA And RST Configuration	Submenu see: SATA And RST Configuration [▶ 104]
▶USB Configuration	Submenu see: USB Configuration [▶ 107]
▶HD Audio Configuration	Submenu see: HD Audio Configuration [▶ 108]
PCH LAN Controller	Enabled / Disabled
Wake on LAN Enable	S0 State / S5 State
State After G3	Disabled / Enabled
Compatible Revision ID	None
Legacy IO Low Latency	Disabled / Enabled
Enable TCO Timer	Enabled / Disabled

7.4.2.1 PCI Express Configuration



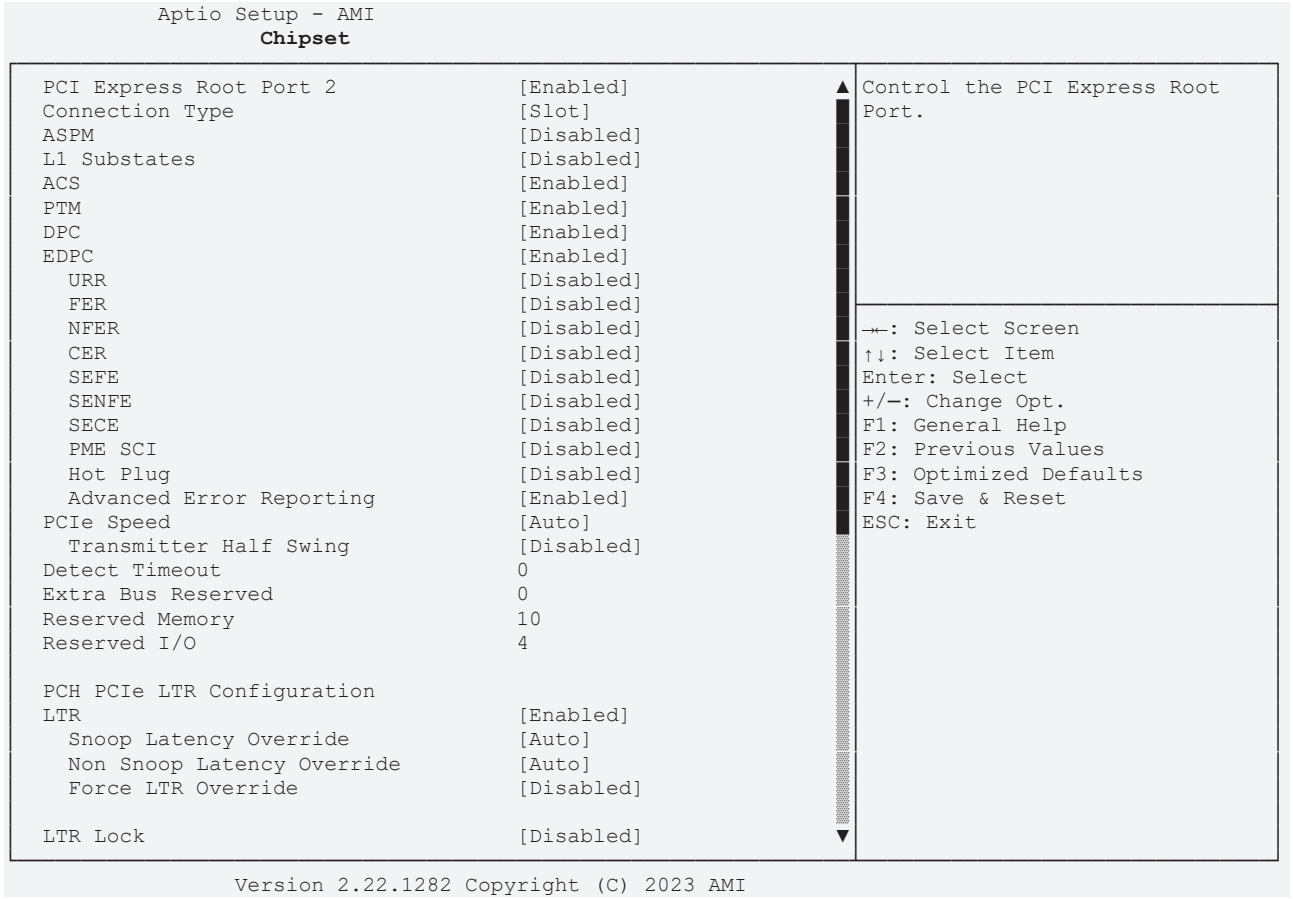
BIOS entry	Options
PCI Express Configuration	
DMI Link ASPM Control	Disabled / L0s / L1 / L0sL1 / Auto
Peer Memory Write Enable	Disabled / Enabled
Compliance Test Mode	Disabled / Enabled
►PCI Express Root Port 1	Submenu see: PCI Express Root Port 1 [▶ 74]
►PCI Express Root Port 2	Submenu see: PCI Express Root Port 2 [▶ 76]
►PCI Express Root Port 3	Submenu see: PCI Express Root Port 3 [▶ 78]
►PCI Express Root Port 4	Submenu see: PCI Express Root Port 4 [▶ 80]
PCI Express Root Port 5	None
►PCI Express Root Port 6	Submenu see: PCI Express Root Port 6 [▶ 82]
►PCI Express Root Port 7	Submenu see: PCI Express Root Port 7 [▶ 84]
►PCI Express Root Port 8	Submenu see: PCI Express Root Port 8 [▶ 86]
►PCI Express Root Port 9	Submenu see: PCI Express Root Port 9 [▶ 88]
PCI Express Root Port 10	None
►PCI Express Root Port 11	Submenu see: PCI Express Root Port 11 [▶ 90]
►PCI Express Root Port 12	Submenu see: PCI Express Root Port 12 [▶ 92]
PCI Express Root Port 13	None
PCI Express Root Port 14	None
PCI Express Root Port 15	None
PCI Express Root Port 16	None
►PCI Express Root Port 17	Submenu see: PCI Express Root Port 17 [▶ 94]
► PCI Express Root Port 18	Submenu see: PCI Express Root Port 18 [▶ 96]
►PCI Express Root Port 19	Submenu see: PCI Express Root Port 19 [▶ 98]
►PCI Express Root Port 20	Submenu see: PCI Express Root Port 20 [▶ 100]
►PCI Express Root Port 21	Submenu see: PCI Express Root Port 21 [▶ 102]
PCI Express Root Port 22	None
PCI Express Root Port 23	None
PCI Express Root Port 24	None

7.4.2.1.1 PCI Express Root Port 1



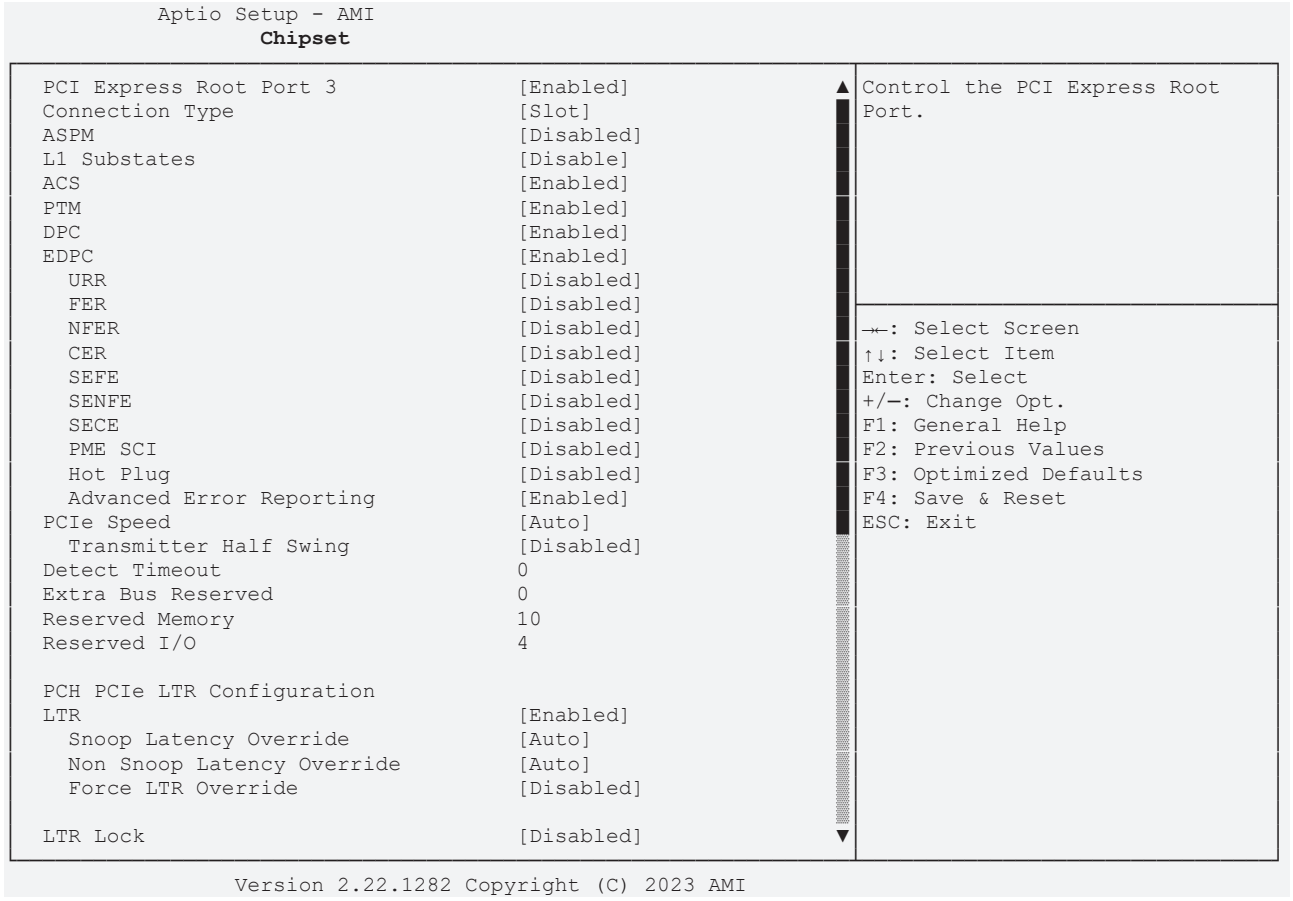
BIOS entry	Options
PCI Express Root Port 1	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

7.4.2.1.2 PCI Express Root Port 2



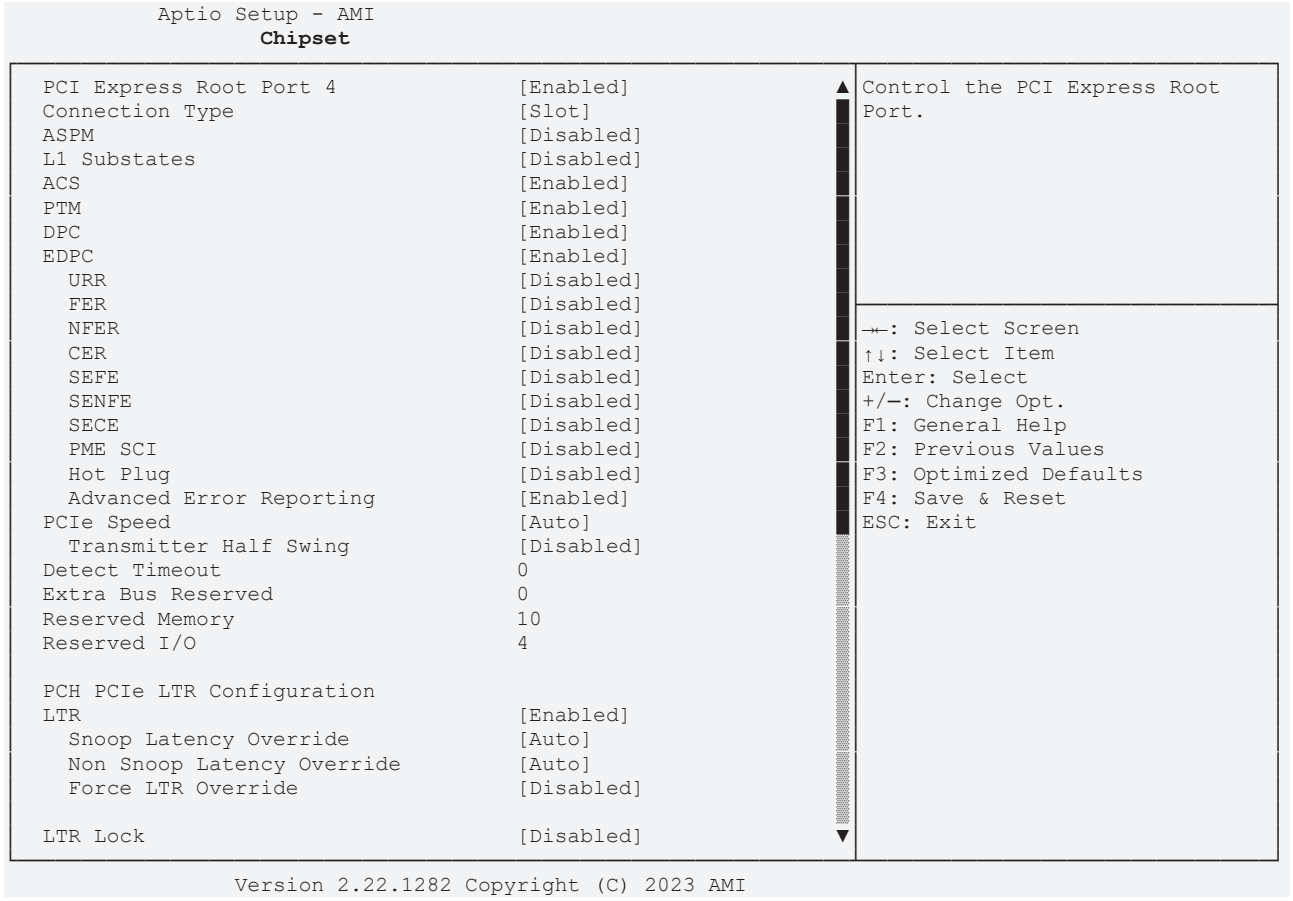
BIOS entry	Options
PCI Express Root Port 2	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

7.4.2.1.3 PCI Express Root Port 3



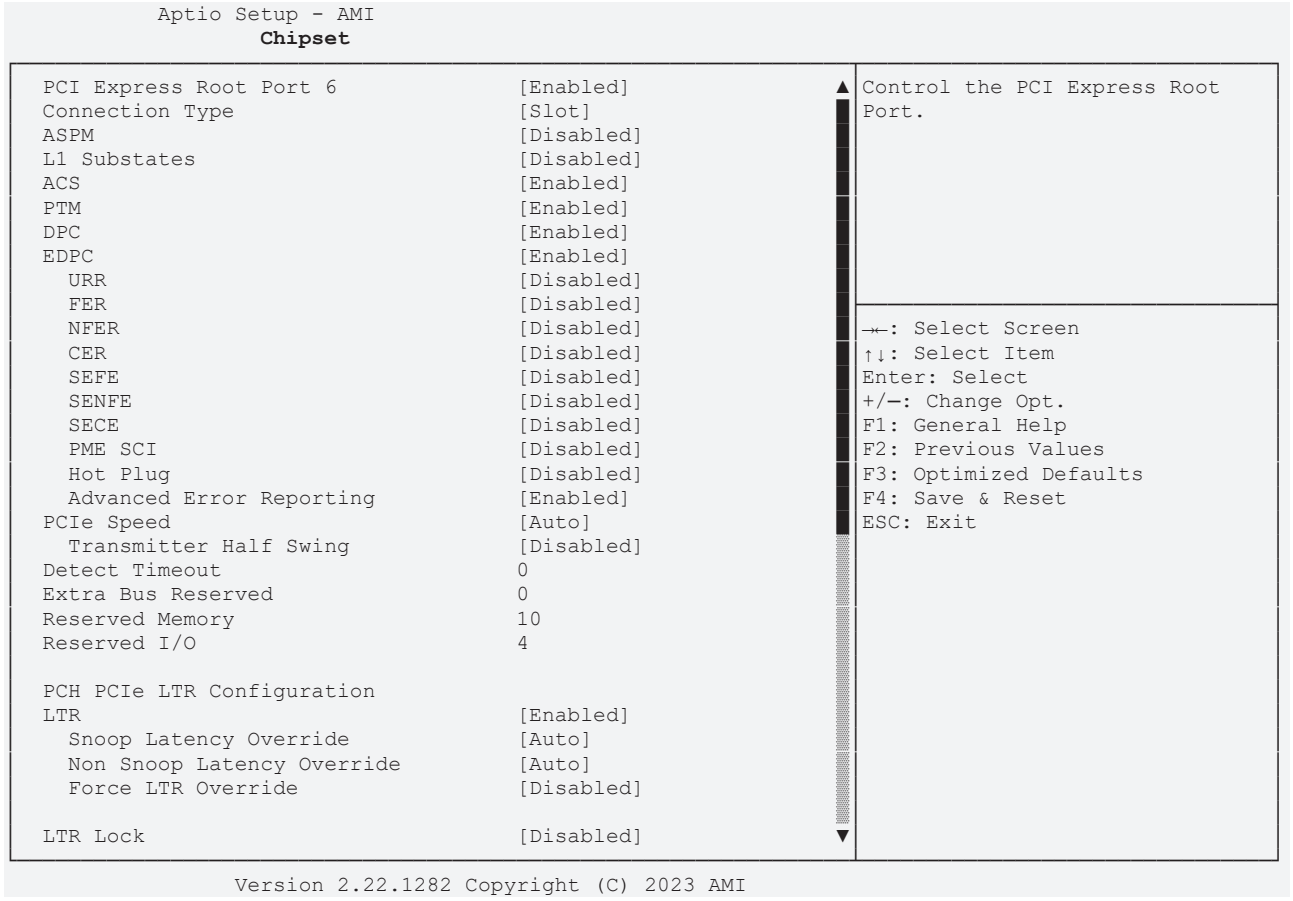
BIOS entry	Options
PCI Express Root Port 3	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

7.4.2.1.4 PCI Express Root Port 4



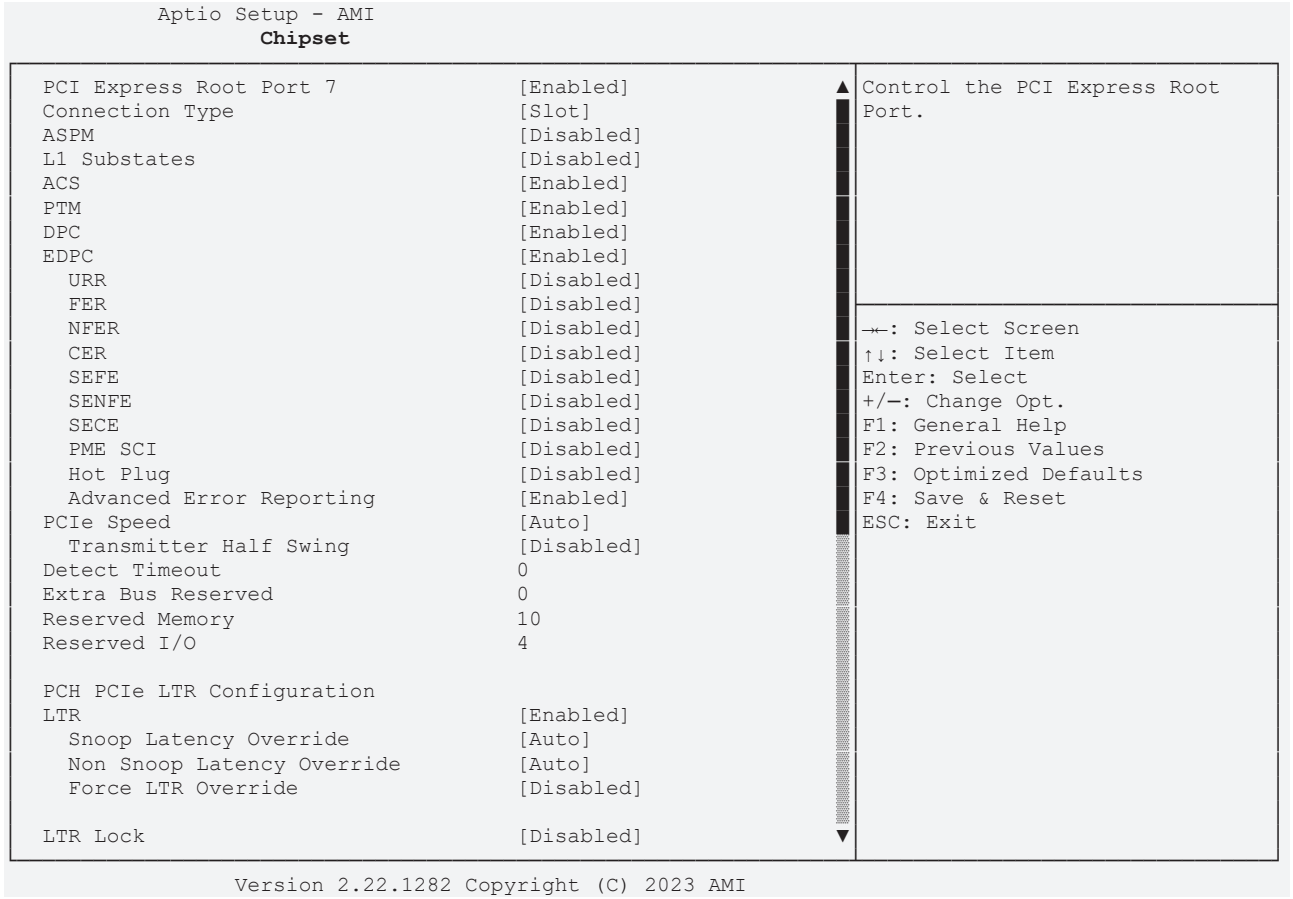
BIOS entry	Options
PCI Express Root Port 4	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

7.4.2.1.5 PCI Express Root Port 6



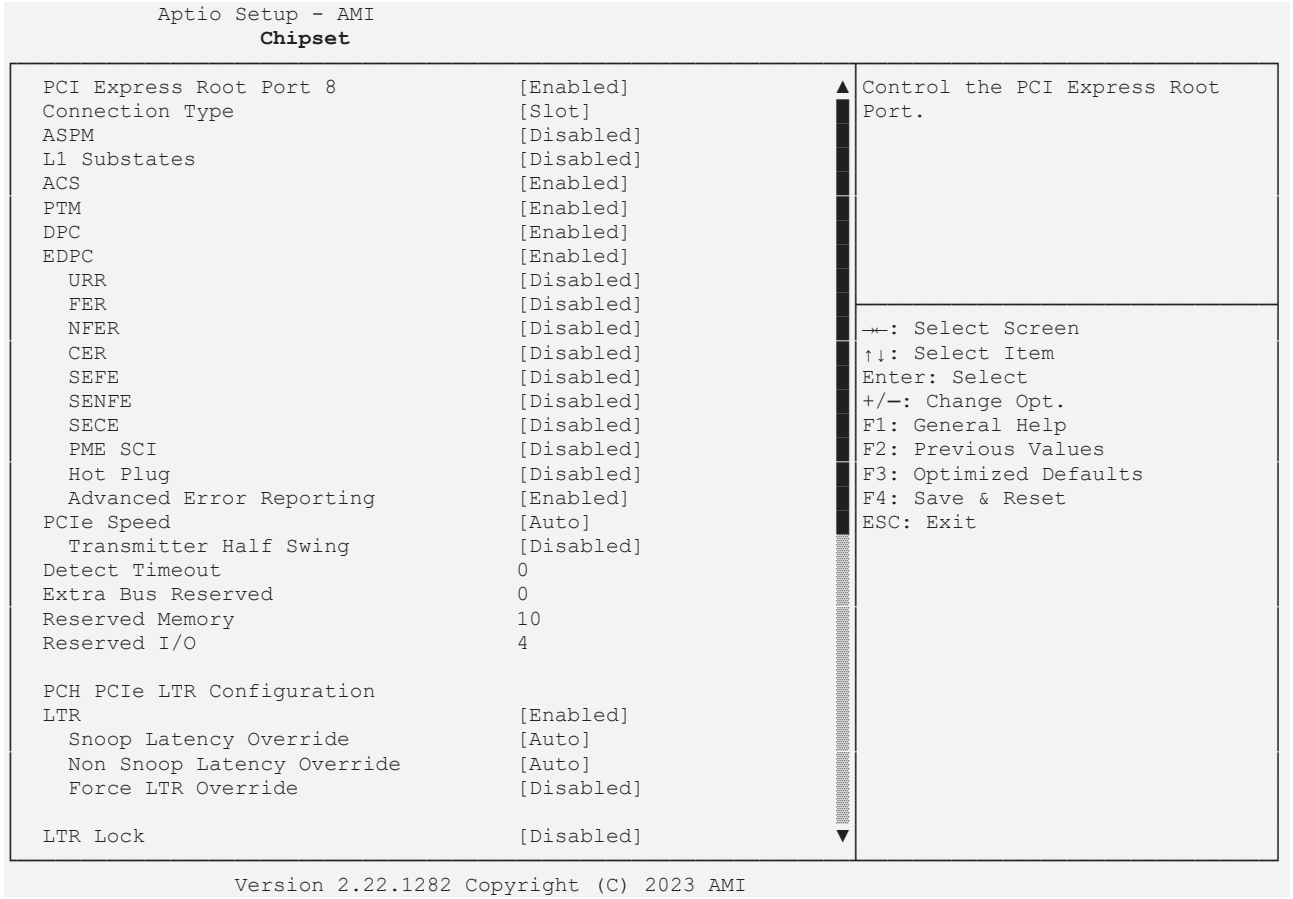
BIOS entry	Options
PCI Express Root Port 6	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

7.4.2.1.6 PCI Express Root Port 7



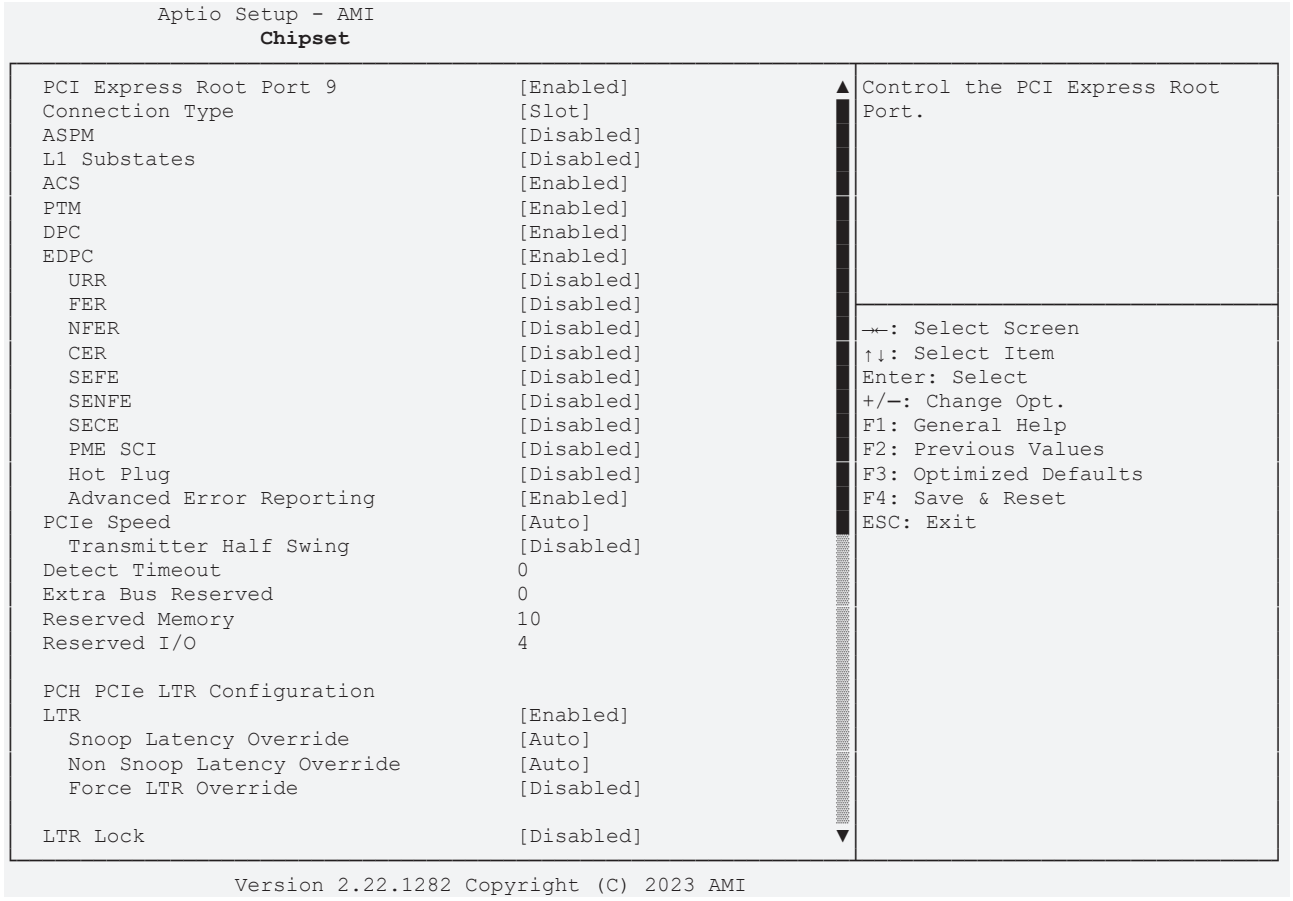
BIOS entry	Options
PCI Express Root Port 7	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

7.4.2.1.7 PCI Express Root Port 8



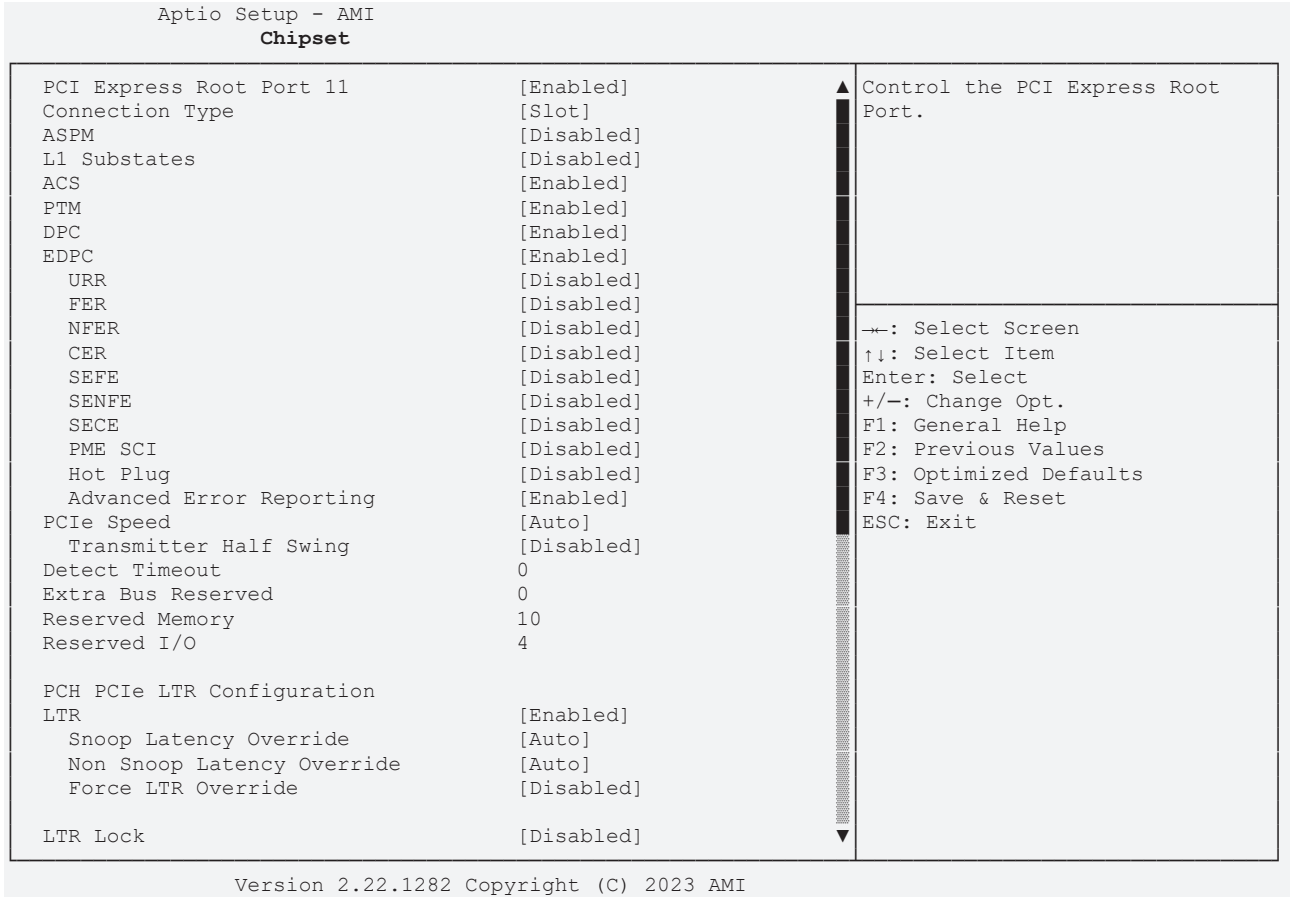
BIOS entry	Options
PCI Express Root Port 8	Enabled / Disabled
Connection Type	Slot / /Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

7.4.2.1.8 PCI Express Root Port 9



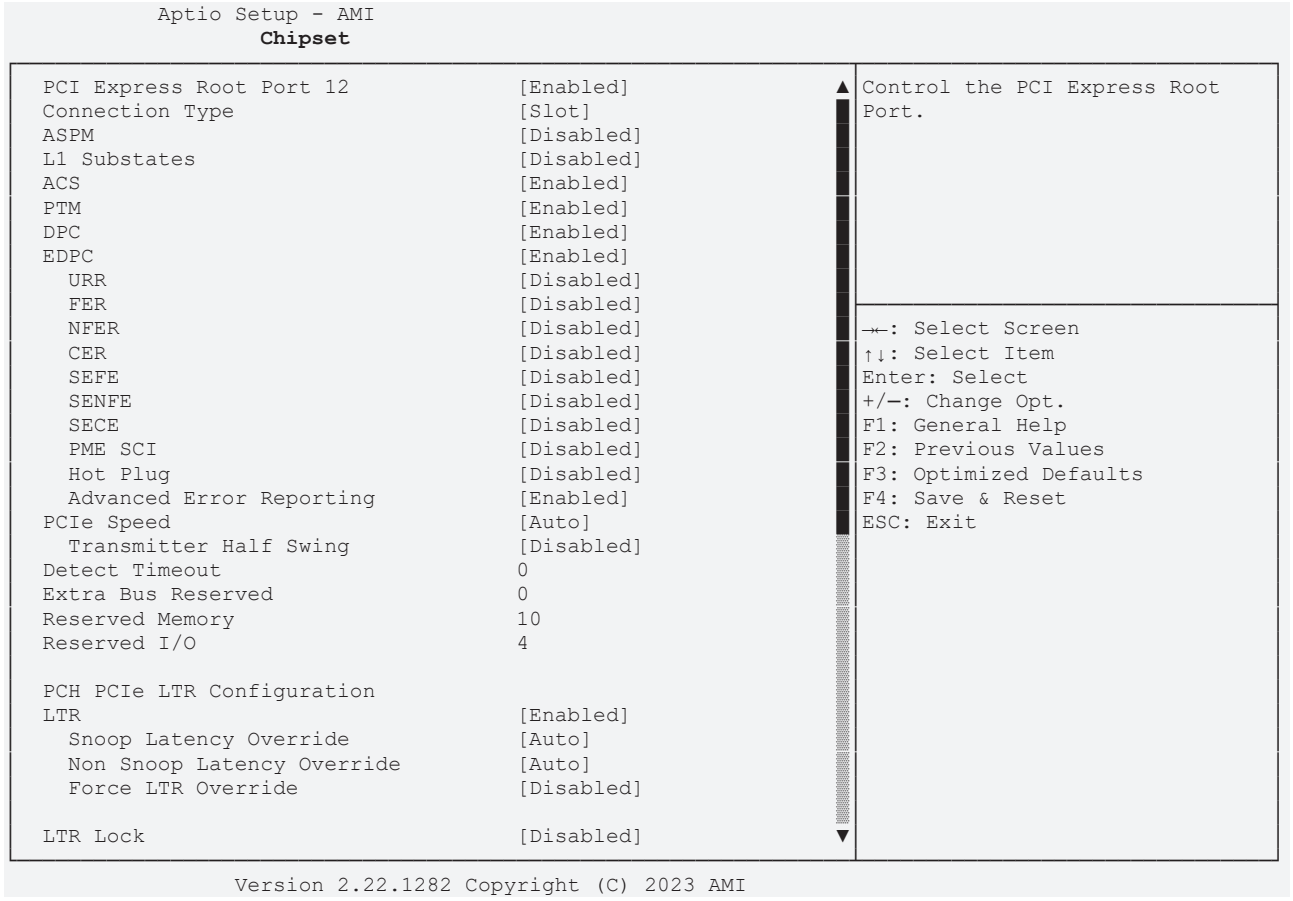
BIOS entry	Options
PCI Express Root Port 9	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

7.4.2.1.9 PCI Express Root Port 11



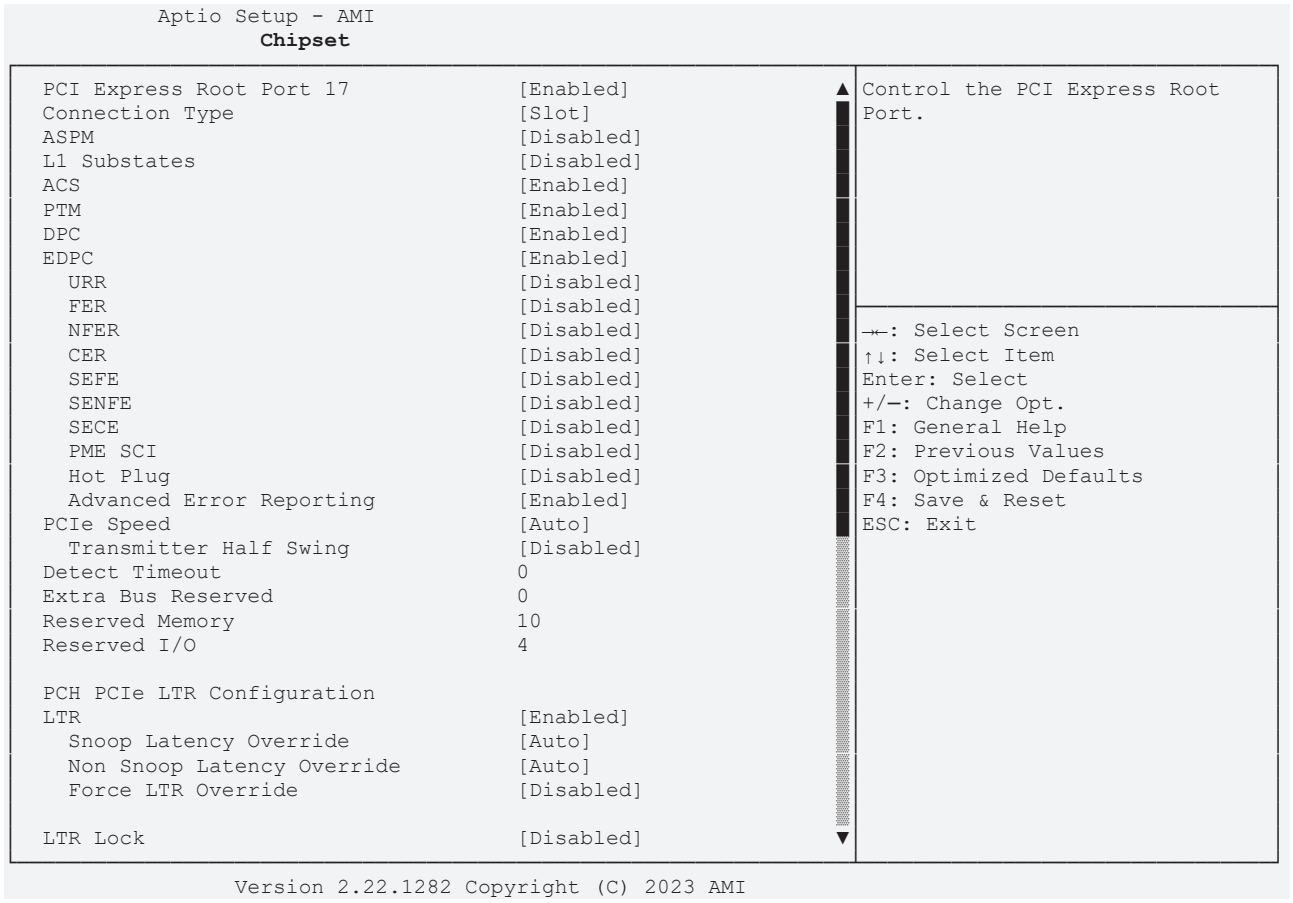
BIOS entry	Options
PCI Express Root Port 11	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

7.4.2.1.10 PCI Express Root Port 12



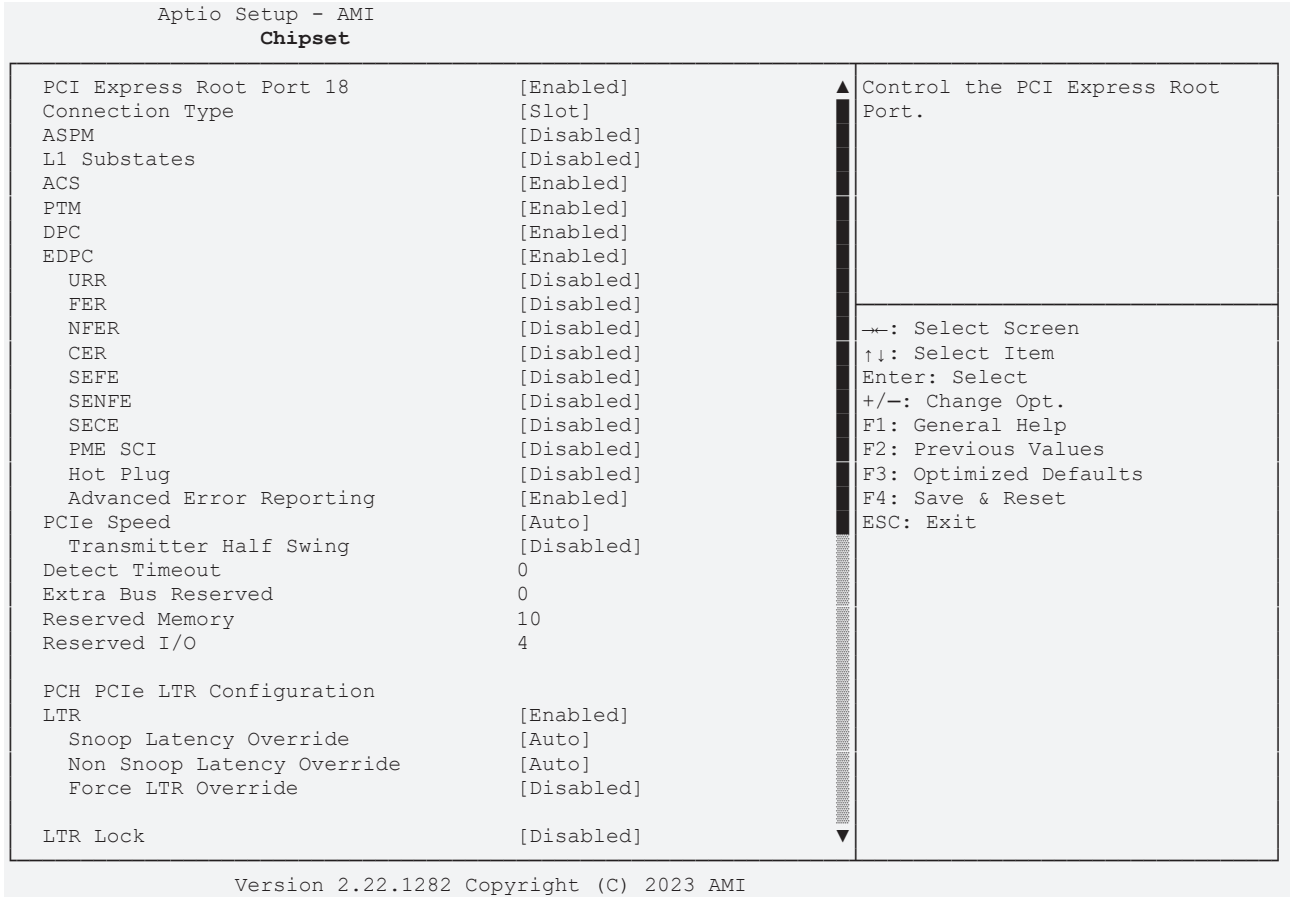
BIOS entry	Options
PCI Express Root Port 12	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

7.4.2.1.11 PCI Express Root Port 17



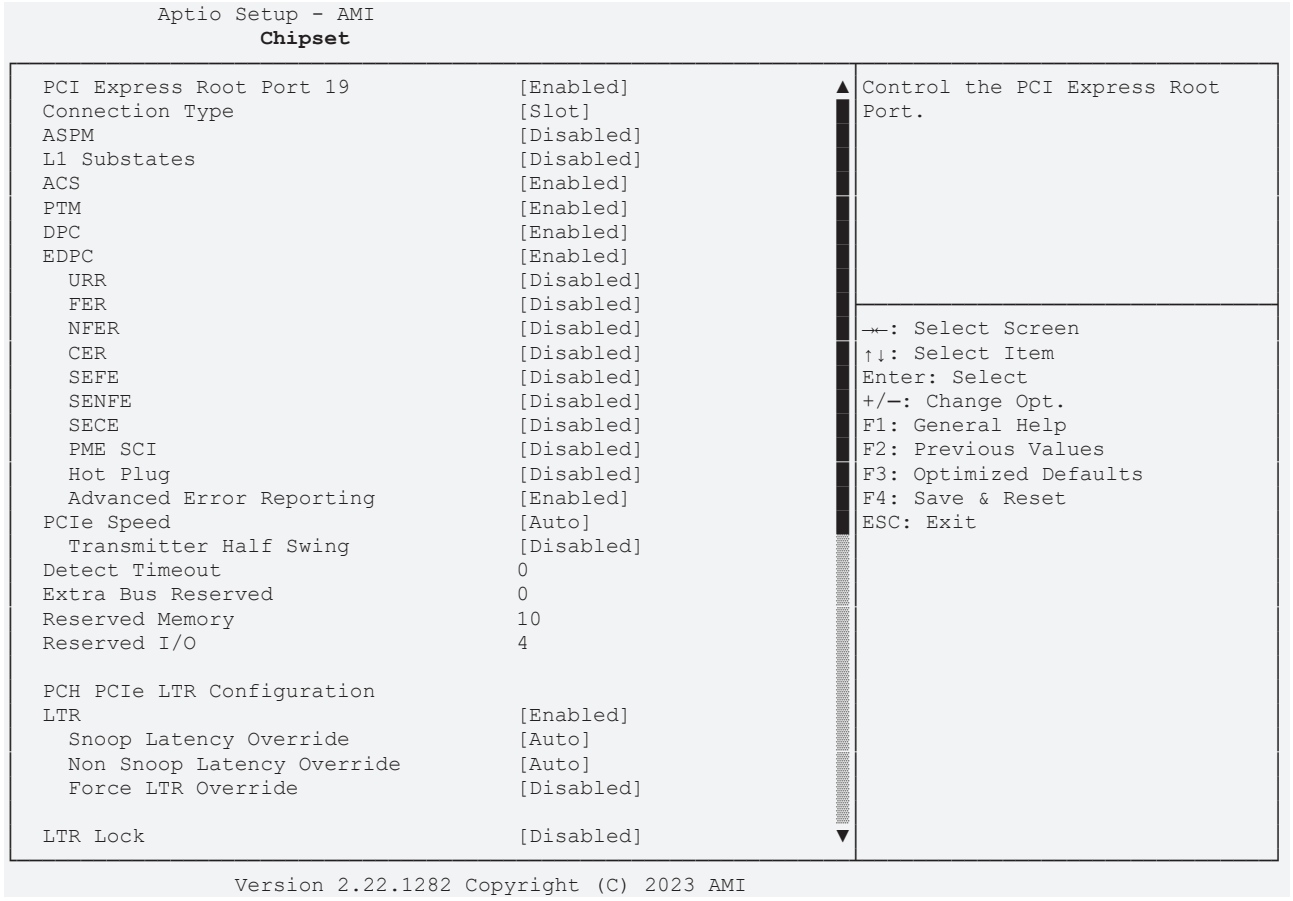
BIOS entry	Options
PCI Express Root Port 17	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

7.4.2.1.12 PCI Express Root Port 18



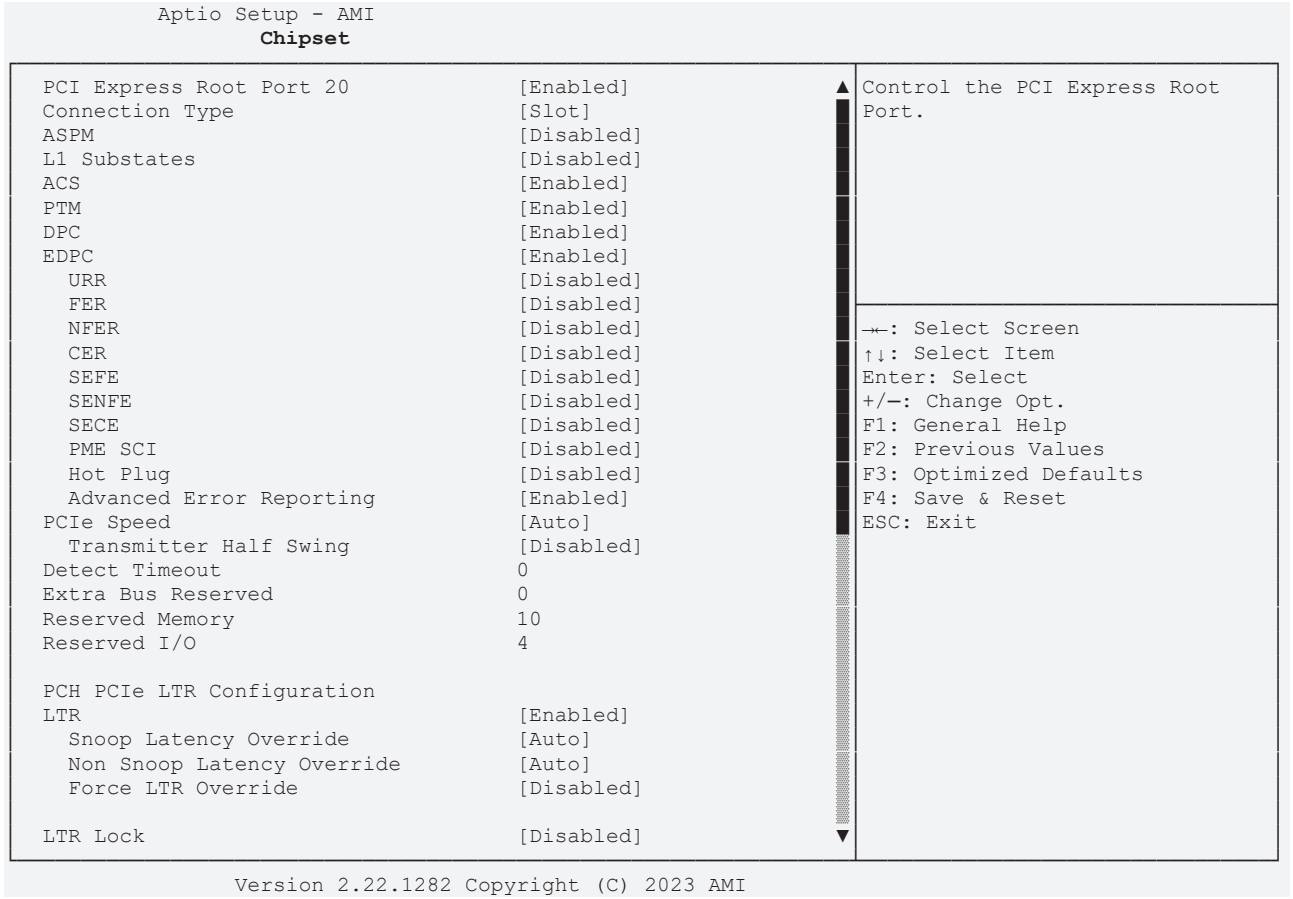
BIOS entry	Options
PCI Express Root Port 18	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

7.4.2.1.13 PCI Express Root Port 19



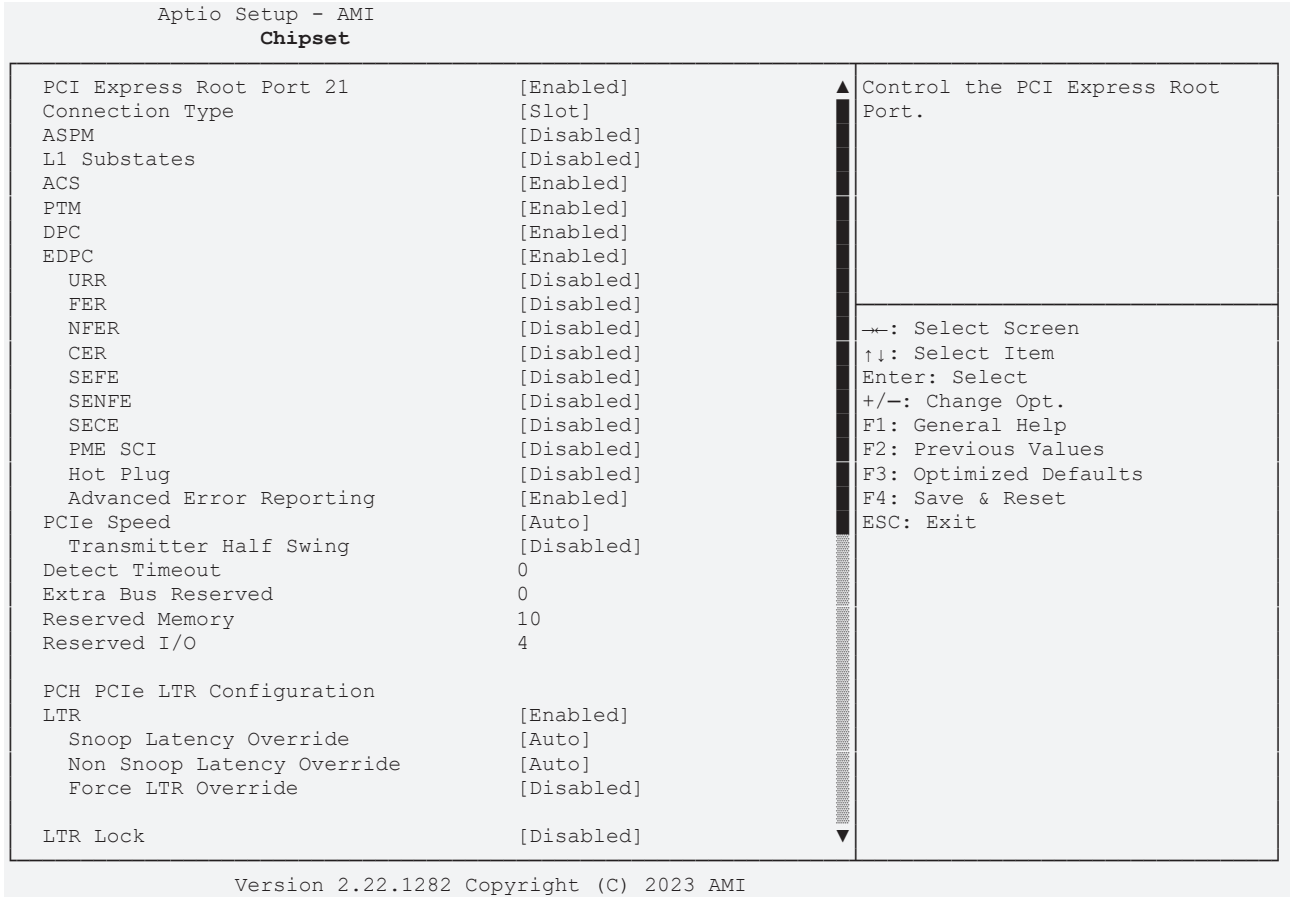
BIOS entry	Options
PCI Express Root Port 19	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

7.4.2.1.14 PCI Express Root Port 20



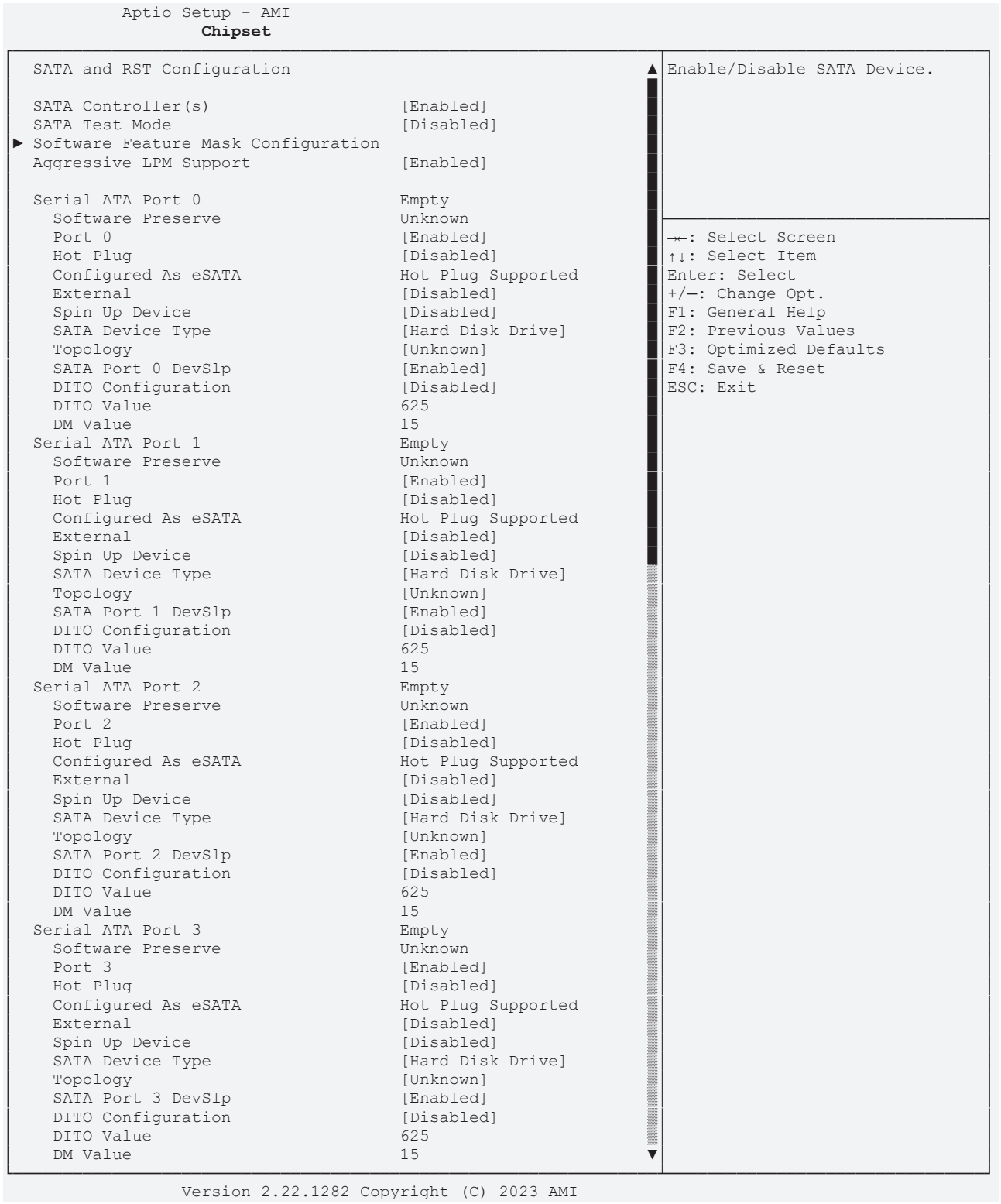
BIOS entry	Options
PCI Express Root Port 20	Enabled / Disabled
Connection Type	Slot / Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

7.4.2.1.15 PCI Express Root Port 21



BIOS entry	Options
PCI Express Root Port 21	Enabled / Disabled
Connection Type	Slot / /Built-in
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Disabled / Enabled
Hot Plug	Enabled / Disabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled

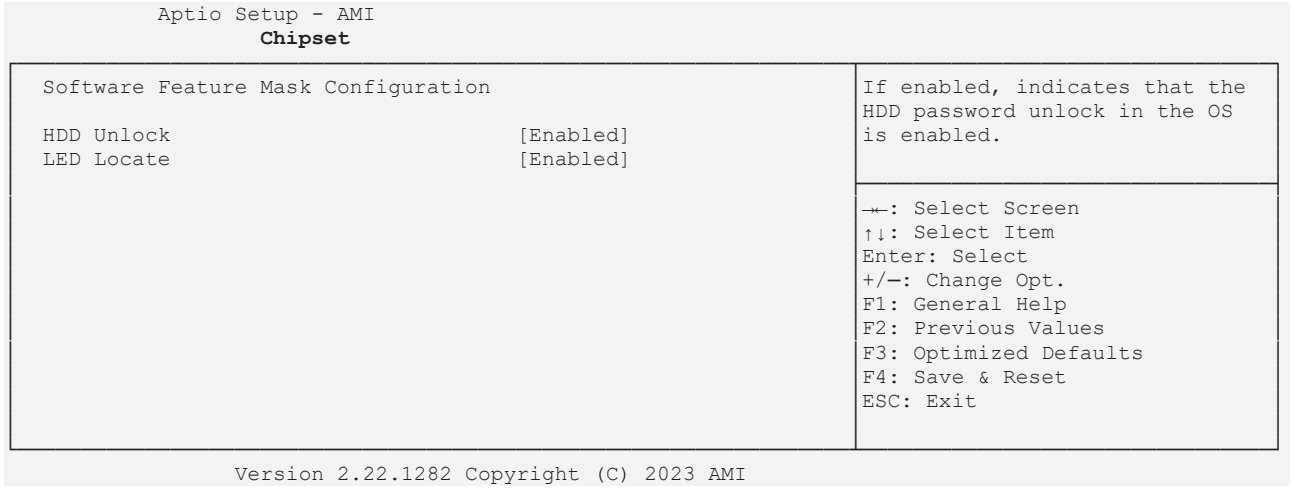
7.4.2.2 SATA And RST Configuration



BIOS entry	Options
SATA and RST Configuration	
SATA Controller(s)	Enabled / Disabled
SATA Mode Selection	None
SATA Test Mode	Disabled / Enabled
►Software Feature Mask Configuration	Submenu see:
Aggressive LPM Support	Enabled / Disabled
Serial ATA Port 0	None
Software Preserve	None
Port 0	Enabled / Disabled
Hot Plug	Disabled / Enabled
Configured As eSATA	None
External	Disabled / Enabled
Spin Up Device	Disabled / Enabled
SATA Device Type	Hard Disk Drive / Solid State Drive
Topology	Unknown / ISATA / Direct Connect / Flex / M2
SATA Port 0 DevSlp	Enabled / Disabled
DITO Configuration	Disabled / Enabled
DITO Value	None
DM Value	None
Serial ATA Port 1	None
Software Preserve	None
Port 1	Enabled / Disabled
Hot Plug	Disabled / Enabled
Configured As eSATA	None
External	Disabled / Enabled
Spin Up Device	Disabled / Enabled
SATA Device Type	Hard Disk Drive / Solid State Drive
Topology	Unknown / ISATA / Direct Connect / Flex / M2
SATA Port 1 DevSlp	Enabled / Disabled
DITO Configuration	Disabled / Enabled
DITO Value	None
DM Value	None
Serial ATA Port 2	None
Software Preserve	None
Port 2	Enabled / Disabled
Hot Plug	Disabled / Enabled
Configured As eSATA	None
External	Disabled / Enabled
Spin Up Device	Disabled / Enabled
SATA Device Type	Hard Disk Drive / Solid State Drive
Topology	Unknown / ISATA / Direct Connect / Flex / M2
SATA Port 2 DevSlp	Enabled / Disabled
DITO Configuration	Disabled / Enabled
DITO Value	None
DM Value	None
Serial ATA Port 3	None

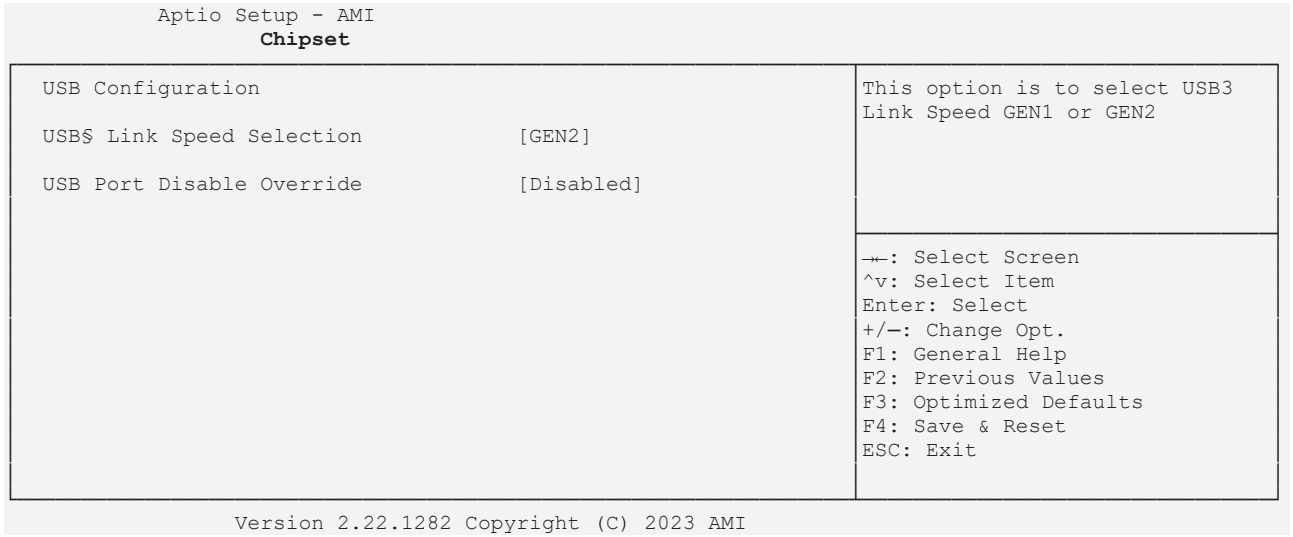
BIOS entry	Options
Software Preserve	None
Port 3	Enabled / Disabled
Hot Plug	Disabled / Enabled
Configured As eSATA	None
External	Disabled / Enabled
Spin Up Device	Disabled / Enabled
SATA Device Type	Hard Disk Drive / Solid State Drive
Topology	Unknown / ISATA / Direct Connect / Flex / M2
SATA Port 3 DevSlp	Enabled / Disabled
DITO Configuration	Disabled / Enabled
DITO Value	None
DM Value	None

7.4.2.2.1 Software Feature Mask Configuration



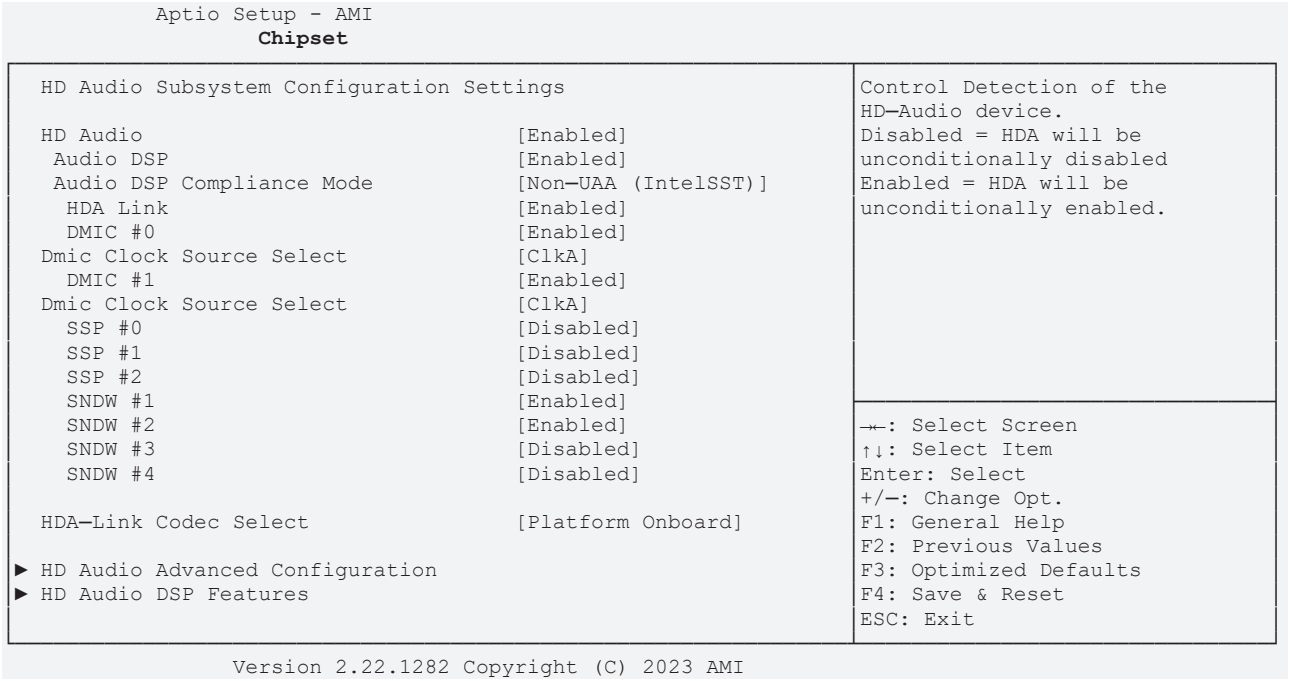
BIOS entry	Options
Software Feature Mask Configuration	
HDD Unlock	Enabled / Disabled
LED Locate	Enabled / Disabled

7.4.2.3 USB Configuration



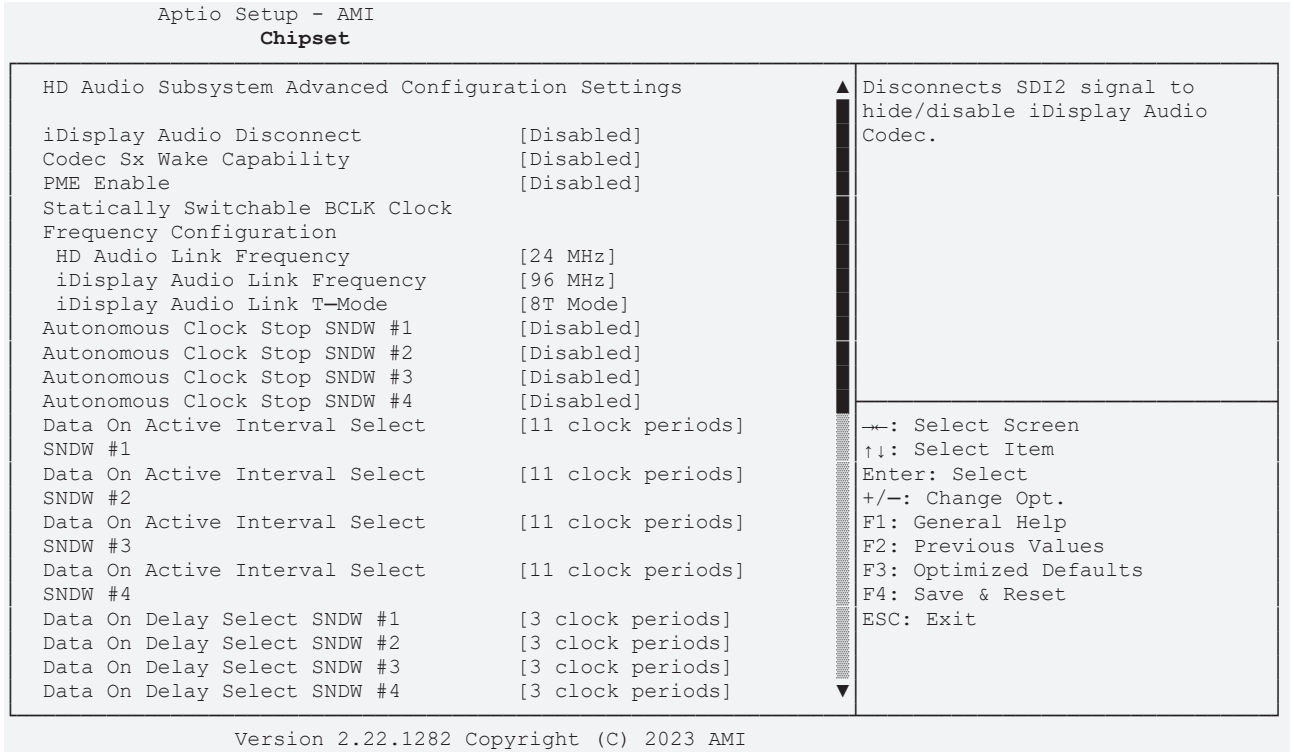
BIOS entry	Options
USB Configuration	
USB3 Link Speed Selection	Gen2 / Gen1
USB Port Disable Override	Disabled / Select Per-Pin

7.4.2.4 HD Audio Configuration



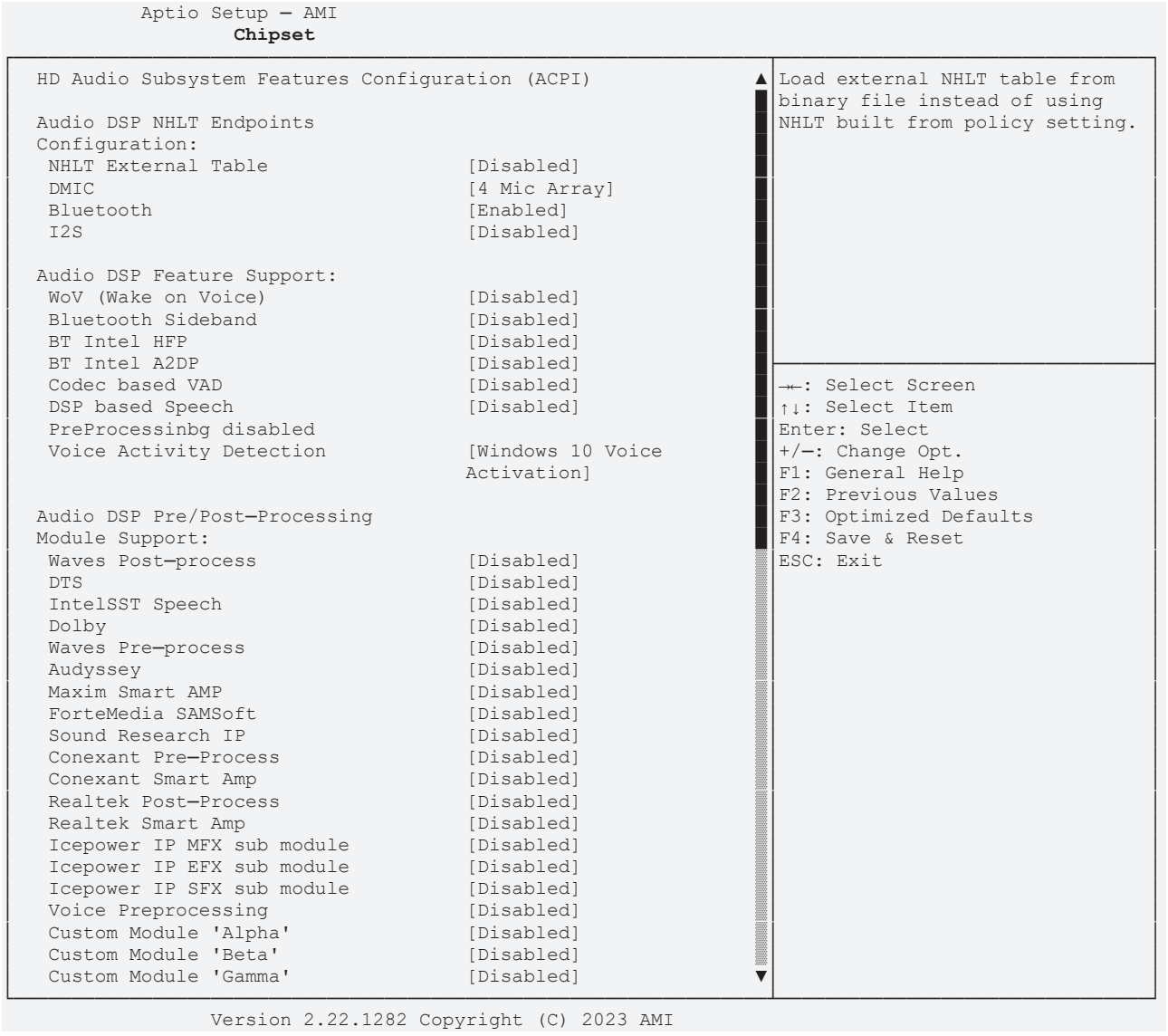
BIOS entry	Options
HD Audio Subsystem Configuration Settings	
HD Audio	Enabled / Disabled
Audio DSP	Enabled / Disabled
Audio DSP Compliance Mode	Non-UAA (IntelSST) / UAA (HDA Inbox/IntelSST)
HDA Link	Enabled / Disabled
DMIC #0	Enabled / Disabled
Dmic Clock Source Select	None
DMIC #1	Enabled / Disabled
Dmic Clock Source Select	None
SSP #0	Disabled / Enabled
SSP #1	Disabled / Enabled
SSP #2	Disabled / Enabled
SNDW #1	Enabled / Disabled
SNDW #2	Enabled / Disabled
SNDW #3	Disabled / Enabled
SNDW #4	Disabled / Enabled
HDA-Link Codec Select	Platform Onboard / External Kit
►HD Audio Advanced Configuration	Submenu see: HD Audio Advanced Configuration [▶ 109]
►HD Audio DSP Features Configuration	Submenu see: HD Audio DSP Features Configuration [▶ 110]

7.4.2.4.1 HD Audio Advanced Configuration



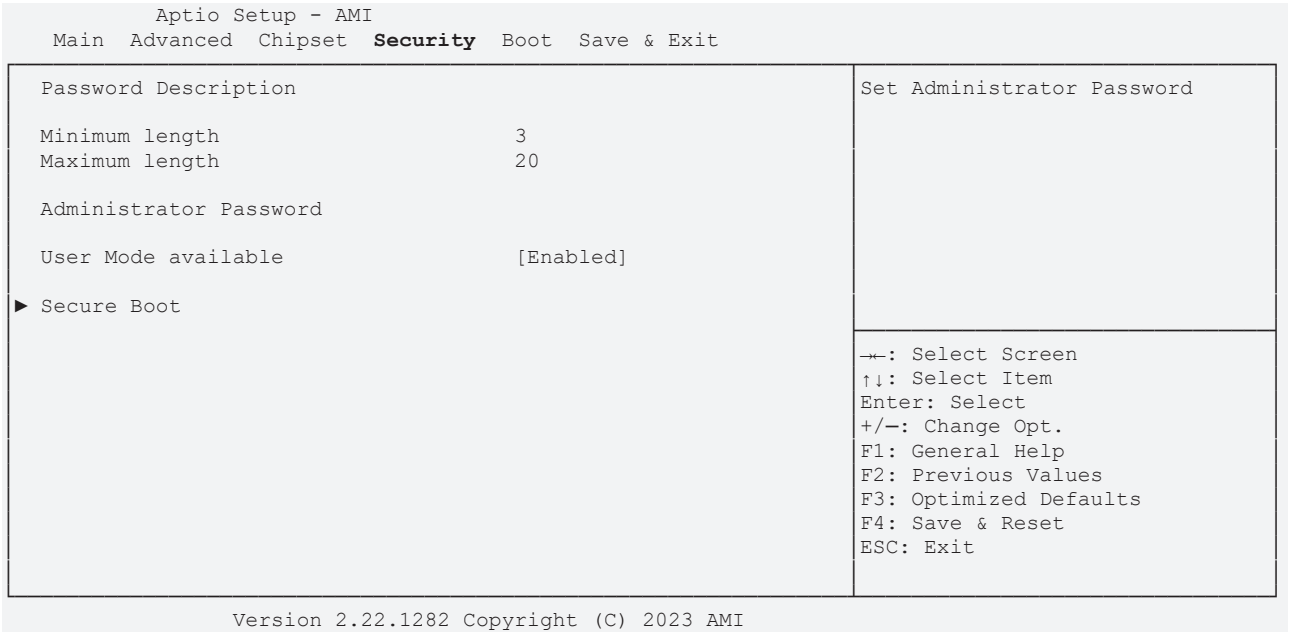
BIOS entry	Options
HD Audio Subsystem Advanced Configuration Settings	
iDisplay Audio Disconnect	Disabled / Enabled
Codec Sx Wake Capability	Disabled / Enabled
PME Enable	Disabled / Enabled
Statically Switchable BCLK Clock DPC Frequency Configuration:	
HD Audio Link Frequency	6 MHz / 12 MHz / 24 MHz
iDisplay Audio Link Frequency	48 MHz / 96 MHz
iDisplay Audio Link T-Mode FER	2T Mode / 4T Mode / 8T Mode / 16T Mode
Autonomous Clock Stop SNDW #1	Disabled / Enabled
Autonomous Clock Stop SNDW #2	Disabled / Enabled
Autonomous Clock Stop SNDW #3	Disabled / Enabled
Autonomous Clock Stop SNDW #4	Disabled / Enabled
Data On Active Interval Select SNDW #1	6 / 7 / 8 / 11 clock periods
Data On Active Interval Select SNDW #2	6 / 7 / 8 / 11 clock periods
Data On Active Interval Select SNDW #3	6 / 7 / 8 / 11 clock periods
Data On Active Interval Select SNDW #4	6 / 7 / 8 / 11 clock periods
Data On Delay Select SNDW #1	2 / 3 clock periods
Data On Delay Select SNDW #2	2 / 3 clock periods
Data On Delay Select SNDW #3	2 / 3 clock periods
Data On Delay Select SNDW #4	2 / 3 clock periods

7.4.2.4.2 HD Audio DSP Features Configuration



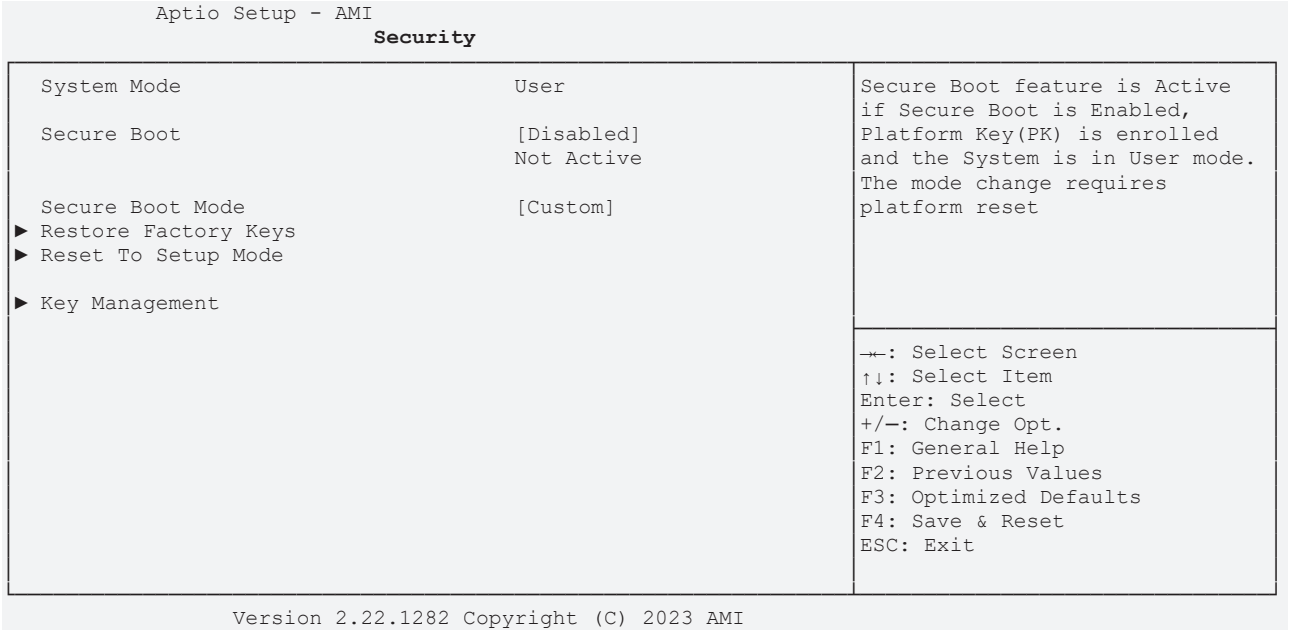
BIOS entry	Options
HD Audio Subsystem Features Configuration (ACPI)	
Audio DSP NHLT Endpoints Configuration:	
NHLT External Table	Disabled / Enabled
DMIC	Disabled / 1 / 2 / 4 Mic Array
Bluetooth	None
I2S	None
Audio DSP Feature Support:	
WoV (Wake on Voice)	Disabled / Enabled
Bluetooth Sideband	Disabled / Enabled
BT Intel HFP	None
BT Intel A2DP	None
Codec based VAD	Disabled / Enabled
DSP based Speech	None
Pre-Processing disabled	
Voice Activity Detection	Intel Wake on Voice / Windows 10 Voice Activation
Audio DSP Pre/Post-Processing Module Support:	
Waves Post-process	Disabled / Enabled
DTS	Disabled / Enabled
IntelSST Speech	Disabled / Enabled
Dolby	Disabled / Enabled
Waves Pre-process	Disabled / Enabled
Audyssey	Disabled / Enabled
Maxim Smart AMP	Disabled / Enabled
ForteMedia SAMSoft	Disabled / Enabled
Sound Research IP	Disabled / Enabled
Conexant Pre-Process	Disabled / Enabled
Conexant Smart Amp	Disabled / Enabled
Realtek Post-Process	Disabled / Enabled
Realtek Smart Amp	Disabled / Enabled
Icepower IP MFX sub module	Disabled / Enabled
Icepower IP EFX sub module	Disabled / Enabled
Icepower IP SFX sub module	Disabled / Enabled
Voice Preprocessing	Disabled / Enabled
Custom Module 'Alpha'	Disabled / Enabled
Custom Module 'Beta'	Disabled / Enabled
Custom Module 'Gamma'	Disabled / Enabled

7.5 Security CB3072



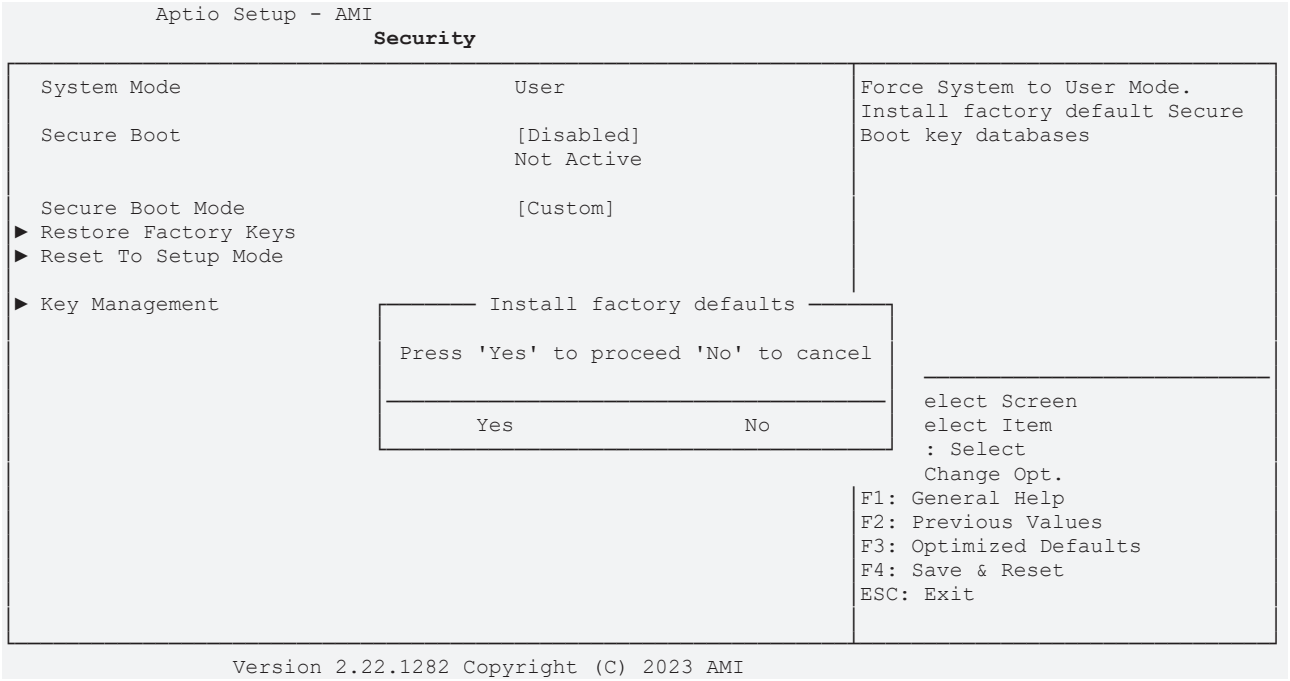
BIOS entry	Options
Password Description	
Minimum length	None
Maximum length	None
Administrator Password	Here you can set an administrator password.
User Mode available	Enabled / Disabled
▶Secure Boot	Submenu see: Secure Boot [▶ 113]

7.5.1 Secure Boot



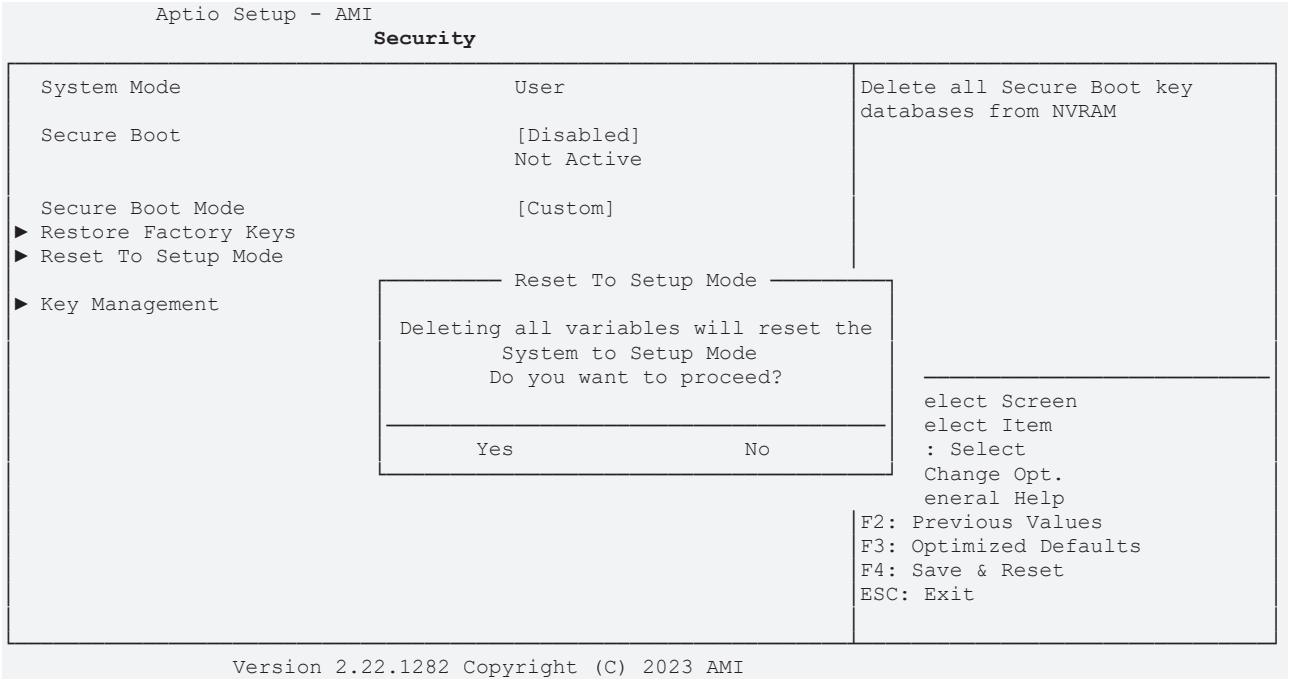
BIOS entry	Options
System Mode	None
Secure Boot	Disabled / Enabled Not Active
Secure Boot Mode	Custom / Standard
►Restore Factory Keys	Submenu see: Restore Factory Keys [▶ 114]
►Reset To Setup Mode	Submenu see: Reset To Setup Mode [▶ 115]
►Key Management	Submenu see: Key Management [▶ 116]

7.5.1.1 Restore Factory Keys



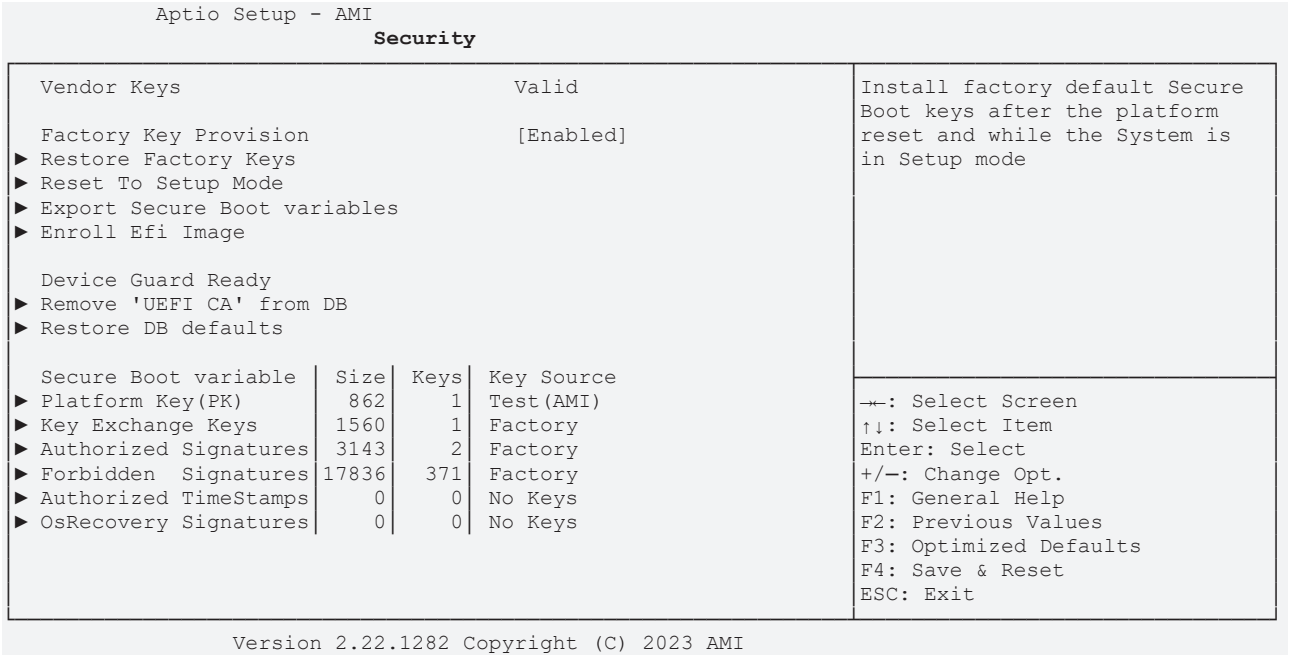
BIOS entry	Options
System Mode	None
Secure Boot	Disabled / Enabled
Secure Boot Mode	Custom / Standard
Restore Factory Keys	Install factory defaults, see box

7.5.1.2 Reset To Setup Mode



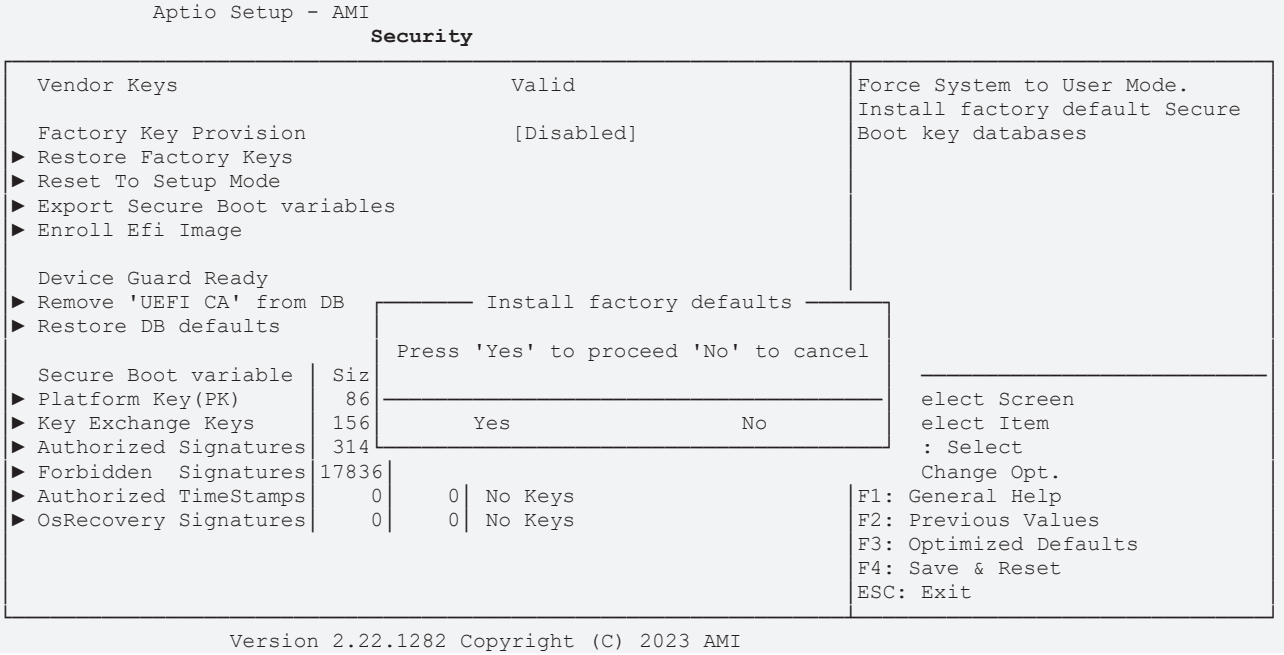
BIOS entry	Options
System Mode	none
Secure Boot	Disabled / Enabled Not Active
Secure Boot Mode	Custom / Standard
Reset To Setup Mode	Reset To Setup Mode (see box)

7.5.1.3 Key Management



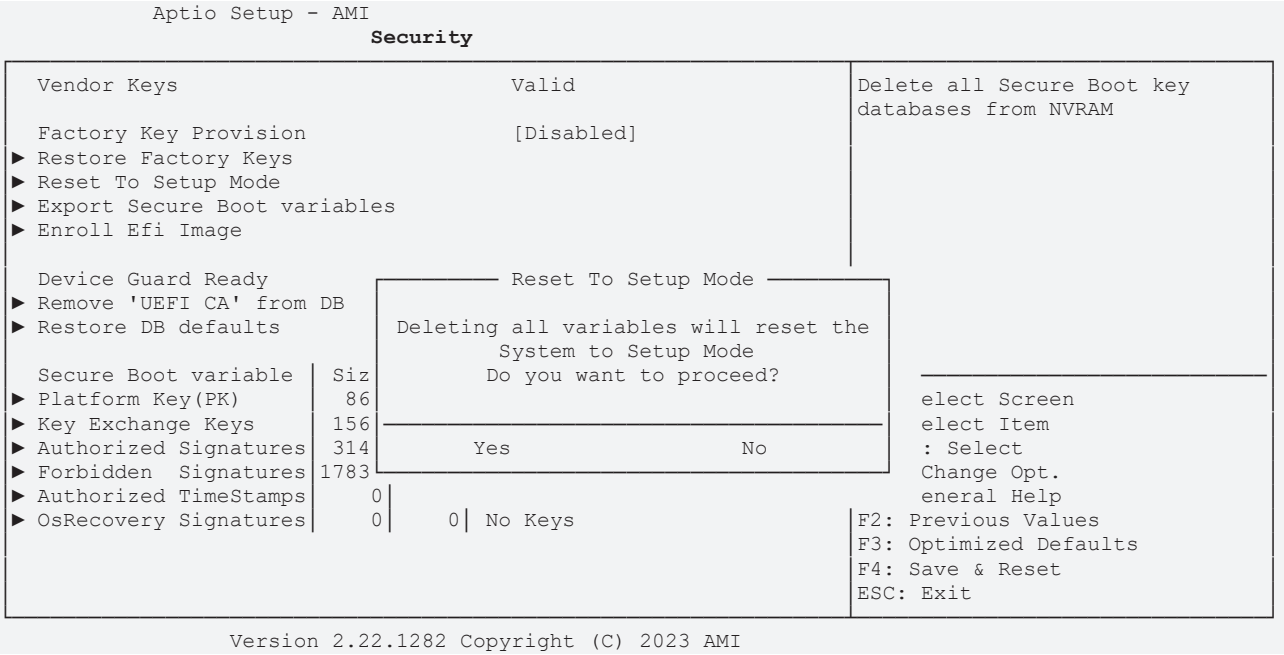
BIOS entry	Options
Vendor Keys	None
Factory Key Provision	Disabled / Enabled
►Restore Factory Keys	Submenu see: Restore Factory Keys [▶ 117]
►Reset To Setup Mode	Submenu see: Reset To Setup Mode [▶ 117]
►Export Secure Boot variables	Submenu see: Export Secure Boot variables [▶ 118]
►Enroll Efi Image	Submenu see: Enroll Efi Image [▶ 118]
Device Guard Ready	
►Remove 'UEFI CA' from DB	Submenu see: Remove 'UEFI CA' from DB [▶ 119]
►Restore DB defaults	Submenu see: Restore DB defaults [▶ 119]
Secure Boot variables	
PlatformKey(PK)	Press enter key
Key Exchange Keys	Press enter key
Authorized Signatures	Press enter key
Forbidden Signatures	Press enter key
Authorized TimeStamps	Press enter key
OsRecovery Signatures	Press enter key

7.5.1.3.1 Restore Factory Keys



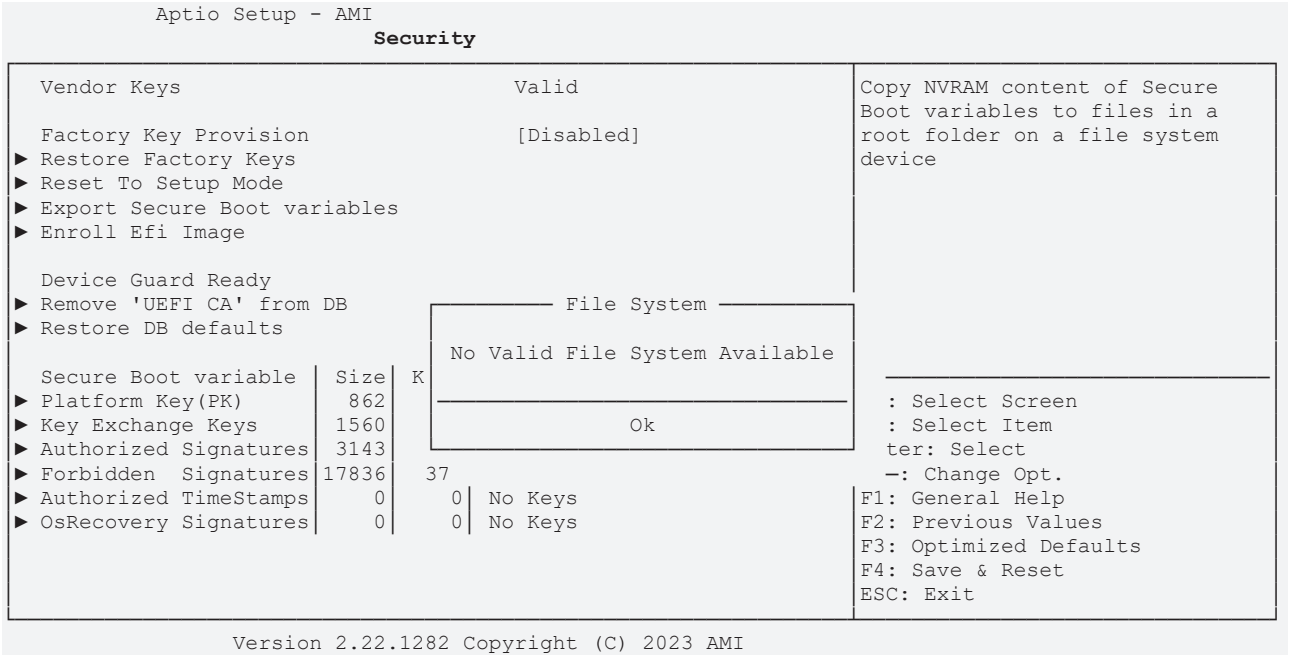
BIOS entry	Options
Vendor Keys	None
Restore Factory Keys	See box

7.5.1.3.2 Reset To Setup Mode



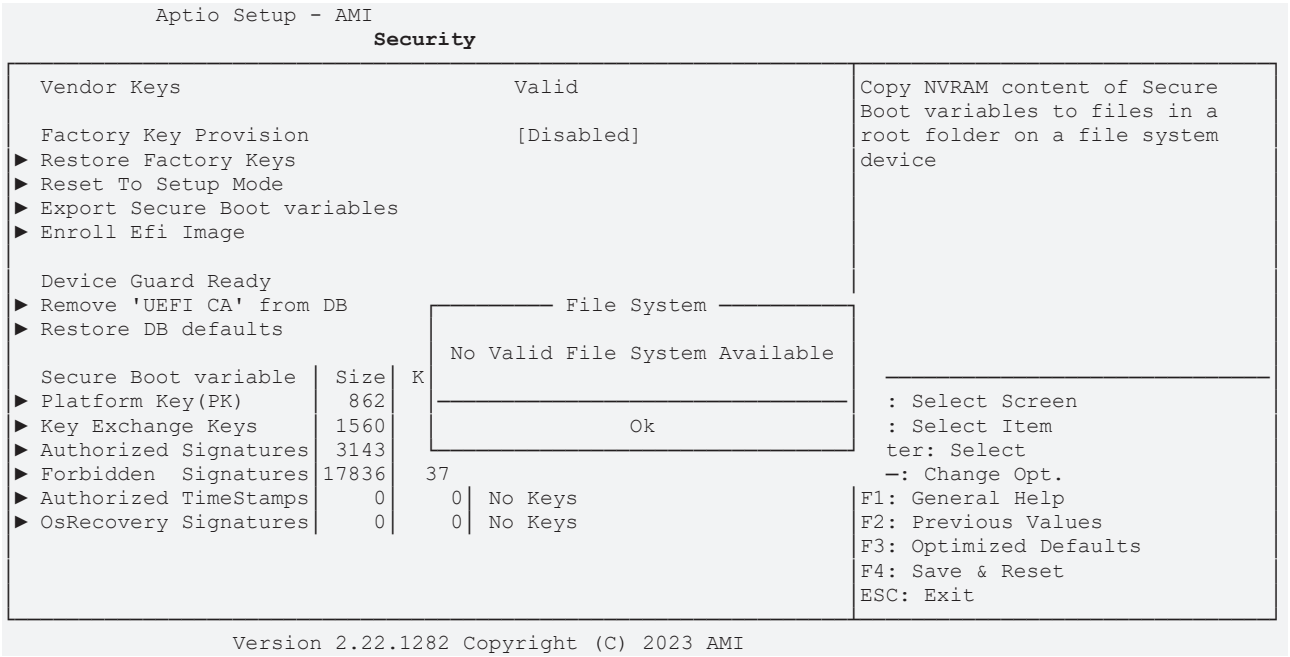
BIOS entry	Options
Vendor Keys	None
Reset To Setup Mode	See box

7.5.1.3.3 Export Secure Boot variables



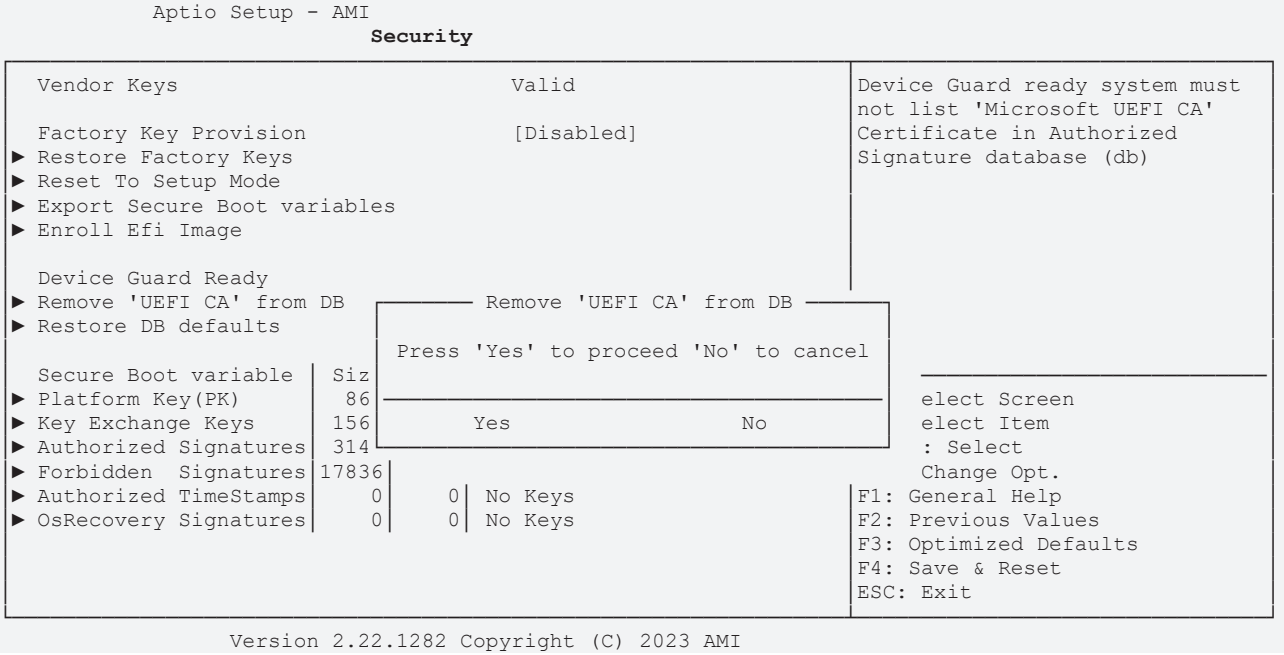
BIOS entry	Options
Vendor Keys	None
Export Secure Boot variables	See box

7.5.1.3.4 Enroll Efi Image



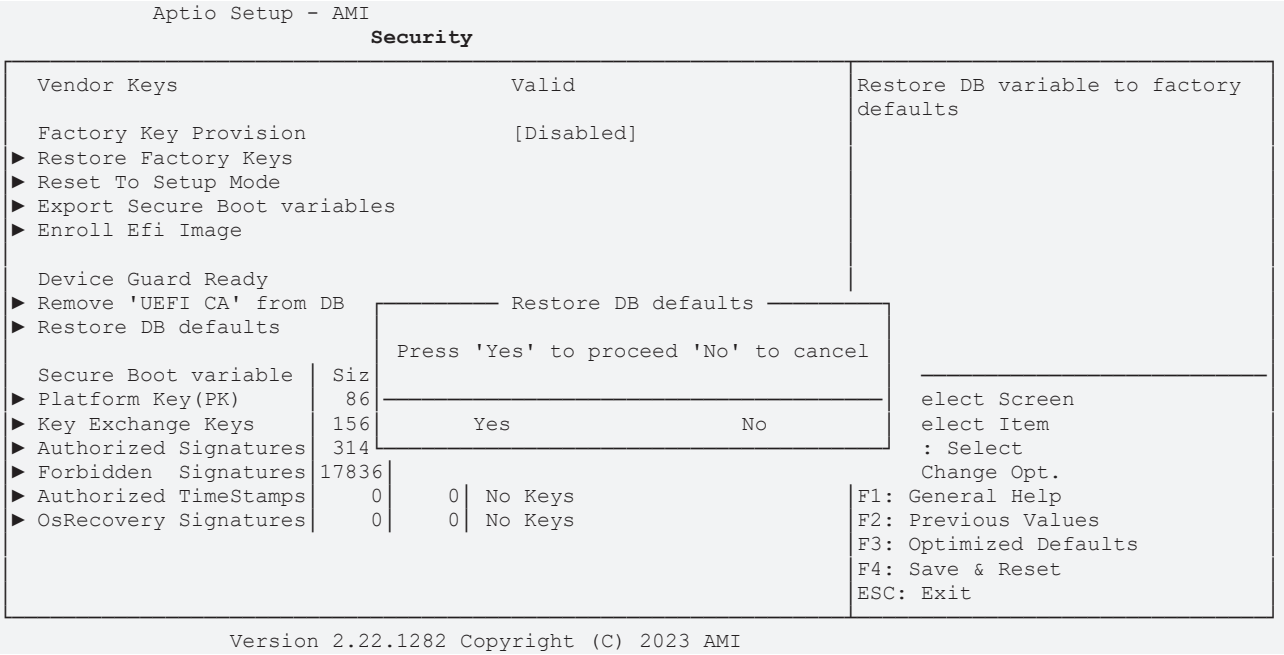
BIOS entry	Options
Vendor Keys	None
Enroll Efi Image	See box

7.5.1.3.5 Remove UEFI CA from DB



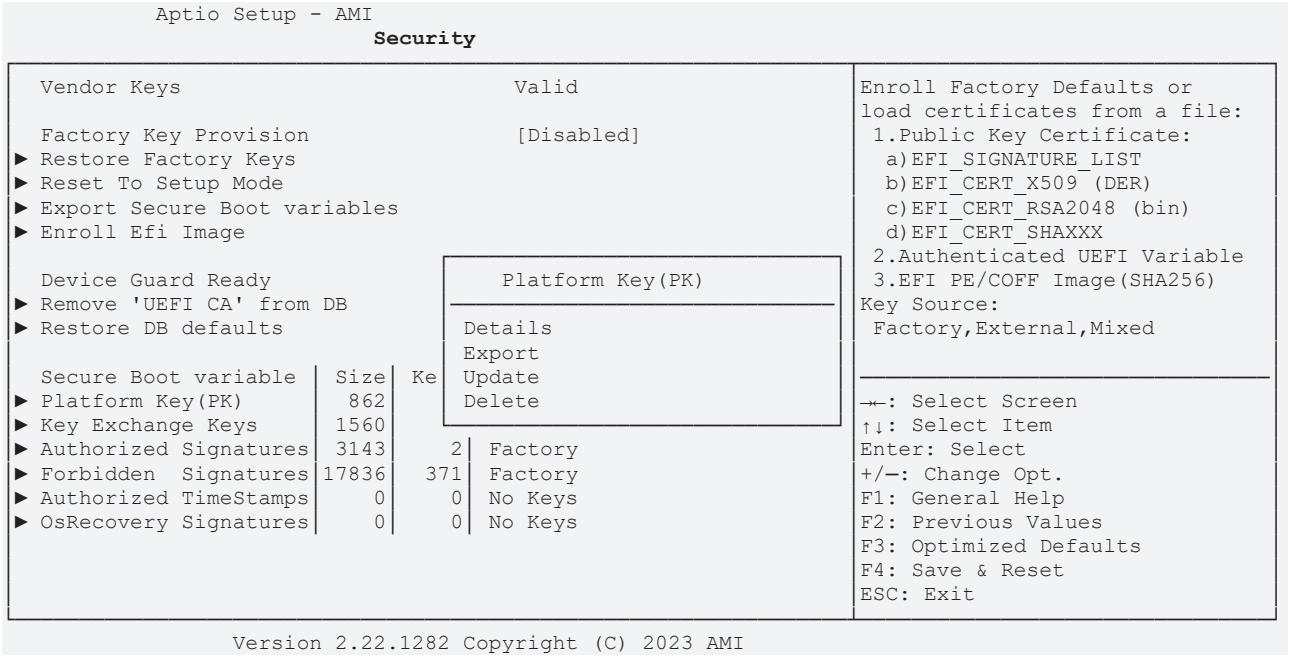
BIOS entry	Options
Vendor Keys	None
Remove ‘UEFI CA‘ from DB	See box

7.5.1.3.6 Restore DB defaults



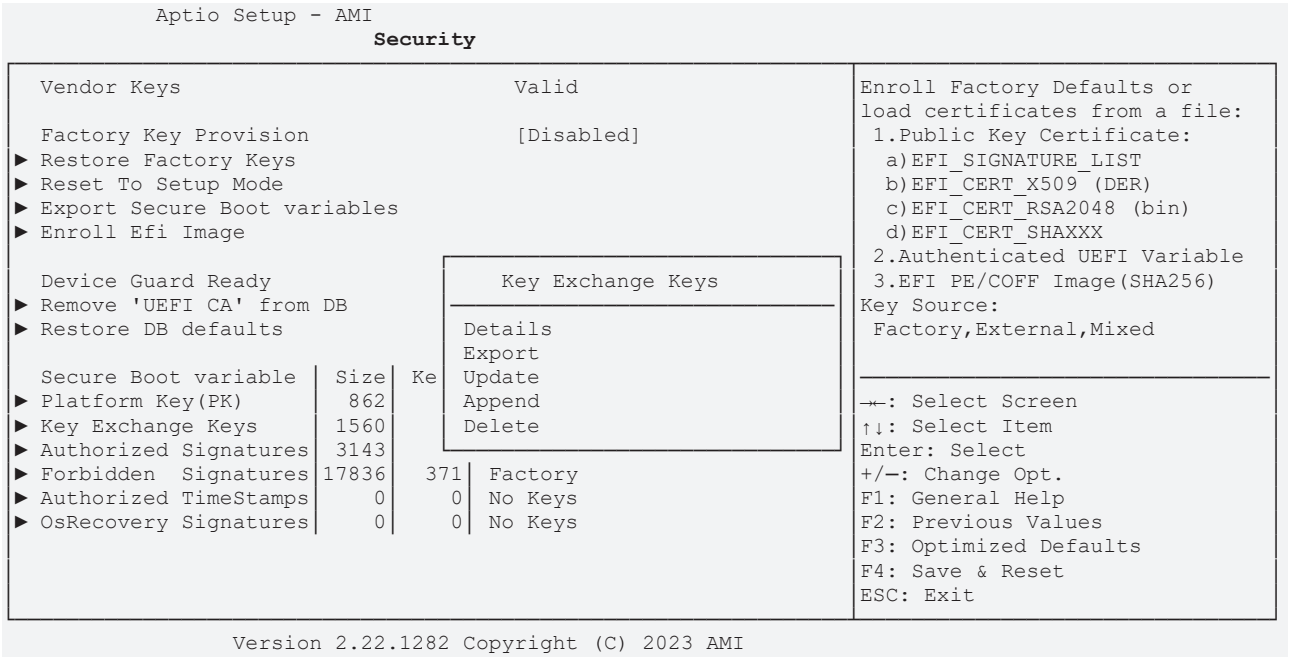
BIOS entry	Options
Vendor Keys	None
Restore DB Faults	See box

7.5.1.3.7 Platform Key (PK)



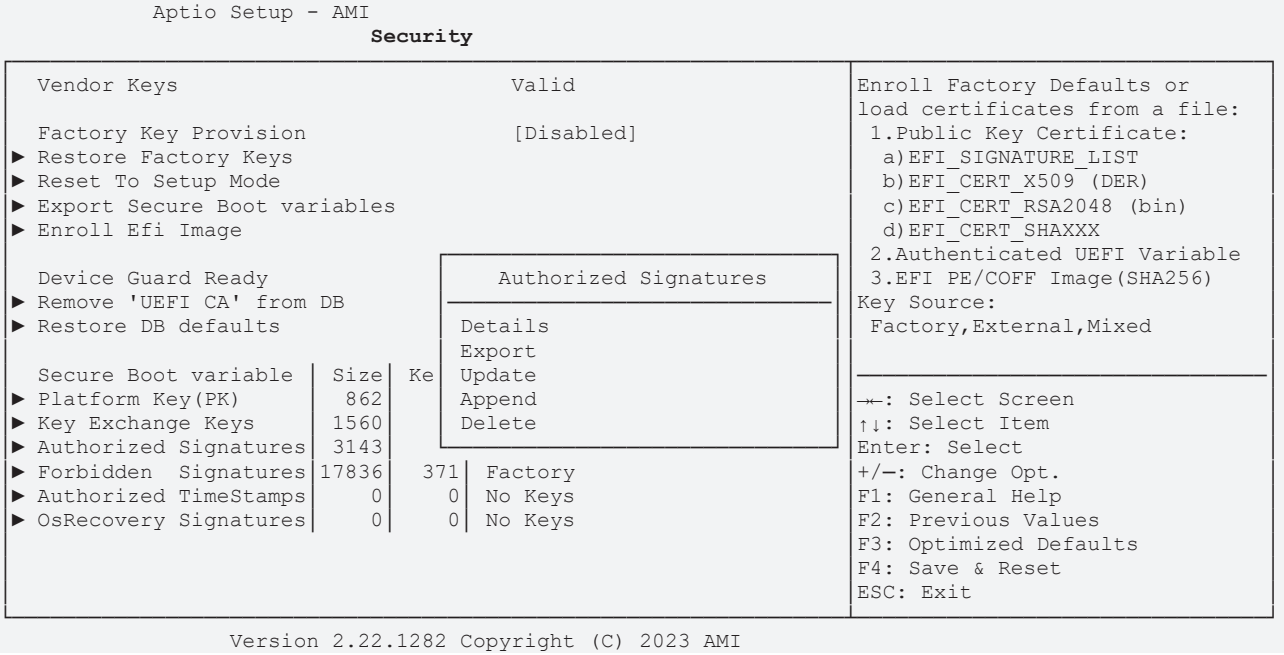
BIOS entry	Options
Vendor Keys	None
Platform Key (PK)	See box

7.5.1.3.8 Key Exchange Keys



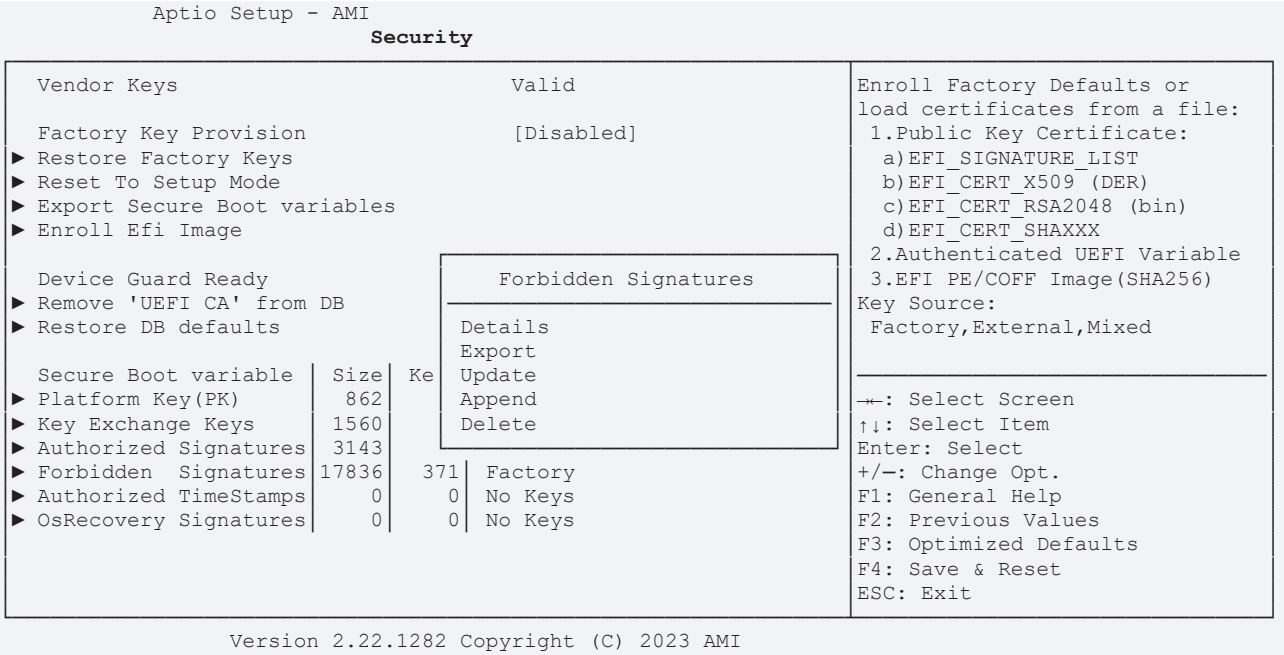
BIOS entry	Options
Vendor Keys	None
Key Exchange Keys	See box

7.5.1.3.9 Authorized Signatures



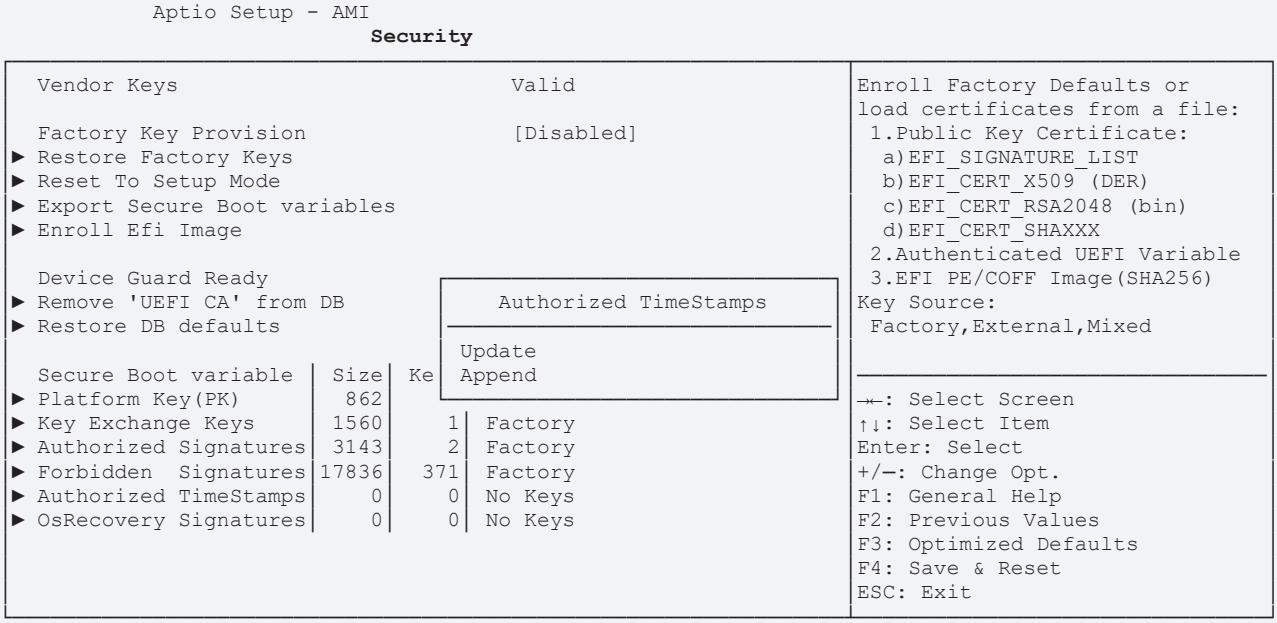
BIOS entry	Options
Vendor Keys	None
Authorized Signatures	See box

7.5.1.3.10 Forbidden Signatures



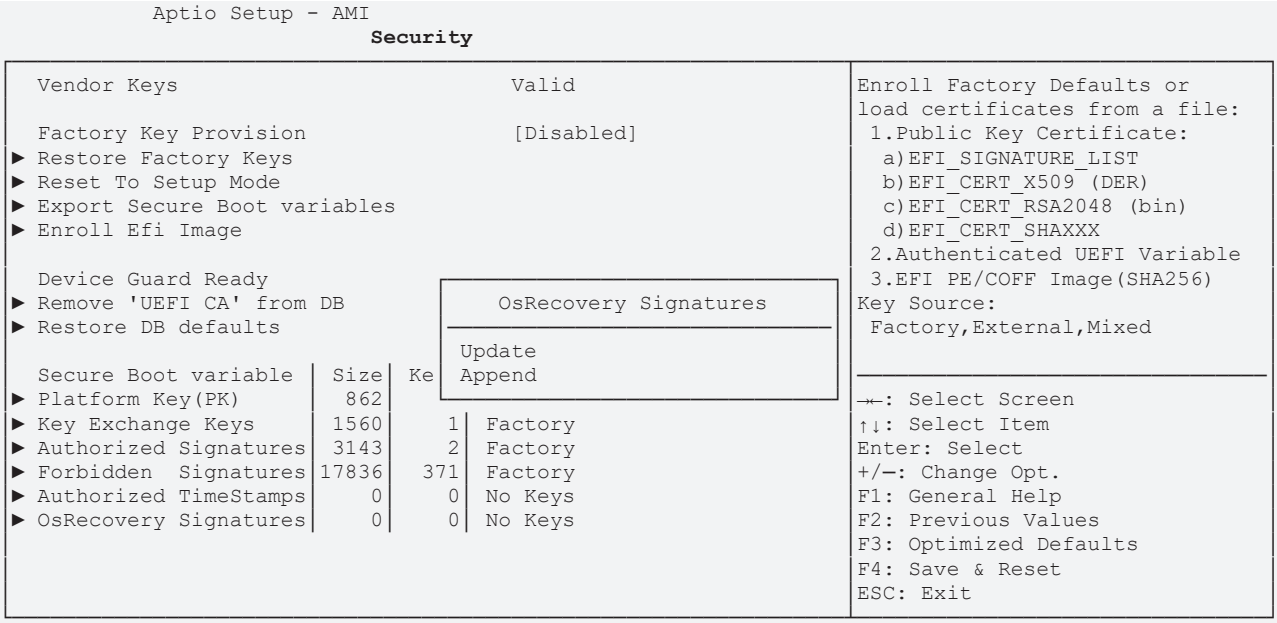
BIOS entry	Options
Vendor Keys	None
Forbidden Signatures	See box

7.5.1.3.11 Authorized TimeStamps



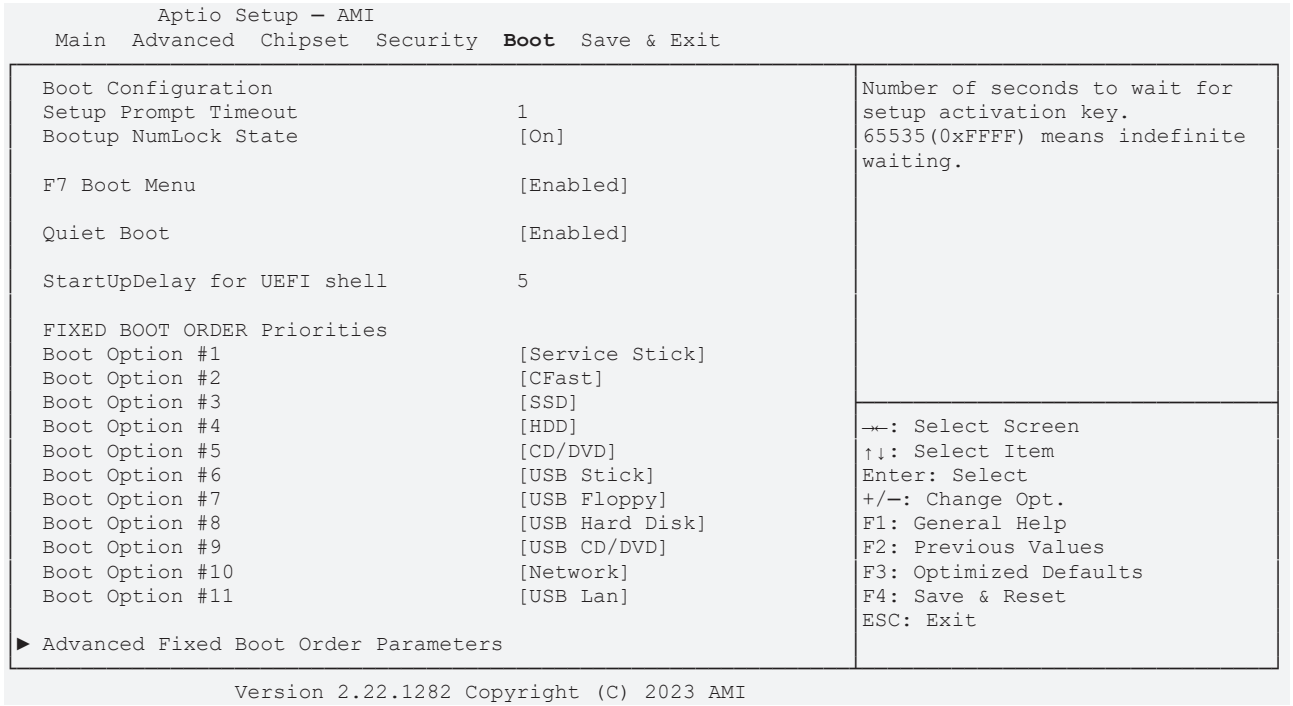
BIOS entry	Options
Vendor Keys	None
Authorized TimeStamps	See box

7.5.1.3.12 OsRecovery Signatures



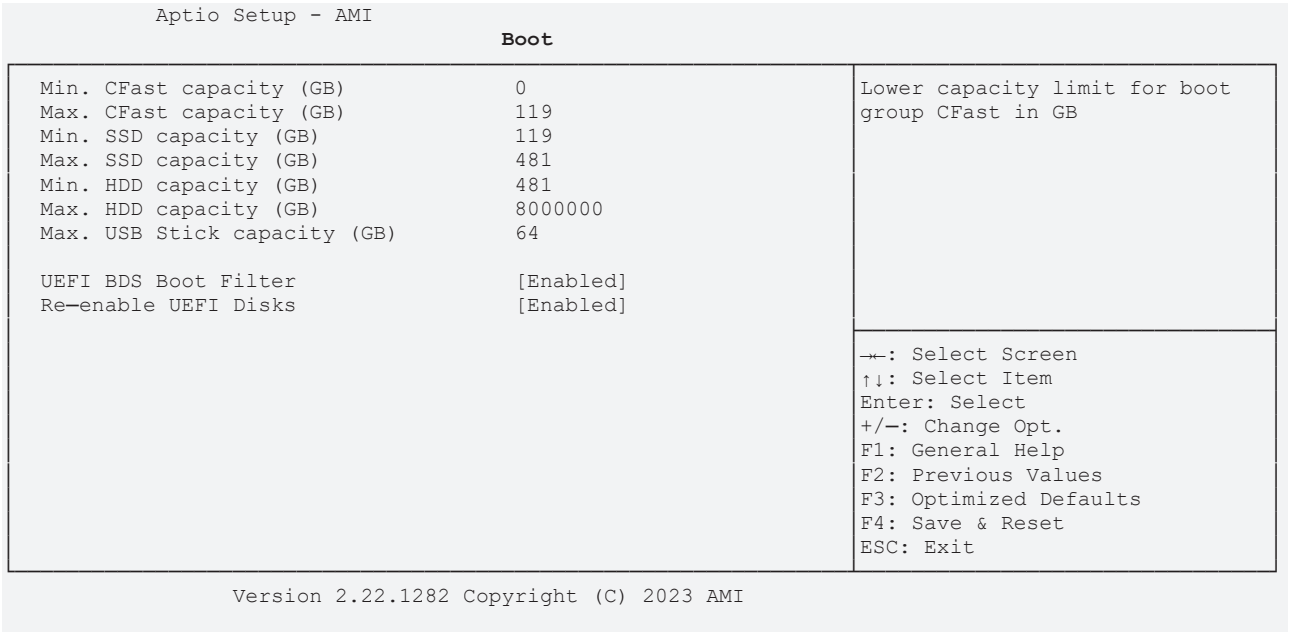
BIOS entry	Options
Vendor Keys	None
OsRecovery Signatures	See box

7.6 Boot CB3072



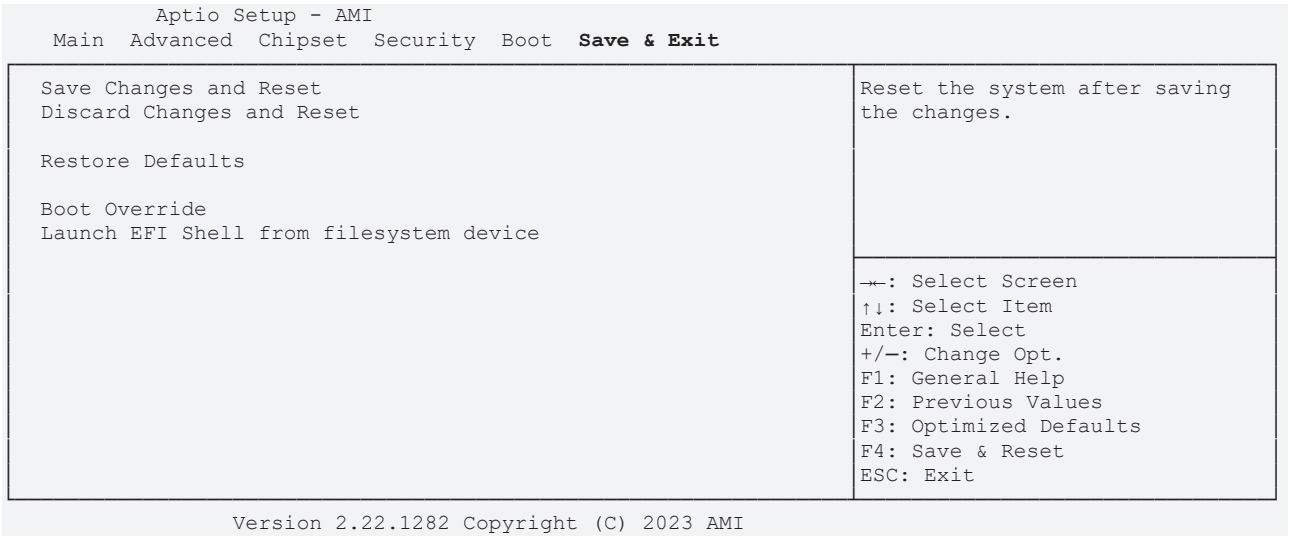
BIOS entry	Options
Boot Configuration	
Setup Prompt Timeout	None
Bootup NumLok State	On / Off
F7 Boot Menu	Enabled / Disabled
Quiet Boot	Enabled / Disabled
StartUpDelay for UEFI shell	None
Fixed Boot Order Priorities	
Boot Option #1 - 11	Here you can set the order of the boot media to be used.
▶Advanced Fixed Boot Order Parameters	Submenu see: Advanced Fixed Boot Order Parameters [▶ 124]

7.6.1 Advanced Fixed Boot Order Parameters



BIOS entry	Options
Min. CFast capacity (GB)	None
Max. CFast capacity (GB)	None
Min. SSD capacity (GB)	None
Max. SSD capacity (GB)	None
Min. HDD capacity (GB)	None
Max. HDD capacity (GB)	None
Max. USB Stick capacity (GB)	None
UEFI BDS Boot Filter	Enabled / Disabled
Re-enable UEFI Disks	Enabled / Disabled

7.7 Save & Exit CB3072



BIOS entry	Options
Save Changes and Reset	
Discard Changes and Reset	Press enter key
Restore Optimized Defaults	Press enter key
Boot Override	
Launch EFI Shell from filesystem device	Press enter key

7.8 BIOS update

The "DecdFlsh" program and a bootable medium with the latest BIOS version are used if the BIOS needs to be updated. When doing this it is important to start the program from a DOS environment without a virtual memory manager such as "EMM386.EXE". If such a memory manager is loaded, the program will abort with an error message or cause a crash.

DecdFlsh is a program for the automatic updating of the BIOS on all boards with AMI-BIOS. All files contained in the zip file must be unpacked into a directory, from where

```
DecdFlsh Bios-Dateiname
```

calling takes place. The name of the BIOS file and its length are checked. The BIOS will now be programmed.

The system must not be interrupted during the flashing process, as otherwise the update will abort and the BIOS on the board will be destroyed. The Flash procedure takes about 75 seconds. The necessary firmware update takes place automatically.

NOTICE

Risk of damage due to incorrect update procedure!

If the BIOS update is performed incorrectly, the board may become unusable. Therefore a BIOS update should only be done if the corrections / additions that the new BIOS version brings with it are really needed.

Before a planned BIOS update, it is essential to ensure that the BIOS file to be reloaded is really released for exactly this board and for exactly this board version. If an inappropriate file is used, the board will inevitably not boot afterwards.

8 Mechanical drawing

Dimensions

All dimensions are in mm.

8.1 PCB: dimensions

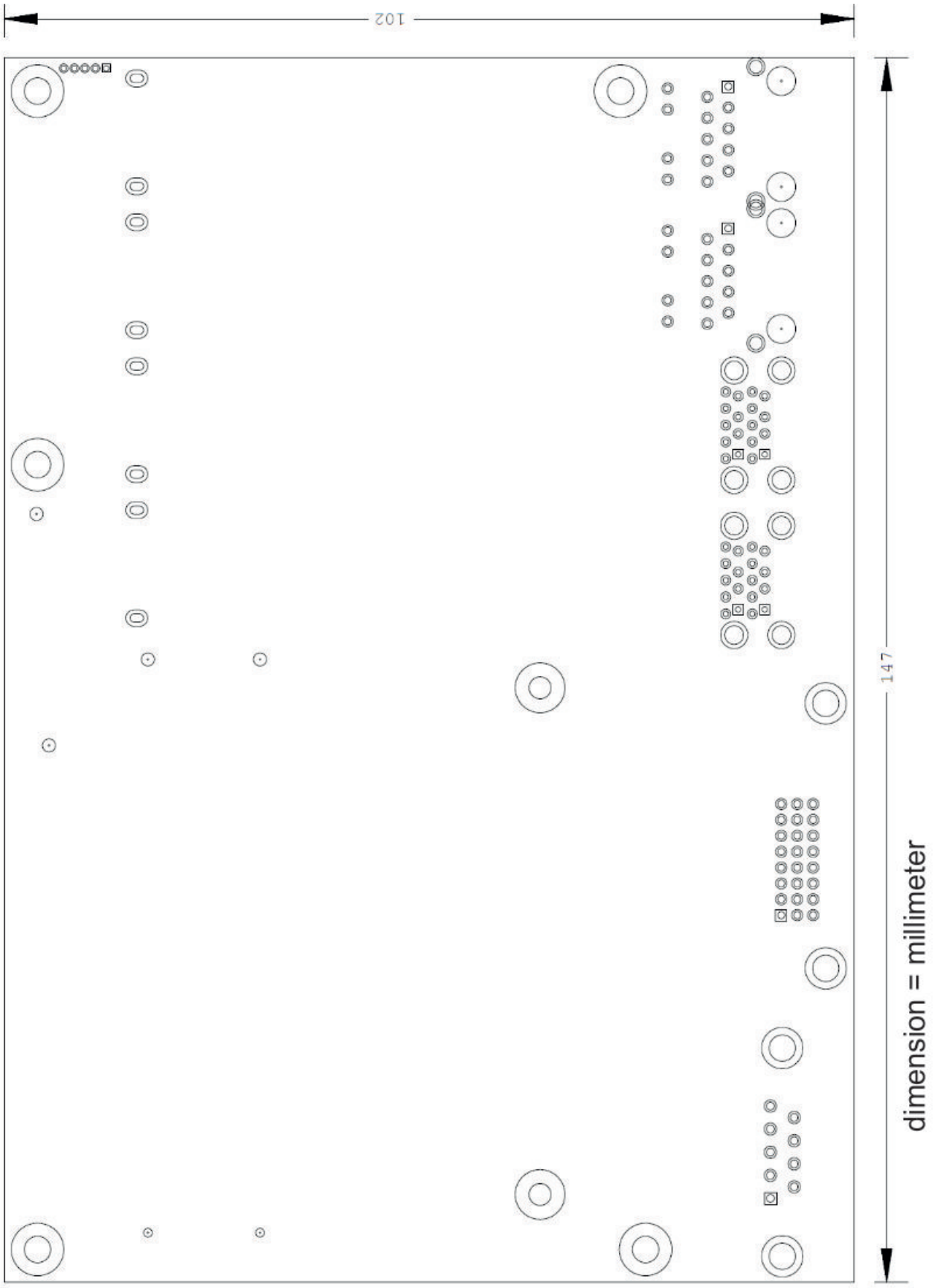


Fig. 18: CB3072 MZ

8.2 PCB: mounting holes

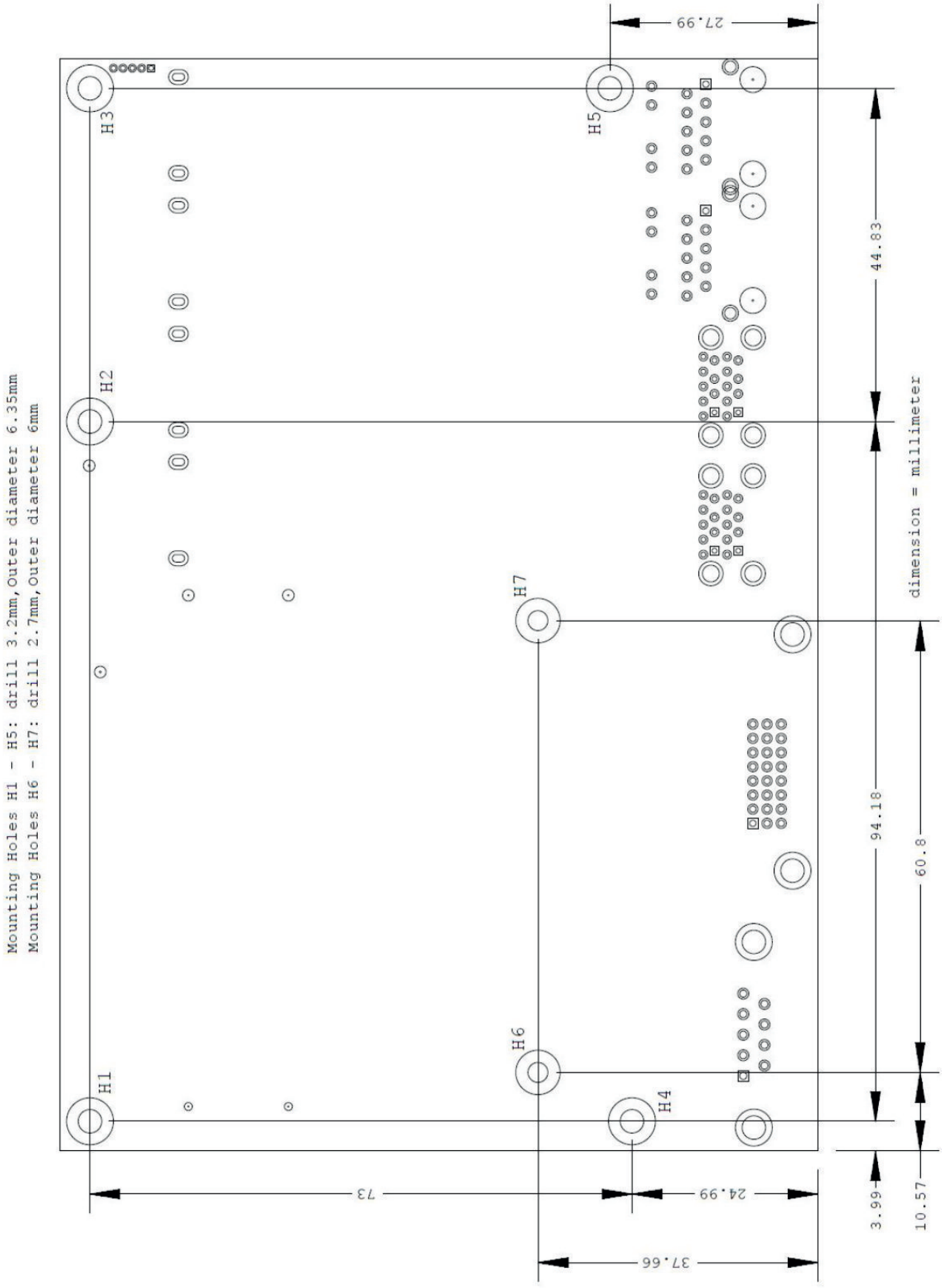


Fig. 19: CB3072 MZ-MH

8.3 PCB: Cooling bottom

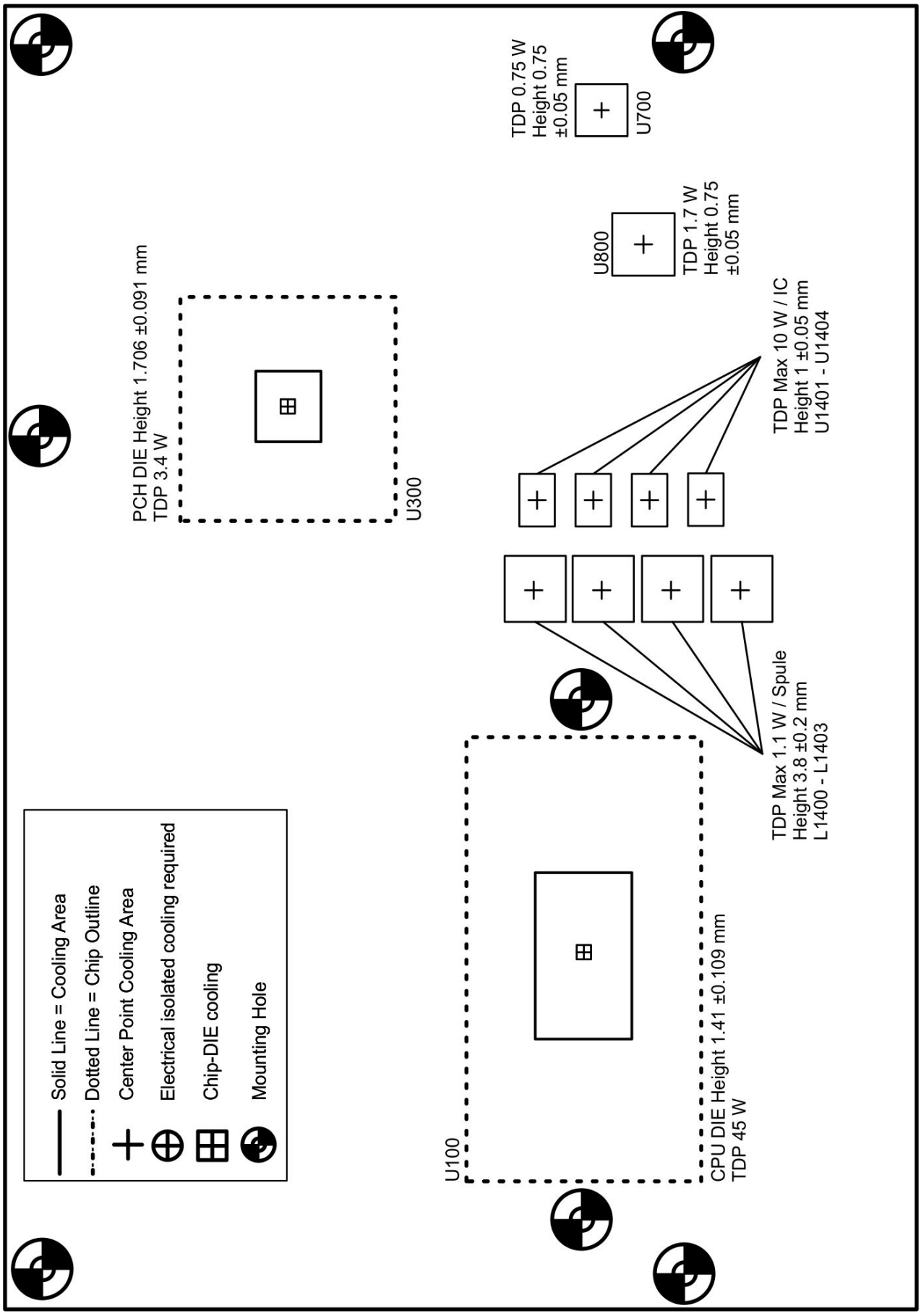


Fig. 20: CB3072-Cooling Bottom

9 Technical data

9.1 Electrical data

Power supply	
Board	3.3 V, 5 V and 12 V (± 5 %)
RTC	≥ 3 V
Current consumption	
RTC	≤ 10 µA

9.2 Environmental conditions

Temperature range	
Operating	0 °C ... +60 °C (extended temperature range on request)
Storage	-25 °C ... +85 °C
Shipping	-25 °C ... +85 °C, for packed boards

Temperature changes	
Operating	0.5 °C per minute, 7.5 °C in 30 minutes
Storage	1.0 °C per minute
Shipping	1.0 °C per minute, for packed boards

Relative humidity	
Operating	5% ... 85% (non-condensing)
Storage	5% ... 95% (non-condensing)
Shipping	5% ... 100% (non-condensing), for packed boards

Impact	
Operating	150 m/s², 6 ms
Storage	400 m/s², 6 ms
Shipping	400 m/s², 6 ms, for packed boards

Vibration	
Operating	10 ... 58 Hz, amplitude 0.075 mm
Storage	5 to 9 Hz, 3.5 mm amplitude 9 to 500 Hz, 10 m/s²
Shipping	5 ... 9 Hz, 3.5 mm amplitude 9 ... 500 Hz, 10 m/s², for packed boards

Note on impact and vibration resistance

The specifications for impact and vibration resistance refer only to the motherboard itself without heat sink, memory module, cabling, etc.

9.3 Thermal specifications

The board is specified for an ambient temperature range from 0 °C ... +60 °C (extended temperature range on request). You must also ensure that the temperature of the processor die does not exceed 100 °C. To ensure this, a suitable cooling concept must be implemented that is oriented to the maximum power consumption of the processor/chipset. Please note that any existing controllers must be taken into account in the cooling concept. The power consumption of these function blocks may be of the same order of magnitude as the power consumption of the processor.

The board is prepared with holes for the use of suitable cooling solutions. We have a series of compatible cooling components in our range. Your distributor will be pleased to assist you in selecting suitable solutions.

NOTICE

Prevent the maximum die temperature being exceeded!

It is the end customer's responsibility to ensure that the die temperature of the processor does not exceed 100 °C! Continuous overheating can destroy the board!

If the temperature exceeds 100 °C, the ambient temperature needs to be reduced. Ensure sufficient air circulation if necessary.

10 Support and Service

Beckhoff and their partners around the world offer comprehensive support and service, making available fast and competent assistance with all questions related to Beckhoff products and system solutions.

Beckhoff's branch offices and representatives

Please contact your Beckhoff branch office or representative for local support and service on Beckhoff products!

The addresses of Beckhoff's branch offices and representatives round the world can be found on our internet page: www.beckhoff.com

You will also find further documentation for Beckhoff components there.

Beckhoff Support

Support offers you comprehensive technical assistance, helping you not only with the application of individual Beckhoff products, but also with other, wide-ranging services:

- support
- design, programming and commissioning of complex automation systems
- and extensive training program for Beckhoff system components

Hotline:	+49 5246 963-157
e-mail:	support@beckhoff.com

Beckhoff Service

The Beckhoff Service Center supports you in all matters of after-sales service:

- on-site service
- repair service
- spare parts service
- hotline service

Hotline:	+49 5246 963-460
e-mail:	service@beckhoff.com

Beckhoff Headquarters

Beckhoff Automation GmbH & Co. KG

Huelshorstweg 20
33415 Verl
Germany

Phone:	+49 5246 963-0
e-mail:	info@beckhoff.com
web:	www.beckhoff.com

11 Appendix I: Post Codes

During the boot phase, the BIOS generates a series of status messages (so-called "POST Codes"), which can be output with the help of a suitable reading device (POST Code card). The meanings of the POST Codes are explained in the document "Aptio™ 5.x Status Codes" from American Megatrends®, which is available from the website http://www.ami.com. In addition, the following OEM POST Codes are output:

Code	Description
87h	BIOS-API started
88h	PCA9535 started
89h	PWRCTRL firmware started

12 Appendix II: Resources

12.1 Interrupt CB3072

The system BIOS determines the interrupt requests (IRQs) for all devices that request interrupts. In the operating system, interrupts can be dynamically forwarded to IRQs and can support a reassignment of IRQs if there is a conflict with the current use of the interrupt.

Further information can be found in chipset manual: Specifications and documents

12.2 PCI-Devices CB3072

The PCI devices listed here all exist on the board, including those that are detected and configured by the BIOS. Due to the BIOS setup settings it may be the case that various PCI devices or functions of devices are not activated. If devices are disabled, the bus numbers of other devices may change as a result.

Bus	Dev.	Fct.	Controller / Slot
00	00	00	Host Bridge ID 3E35
00	02	00	VGA Controller ID 3EA0
00	04	00	Data Acquisition/Signal Processing Controller ID 1903
00	08	00	System Device ID 1911
00	12	00	Data Acquisition/Signal Processing Controller ID 9DF9
00	14	00	XHCI USB Controller ID 9DED
00	14	02	RAM Controller ID 9DEF
00	16	00	Communication Device ID 9DE0
00	17	00	RAID Controller ID 282A
00	1C	00	PCI-to-PCI Bridge (PCIE) ID 9DB8
00	1C	07	PCI-to-PCI Bridge (PCIE) ID 9DBF
00	1D	00	PCI-to-PCI Bridge (PCIE) ID 9DB0
00	1D	03	PCI-to-PCI Bridge (PCIE) ID 9DB3
00	1F	00	ISA Bridge ID 9D84
00	1F	03	HD Audio Device ID 9DC8
00	1F	04	SMBus Controller ID 9DA3
00	1F	05	Controller ID 9DA4
00	1F	06	Ethernet Controller ID 15BD
02	00	00	Ethernet Controller (PCIE) ID 1533
03	00	00	Mass Storage Controller (PCIE) ID 5008
04	00	00	Ethernet Controller (PCIE) ID 1533

12.3 SMB-Devices CB3072

The following table lists the reserved SM-Bus device addresses in 8-bit notation.

NOTICE

These address ranges may not be used by external devices even if the component assigned in the table doesn't exist on the motherboard.

Address	Function
B0, B2, B8, BA	PWCTR3
70, 72	PostCode
34 (old B4)	CA2000-0021/23 (power supply unit)
40	PCA9535BS (16-bit I2C and SMBus, low power I/O port with interrupt)
..	S UPS

Beckhoff Automation GmbH & Co. KG
Hülshorstweg 20
33415 Verl
Germany
Phone: +49 5246 9630
info@beckhoff.com
www.beckhoff.com