BECKHOFF New Automation Technology

Operating Manual | EN

CB1076

Computerboard

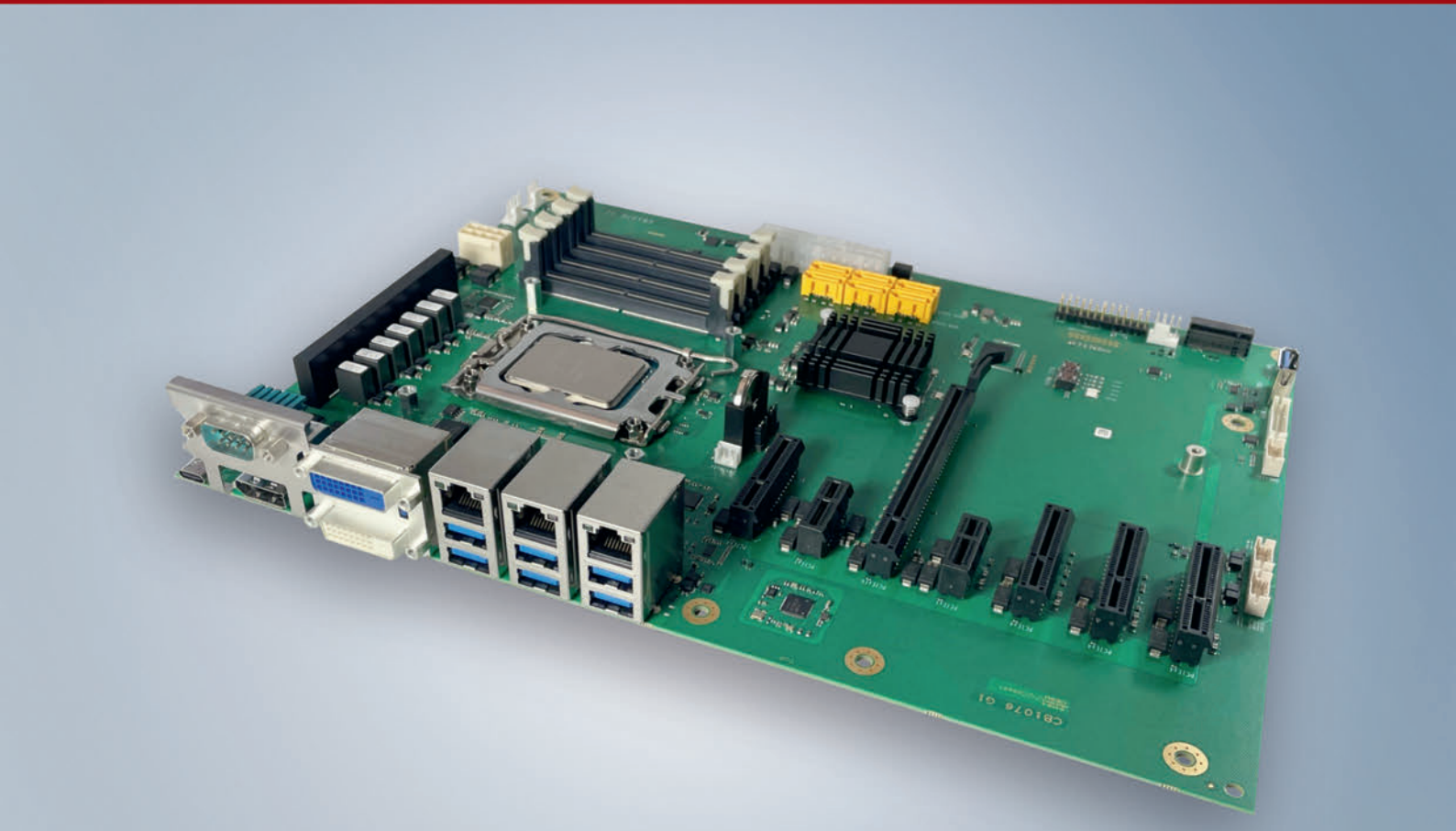

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Table of contents

1 Documentation issue status

Version	Modifications
0.1	First preliminary version, HW version G1
1.0	First release with BIOS version 0.08, revision 1

2 Notes on the documentation

This description is intended exclusively for trained specialists in control and automation technology who are familiar with the applicable national standards.
For installation and commissioning of the components, it is absolutely necessary to observe the documentation and the following notes and explanations.
It is the duty of the responsible staff to use the documentation published at the respective time of each installation and commissioning.

The responsible staff must ensure that the application or use of the products described satisfy all the requirements for safety, including all the relevant laws, regulations, guidelines and standards.

Origin of the document

This documentation was originally written in German. All other languages are derived from the German original.

Disclaimer

The documentation has been prepared with care. The products described are, however, constantly under development.
We reserve the right to revise and change the documentation at any time and without notice.
No claims for the modification of products that have already been supplied may be made on the basis of the data, diagrams, and descriptions in this documentation.

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EP1590927, EP1789857, EP1456722, EP2137893, DE102015105702
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3 Safety instructions

Safety regulations

Please observe the following safety instructions and explanations!
Product-specific safety instructions can be found on following pages or in the mounting, wiring, commissioning areas, etc.

Exclusion of liability

All of the components are supplied in specific hardware and software configurations depending on the application requirements. Modifications to hardware or software configurations other than those described in the documentation are not permitted, and nullify the liability of Beckhoff Automation GmbH & Co. KG.

Personnel qualification

This description is only intended for trained specialists in control, automation, and drive technology who are familiar with the applicable national standards.

Description of symbols

In this documentation the following symbols are used with an accompanying safety instruction or note. The safety instructions must be read carefully and followed without fail!

⚠ DANGER

Serious risk of injury!

Failure to follow the safety instructions associated with this symbol directly endangers human life and health!

⚠ WARNING

Risk of injury!

Failure to follow the safety instructions associated with this symbol endangers human life and health!

⚠ CAUTION

Personal injuries!

Failure to follow the safety instructions associated with this symbol can lead to physical injuries!

NOTICE

Damage to the environment or devices

Failure to follow the instructions associated with this symbol can lead to damage to the environment or equipment.

Tip or pointer

This symbol indicates information that contributes to better understanding.

This symbol indicates important information regarding UL approval.

Intended use

The CB1076 Computer Board was designed and developed exclusively for configuration in automation processes. To that end the board is equipped with external interfaces in order to acquire or output digital or analog signals or forward them to higher-level components.

The specified limits for electrical and technical data must be adhered to.

Any other use is regarded as inappropriate.

4 Overview

4.1 Properties

The CB1076 is an industrial motherboard in the ATX form factor. It is based on Intel®'s latest hybrid technology. Intel® processors of the 12th and 13th generation (Core™, Celeron™ and Pentium) are installed. The Intel® R680E-PCH chipset is used.

This new hybrid design has a combination of performance and efficiency cores. Up to 24 kB are available. It can be equipped with up to 128 GB of memory via four SO-DIMM slots. A maximum clock rate of up to 5600 MHz is possible.

The large number of internal and external connections make the CB1076 a very versatile motherboard:

- 14x USB interfaces, including 7x USB3.1 Gen2, 1x USB-C, 6x USB2.0
- 1x LAN connection 1 Gb
- 2x LAN connections 2.5 Gb
- DVI/HDMI and DisplayPort connection
- 1x M.2 Key M (SATA/NVME)
- 1x PCIe x16 slot
- 2x serial interfaces, 1x external, 1x onboard
- 2x PCIe x1
- 4x PCIe x4
- 6x SATA ports 6G onboard

The board provides basic safety functions via the integrated Trusted Platform Module (TPM) as a Trusted Computing Platform.

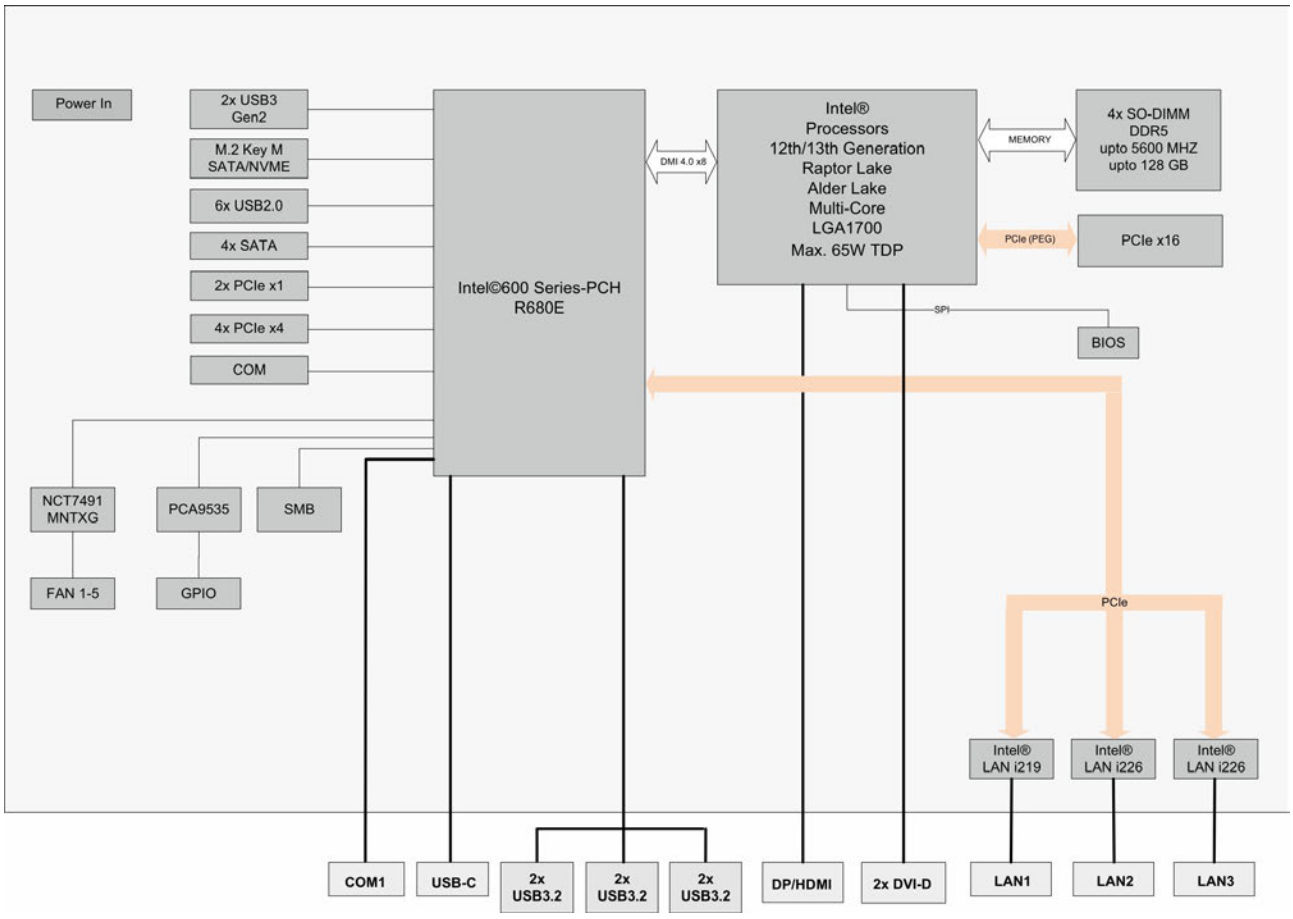


Fig. 1: CB1076 block diagram

4.2 List of features

CB1076	ATX-Board
CPU	Intel® processors of the 12th/13th generation Alder Lake and Raptor Lake Intel® Celeron® G6900E Intel® Pentium® G7400E Intel® Core™ i3-13100E Intel® Core™ i5-13400E Intel® Core™ i7-13700E Intel® Core™ i9-13900E
Chipset	Intel® R680E-PCH
Socket	LGA 1700
Memory	4x SO-DIMM up to 128 GB, DDR5 up to 5600 MHz
I/O external	1x USB-C 6x USB3.1 Gen2 1x LAN 1 Gb 2x LAN 2.5 Gb 1x DP 1.2 2x DVI-D (DVI or HDMI 1.4) 1x COM
I/O internal	1x M.2 (M) (SATA, NVME) 1x COM 6x SATA 3.0, RAID 0/1/5/10 2x PCIe x1 (3.0) 4x PCIe x4 (3.0) 1x PCIe x16 (5.0) 6x USB 2.0 1x USB3 8x GPIO 5x fans (of which 3 are controlled fans) 1x SMB connection 1x 2x9-pin connector system 1x 2x13-pin connector ATX Bh system
Graphic resolution	DisplayPort1.2: 4096x2304@60 Hz HDMI1.4: 4096x2160@30 Hz
RTC	Internal or external CMOS battery
BIOS	AMI® Aptio V
Power supply	Standard ATX power supply
Format	305 x 220 mm

Availability of the processors

The list of features lists all the processors that can be ordered. Their actual availability depends on the manufacturer.

4.3 Specifications and documents

The following documents, specifications or webpages were used for the preparation of this manual or as further technical documentation respectively.

- **PCI specification**
- Version 2.3 or 3.0
- www.pcisig.com
- **PCI Express® Base Specification**
- Version 5.0
- www.pcisig.com
- **ACPI specification**
- Version 5.0
- www.acpi.info
- **ATA/ATAPI specification**
- Version 7 Rev. 1
- www.t13.org
- **USB specifications**
- www.usb.org
- **SMBus specification**
- Version 2.0
- www.smbus.org
- **Intel® chip descriptions**
- Intel® Core™ Processor Product Family datasheet
- www.intel.com
- **Intel® chip description**
- i219 Datasheet
- i225/226 Datasheet
- www.intel.com
- **SMSC® chip description**
- SCH3114 Datasheet (NDA required)
- www.smsc.com
- **American Megatrends®**
- Aptio™ Text Setup Environment (TSE) User Manual
- www.ami.com
- **American Megatrends®**
- Aptio™ 5.x Status Codes
- www.ami.com

5 Notes on information security

The products of Beckhoff Automation GmbH & Co. KG (Beckhoff), insofar as they can be accessed online, are equipped with security functions that support the secure operation of plants, systems, machines and networks. Despite the security functions, the creation, implementation and constant updating of a holistic security concept for the operation are necessary to protect the respective plant, system, machine and networks against cyber threats. The products sold by Beckhoff are only part of the overall security concept. The customer is responsible for preventing unauthorized access by third parties to its equipment, systems, machines and networks. The latter should be connected to the corporate network or the Internet only if appropriate protective measures have been set up.

In addition, the recommendations from Beckhoff regarding appropriate protective measures should be observed. Further information regarding information security and industrial security can be found in our https://www.beckhoff.com/secguide.

Beckhoff products and solutions undergo continuous further development. This also applies to security functions. In light of this continuous further development, Beckhoff expressly recommends that the products are kept up to date at all times and that updates are installed for the products once they have been made available. Using outdated or unsupported product versions can increase the risk of cyber threats.

To stay informed about information security for Beckhoff products, subscribe to the RSS feed at https://www.beckhoff.com/secinfo.

6 Interfaces

6.1 Interface overview

The figures show the interfaces of the CB1076 board in a top view. The table shows the function of the respective interface as well as a reference to the manual page for further information. The listing is clockwise, starting with P1304 USB-C

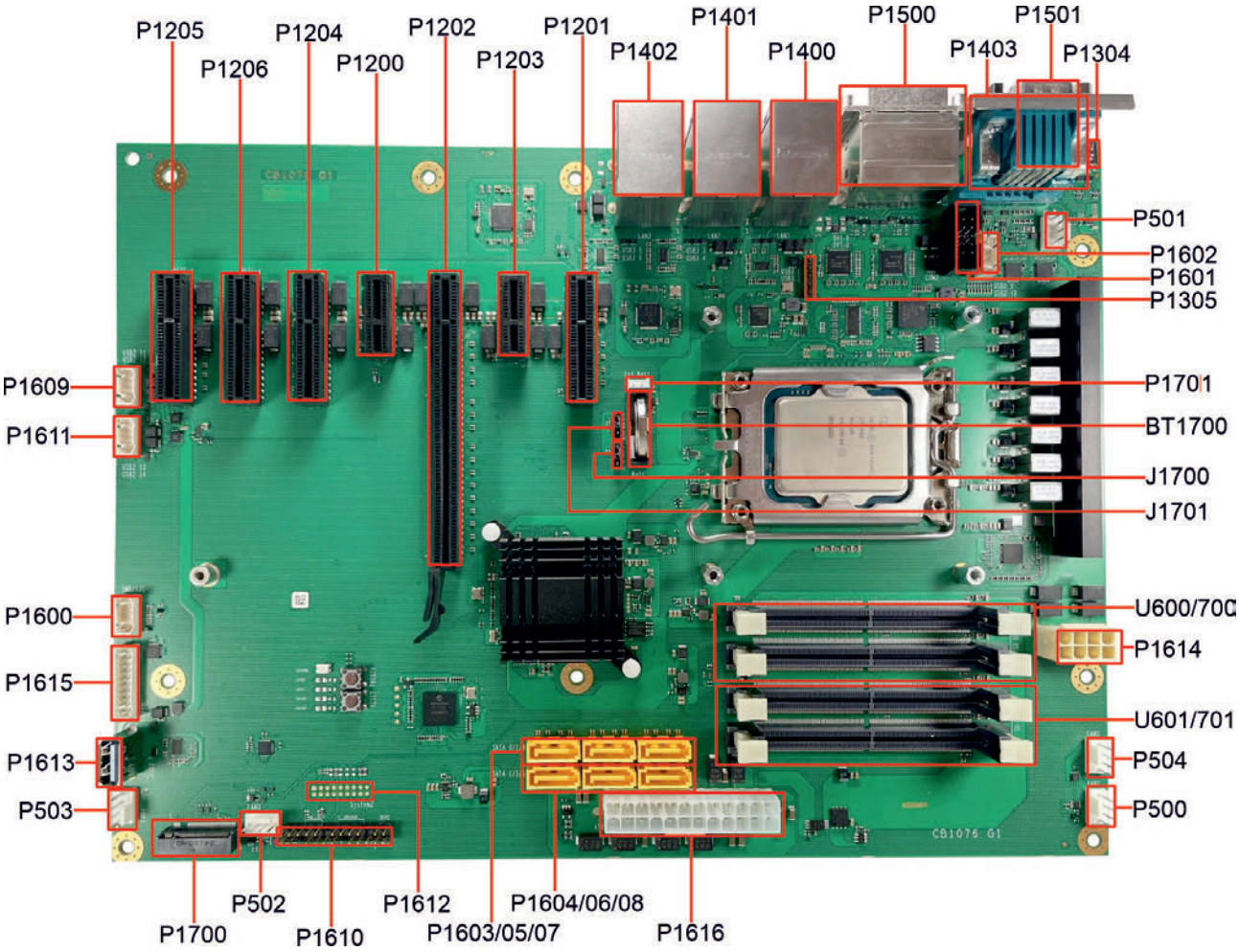


Fig. 2: CB1076 interfaces

Number	Function (designation)	Page
P1304	USB-C	USB-C Port (P1304) [▶ 15]
P501	4-pin connector (FAN)	FAN 1 – 5 (P500/1/2/3/4) [▶ 16]
P1602	2x5-pin connector (USB2.0)	USB 2.0 (P1602/P1609/P1611) [▶ 17]
P1601	2x5-pin connector (COM2)	Serial interfaces COM2 (P1601) [▶ 18]
P1305	5-pin connector (programming port)	Programming port (P1305) [▶ 19]
P1701	2-pin connector (RTC-BAT)	Battery (BT1700/P1701) [▶ 20]
BT1700	Battery holder for CR2032	Battery (BT1700/P1701) [▶ 20]
J1700/ J1701	Jumper Clear CMOS 1/CMOS2	
U600/700	SO-DIMM262 A1 and A2	Memory (U600, U700, U601, U701) [▶ 21]
P1614	2x4-pin connector MiniFit 12 V	Power supply (P1614/P1616) [▶ 28]
U601/701	SO-DIMM262 B1 and B2	Memory (U600, U700, U601, U701) [▶ 21]
P504	4-pin connector (FAN)	FAN 1 – 5 (P500/1/2/3/4) [▶ 16]
P500	4-pin connector (FAN)	FAN 1 – 5 (P500/1/2/3/4) [▶ 16]
P1616	2x12-pin connector ATX-Power	Power supply (P1614/P1616) [▶ 28]
P1604/06/08	SATA 2/4/6	SATA (P1603 – P1608) [▶ 29]
P1603/05/07	SATA 1/3/5	SATA (P1603 – P1608) [▶ 29]
P1612	2x9-pin connector system	Reserved
P1610	2x13-pin connector ATX Bh system	System Port (P1610) [▶ 29]
P502	4-pin connector FAN	FAN 1 – 5 (P500/1/2/3/4) [▶ 16]
P1700	M.2M PCIe/SATA	M.2 Key-M (P1700) [▶ 30]
P503	4-pin connector (FAN)	FAN 1 – 5 (P500/1/2/3/4) [▶ 16]
P1613	Connector USB3.0	USB3.1 Gen2 Typ A (P1613) [▶ 33]
P1615	2x10-pin connector (GPIO)	GPIO (P1615) [▶ 34]
P1600	2x5-pin connector (SMBus)	SMB/I²C (P1600) [▶ 34]
P1611	2x5-pin connector USB 2.0	USB 2.0 (P1602/P1609/P1611) [▶ 17]
P1609	2x5-pin connector USB 2.0	USB 2.0 (P1602/P1609/P1611) [▶ 17]
P1205/06/04	PCIe x4 socket	PCIe x4 (P1205/P1206/P1204/P1201) [▶ 35]
P1200	PCIe x1 socket	PCIe x1 (P1200/P1203) [▶ 36]
P1202	PCIe x16 socket	PCIe x16 (P1202) [▶ 37]
P1203	PCIe x1 socket	PCIe x1 (P1200/P1203) [▶ 36]
P1201	PCIe x4 socket	PCIe x4 (P1205/P1206/P1204/P1201) [▶ 35]
P1402	LAN 2.5 Gb + USB3.1Gen2	LAN 2.5 Gbit and USB 3.1Gen2 (P1402/P1401/P1400) [▶ 40]
P1401	LAN 2.5 Gb + USB3.1Gen2	LAN 2.5 Gbit and USB 3.1Gen2 (P1402/P1401/P1400) [▶ 40]
P1400	LAN 1 Gb + USB3.1Gen2	LAN 2.5 Gbit and USB 3.1Gen2 (P1402/P1401/P1400) [▶ 40]
P1500	DVI-D A+B	DVI-D (P1500A/B) [▶ 42]
P1403	DSUB9M (COM1)	Serial interface COM1 (P1403) [▶ 43]
P1501	DisplayPort	Display Port (P1501) [▶ 43]

6.2 USB-C Port (P1304)

24-pin USB-C connector. Signals with up to 10 Gbit/s can be led out via this connector.

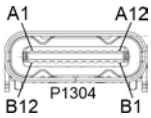


Fig. 3: CB1076 USB-C

Pin assignment USB-C					
Description	**Name**	**Pin**		**Name**	**Description**
Ground	GND	A1	B12	GND	Ground
Transmit+	TX1+	A2	B11	RX1+	Receive+
Transmit-	TX1-	A3	B10	RX1-	Receive-
Voltage	VBUS1	A4	B9	VBUS3	Voltage
Configuration channel	CC1	A5	B8	SBU2	Sideband Use2
USB2.0-Signal+	D0+	A6	B7	D1-	USB2.0-Signal-
USB2.0-Signal-	D0-	A7	B6	D1+	USB2.0-Signal+
Sideband Use1	SBU1	A8	B5	Vconn/ CC2	Configuration channel
Voltage	VBUS2	A9	B4	VBUS4	Voltage 5 V
Receive-	RX2-	A10	B3	TX2-	Transmit-
Receive+	RX2+	A11	B2	TX2+	Transmit+
Ground	GND	A12	B1	GND	Ground

6.3 FAN 1 – 5 (P500/1/2/3/4)

The module has five 4-pin fan connections, with which you can connect fans with a supply voltage of 12 V directly to the module. The connections FAN1, FAN2 and FAN3 have a speed monitoring function. The connected fan must supply a corresponding tachometer signal if this is to be used.

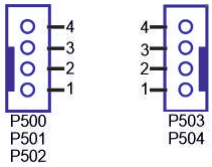


Fig. 4: CB1076 FAN 1-5

Pin assignment FAN 1 (P500)			
P500	**Pin**	**Name**	**Description**
	1	FANON	Ground switched fan 1
	2	12 V	12 V
	3	TACH1	Monitoring fan 1
	4	PWM1	Fan 1 power management

Pin assignment FAN 2 (P501)			
P501	**Pin**	**Name**	**Description**
	1	FANON	Ground switched fan 2
	2	12 V	12 V
	3	TACH2	Monitoring fan 2
	4	PWM2	Fan 2 power management

Pin assignment FAN 3 (P502)			
P502	**Pin**	**Name**	**Description**
	1	FANON	Ground switched fan 3
	2	12 V	12 V
	3	TACH3	Monitoring fan 3
	4	PWM3	Fan 3 power management

Pin assignment FAN 4 (P503)			
P503	**Pin**	**Name**	**Description**
	1	FANON	Ground switched fan 4
	2	12 V	12 V
	3	N/C	
	4	PWM3	Fan 3 power management

Pin assignment FAN 5 (P504)			
P504	**Pin**	**Name**	**Description**
	1	FANON	Ground switched fan 5
	2	12 V	12 V
	3	N/C	
	4	PWM1	Fan 1 power management

Parallel assignment for FAN1/5 and FAN 3/4

These connectors are supplied in parallel via the PWM signal.

6.4 USB 2.0 (P1602/P1609/P1611)

Six USB signals are made available via these three 2x5-pin connectors.

The signals comply with USB specification 2.0.

All necessary settings for USB can be made by the BIOS. Note that the "USB mouse and keyboard" function in the BIOS setup is only required if the operating system does not offer USB support. This function should not be selected for settings in the setup and for booting Windows with a USB mouse and keyboard connected, because this would lead to considerable performance limitations.

The individual USB interfaces can supply a current of up to 500 mA and are electronically protected.

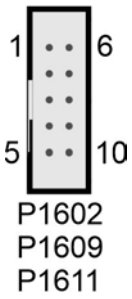


Fig. 5: CB1076 USB 2.0 internal

Pin assignment internal USB 2.0 connector:					
Description	**Name**	**Pin**		**Name**	**Description**
5 V for USB	VCC	1	6	VCC	5 V for USB
Minus data channel USB	USB-	2	7	USB-	Minus data channel USB
Plus data channel USB	USB+	3	8	USB+	Plus data channel USB
Ground	GND	4	9	GND	Ground
Not connected	N/C	5	10	N/C	Not connected

6.5 Serial interfaces COM2 (P1601)

An additional serial interface COM2 is installed on the board in a 2x5-pin connector. The signals correspond to the RS232 standard.

The port address and the interrupt used are set with the help of the BIOS setup.

2x5-pin connector:

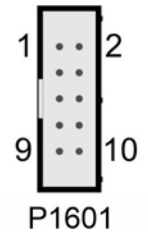


Fig. 6: CB1076 COM 2

Pin assignment COM connector					
Description	**Name**	**Pin**		**Name**	**Description**
Data Carrier Detect-	DCD#	1	2	DSR#	Data Set Ready-
Receive Data	RXD	3	4	RTS	Request to Send
Transmit Data	TXD	5	6	CTS	Clear to Send
Data Terminal Ready-	DTR#	7	8	RI#	Ring Indicator-
Ground	GND	9	10	VCC	Supply voltage 5 V

6.6 Programming port (P1305)

You can transfer programming signals to the board via this 5-pin connection. The supply voltage is 3.3 V.

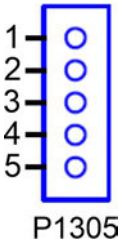


Fig. 7: CB1076 Programming port

Pin assignment programming port		
Pin	**Signal**	**Description**
1	3.3 V	Supply voltage 3.3 V
2	EEP-SMBCLK	SMB-Clock
3	EEP-SMBDAT	SMB Data
4	PMCALERT#	PMC Alert-
5	GND	Ground

6.7 Battery (BT1700/P1701)

The board is supplied with a CR2032 battery holder (BT1700) including a 3 V battery, but can also be connected to an external battery via a two-pin housing connector (P1701) in order to keep the integrated clock supplied in case of a power failure.

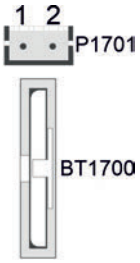


Fig. 8: CB1076 Battery

Pin assignment RTC battery connector		
Pin	**Name**	**Description**
1	BATT	3.3 V battery voltage
2	GND	Ground

6.8 Memory (U600, U700, U601, U701)

Four vertical SO-DIMM memory slots, DDR5- 5600 MT/s, max. 128 GB RAM are installed on the CB1076 board. For technical and mechanical reasons, it is possible that certain memory modules cannot be used. Information regarding the recommended memory modules can be obtained from your distributor.

NOTICE

Memory modules

When populating the memory sockets, make sure that you use identical memory modules.

All timing parameters for the different makes and versions are automatically set by the BIOS.

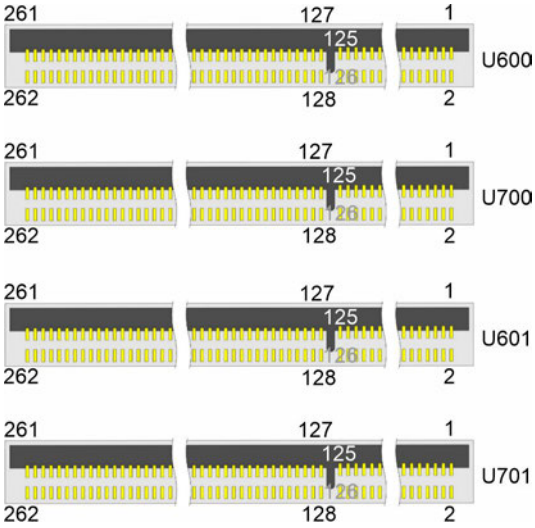


Fig. 9: CB1076 SODIMM-262

Pin assignment memory socket U600/U700					
Description	**Signal**	**Pin1**		**Signal**	**Description**
Supply voltage 5 V	M_VIN	1	2	SA0	Ground
Supply voltage 5 V	M_VIN	3	4	SCL	SMBus-CLK
Reserved	Res1	5	6	SDA	SMBus-Data
Powergood	PWRGOOD	7	8	PWR_EN	Power Enable
Ground	GND	9	10	GND	Ground
Data line A3	ADQ0	11	12	ADQ1	Data line A2
Ground	GND	13	14	GND	Ground
Data line A0	ADQ2	15	16	ADQ3	Data line A1
Ground	GND	17	18	GND	Ground
Ground	ADM0	19	20	ADQS#0	Data Strobe A0 -
Ground	GND	21	22	ADQS0	Data Strobe A0+
Data line A5	ADQ4	23	24	GND	Ground
Ground	GND	25	26	ADQ5	Data line A6
Data line A4	ADQ6	27	28	GND	Ground
Ground	GND	29	30	ADQ7	Data line A7
Data line A11	ADQ8	31	32	GND	Ground
Ground	GND	33	34	ADQ9	Data line A10
Data line A8	ADQ10	35	36	GND	Ground
Ground	GND	37	38	ADQ11	Data line A9
Data Strobe A1 -	ADQS#1	39	40	GND	Ground
Data Strobe A1 +	ADQS1	41	42	ADM1	Ground
Ground	GND	43	44	GND	Ground
Data line A12	ADQ12	45	46	ADQ13	Data line A13
Ground	GND	47	48	GND	Ground
Data line A15	ADQ14	49	50	ADQ15	Data line A14
Ground	GND	51	52	GND	Ground
Data line A17	ADQ16	53	54	ADQ17	Data line A16
Ground	GND	55	56	GND	Ground
Data line A19	ADQ18	57	58	ADQ19	Data line A18
Ground	GND	59	60	GND	Ground
Ground	ADM2	61	62	ADQS#2	Data Strobe A2 -
Ground	GND	63	64	ADQS2	Data Strobe A2 +
Data line A20	ADQ20	65	66	GND	Ground
Ground	GND	67	68	ADQ21	Data line A21
Data line A23	ADQ22	69	70	GND	Ground
Ground	GND	71	72	ADQ23	Data line A22
Data line A25	ADQ24	73	74	GND	Ground
Ground	GND	75	76	ADQ25	Data line A24
Data line A27	ADQ26	77	78	GND	Ground
Ground	GND	79	80	ADQ27	Data line A26
Data Strobe A3 -	ADQS#3	81	82	GND	Ground
Data Strobe A3 +	ADQS 3	83	84	ADM3	Ground
Ground	GND	85	86	GND	Ground
Data line A30	DQ28	87	88	ADQ29	Data line A31
Ground	GND	89	90	GND	Ground
Data line A28	ADQ30	91	92	ADQ31	Data line A29

Pin assignment memory socket U600/U700					
Description	**Signal**	**Pin1**		**Signal**	**Description**
Ground	GND	93	94	GND	Ground
Data line A32	ACB0	95	96	ACB1	Data line A33
Ground	GND	97	98	GND	Ground
Data line A35	ACB2	99	100	ADQS#4	Data Strobe A4 -
Ground	GND	101	102	ADQS4	Data Strobe A4 +
Data line A34	ACB3	103	104	GND	Ground
Ground	GND	105	106	ACS#0	Control A0 -
Command A0	ACA0	107	108	ALERT#	Alert -
Command A1	ACA1	109	110	ACS#1	Control A1 -
Ground	GND	111	112	GND	Ground
Command A2	ACA2	113	114	ACA3	Command A3
Command A4	ACA4	115	116	ACA5	Command A5
Ground	GND	117	118	GND	Ground
Command A6	ACA6	119	120	ACA7	Command A7
Command A8	ACA8	121	122	ACA9	Command A9
Ground	GND	123	124	GND	Ground
Command A10	ACA10	125	126	ACA11	Command A11
Command A12	ACA12	127	128	RES2	Reserved
Ground	GND	129	130	GND	Ground
Clock-Signal A0 +	ACK0	131	132	ACK1	Clock-Signal A1+
Clock-Signal A0 -	ACK#0	133	134	ACK#1	Clock-Signal A1-
Ground	GND	135	136	Ground	GND
Clock-Signal B0 +	BCK0	137	138	BCK1	Clock-Signal B1 +
Clock-Signal B0 -	BCK#0	139	140	BCK#1	Clock-Signal B1 -
Ground	GND	141	142	GND	Ground
Reserved	RES3	143	144	BCA12	Command B12
Command B11	BCA11	145	146	BCA10	Command B10
Ground	GND	147	148	GND	Ground
Command B9	BCA9	149	150	BCA8	Command B8
Command B7	BCA7	151	152	BCA6	Command B6
Ground	GND	153	154	GND	Ground
Command B5	BCA5	155	156	BCA4	Command B4
Command B3	BCA3	157	158	BCA2	Command B2
Ground	GND	159	160	GND	Ground
Command 0 -	BCS#0	161	162	BCA1	Command B1
Reset	RESET	163	164	BCA0	Command B0
Command 1 -	BCS#1	165	166	GND	Ground
Ground	GND	167	168	BCB0	Data line B35
Data Strobe B4 -	BDQS#4	169	170	GND	Ground
Data Strobe B4 +	BDQS4	171	172	BCB1	Data line B32
Ground	GND	173	174	GND	Ground
Data line B33	BCB3	175	176	BCB2	Data line B34
Ground	GND	177	178	GND	Ground
Data line B3	BDQ0	179	180	BDQ1	Data line B2
Ground	GND	181	182	GND	Ground
Data line B0	BDQ2	183	184	BDQ3	Data line B1
Ground	GND	185	186	GND	Ground

Pin assignment memory socket U600/U700					
Description	**Signal**	**Pin1**		**Signal**	**Description**
Ground	BDM0	187	188	BDQS#0	Data Strobe B0 -
Ground	GND	189	190	BDQS0	Data Strobe B0 +
Data line B4	BDQ4	191	192	GND	Ground
Ground	GND	193	194	BDQ5	Data line B5
Data line B6	BDQ6	195	196	GND	Ground
Ground	GND	197	198	BDQ7	Data line B7
Data line B8	BDQ8	199	200	GND	Ground
Ground	GND	201	202	BDQ9	Data line B10
Data line B11	BDQ10	203	204	GND	Ground
Ground	GND	205	206	BDQ11	Data line B9
Data Strobe B1 -	BDQS#1	207	208	GND	Ground
Data Strobe B1 +	BDQS1	209	210	BDM1	Ground
Ground	GND	211	212	GND	Ground
Data line B12	BDQ12	213	214	BDQ13	Data line B13
Ground	GND	215	216	GND	Ground
Data line B15	BDQ14	217	218	BDQ15	Data line B14
Ground	GND	219	220	GND	Ground
Data line B16	BDQ16	221	222	BDQ17	Data line B17
Ground	GND	223	224	GND	Ground
Data line B18	BDQ18	225	226	BDQ19	Data line B19
Ground	GND	227	228	GND	Ground
Ground	BDM2	229	230	BDQS#2	Data Strobe B2 -
Ground	GND	231	232	BDQS2	Data Strobe B2 +
Data line B23	BDQ20	233	234	GND	Ground
Ground	GND	235	236	BDQ21	Data line B21
Data line B22	BDQ22	237	238	GND	Ground
Ground	GND	239	240	BDQ23	Data line B20
Data line B25	BDQ24	241	242	GND	Ground
Ground	GND	243	244	BDQ25	Data line B24
Data line B22	BDQ26	245	246	GND	Ground
Ground	GND	247	248	BDQ27	Data line B26
Data Strobe B3 -	BDQS#3	249	250	GND	Ground
Data Strobe B3 +	BDQS3	251	252	BDM3	Ground
Ground	GND	253	254	GND	Ground
Data line B31	BDQ28	255	256	BDQ29	Data line B28
Ground	GND	257	258	GND	Ground
Data line B29	BDQ30	259	260	BDQ31	Data line B30
Ground	GND	261	262	GND	Ground

Pin assignment memory socket U601/U701					
Description	**Signal**	**Pin1**		**Signal**	**Description**
Supply voltage 5 V	M_VIN	1	2	SA0	Ground
Supply voltage 5 V	M_VIN	3	4	SCL	SMBus-CLK
Reserved	Res1	5	6	SDA	SMBus-Data
Powergood	PWRGOOD	7	8	PWR_EN	Power Enable
Ground	GND	9	10	GND	Ground
Data line A0	ADQ0	11	12	ADQ1	Data line A1
Ground	GND	13	14	GND	Ground
Data line A2	ADQ2	15	16	ADQ3	Data line A3
Ground	GND	17	18	GND	Ground
Ground	ADM0	19	20	ADQS#0	Data Strobe A0 -
Ground	GND	21	22	ADQS0	Data Strobe A0+
Data line A5	ADQ4	23	24	GND	Ground
Ground	GND	25	26	ADQ5	Data line A7
Data line A4	ADQ6	27	28	GND	Ground
Ground	GND	29	30	ADQ7	Data line A6
Data line A11	ADQ8	31	32	GND	Ground
Ground	GND	33	34	ADQ9	Data line A9
Data line A8	ADQ10	35	36	GND	Ground
Ground	GND	37	38	ADQ11	Data line A10
Data Strobe A1 -	ADQS#1	39	40	GND	Ground
Data Strobe A1 +	ADQS1	41	42	ADM1	Ground
Ground	GND	43	44	GND	Ground
Data line A12	ADQ12	45	46	ADQ13	Data line A13
Ground	GND	47	48	GND	Ground
Data line A15	ADQ14	49	50	ADQ15	Data line A14
Ground	GND	51	52	GND	Ground
Data line A16	ADQ16	53	54	ADQ17	Data line A17
Ground	GND	55	56	GND	Ground
Data line A20	ADQ18	57	58	ADQ19	Data line A19
Ground	GND	59	60	GND	Ground
Ground	ADM2	61	62	ADQS#2	Data Strobe A2 -
Ground	GND	63	64	ADQS2	Data Strobe A2 +
Data line A18	ADQ20	65	66	GND	Ground
Ground	GND	67	68	ADQ21	Data line A23
Data line A22	ADQ22	69	70	GND	Ground
Ground	GND	71	72	ADQ23	Data line A21
Data line A25	ADQ24	73	74	GND	Ground
Ground	GND	75	76	ADQ25	Data line A24
Data line A26	ADQ26	77	78	GND	Ground
Ground	GND	79	80	ADQ27	Data line A27
Data Strobe A3 -	ADQS#3	81	82	GND	Ground
Data Strobe A3 +	ADQS 3	83	84	ADM3	Ground
Ground	GND	85	86	GND	Ground
Data line A31	DQ28	87	88	ADQ29	Data line A29
Ground	GND	89	90	GND	Ground
Data line A30	ADQ30	91	92	ADQ31	Data line A28

Pin assignment memory socket U601/U701					
Description	**Signal**	**Pin1**		**Signal**	**Description**
Ground	GND	93	94	GND	Ground
Data line A32	ACB0	95	96	ACB1	Data line A34
Ground	GND	97	98	GND	Ground
Data line A33	ACB2	99	100	ADQS#4	Data Strobe A4 -
Ground	GND	101	102	ADQS4	Data Strobe A4 +
Data line A35	ACB3	103	104	GND	Ground
Ground	GND	105	106	ACS#0	Control A0 -
Command A0	ACA0	107	108	ALERT#	Alert -
Command A1	ACA1	109	110	ACS#1	Control A1 -
Ground	GND	111	112	GND	Ground
Command A2	ACA2	113	114	ACA3	Command A3
Command A4	ACA4	115	116	ACA5	Command A5
Ground	GND	117	118	GND	Ground
Command A6	ACA6	119	120	ACA7	Command A7
Command A8	ACA8	121	122	ACA9	Command A9
Ground	GND	123	124	GND	Ground
Command A10	ACA10	125	126	ACA11	Command A11
Command A12	ACA12	127	128	RES2	Reserved
Ground	GND	129	130	GND	Ground
Clock-Signal A0 +	ACK0	131	132	ACK1	Clock-Signal A1+
Clock-Signal A0 -	ACK#0	133	134	ACK#1	Clock-Signal A1-
Ground	GND	135	136	GND	Ground
Clock-Signal B0 +	BCK0	137	138	BCK1	Clock-Signal B1 +
Clock-Signal B0 -	BCK#0	139	140	BCK#1	Clock-Signal B1 -
Ground	GND	141	142	GND	Ground
Reserved	RES3	143	144	BCA12	Command B12
Command B11	BCA11	145	146	BCA10	Command B10
Ground	GND	147	148	GND	Ground
Command B9	BCA9	149	150	BCA8	Command B8
Command B7	BCA7	151	152	BCA6	Command B6
Ground	GND	153	154	GND	Ground
Command B5	BCA5	155	156	BCA4	Command B4
Command B3	BCA3	157	158	BCA2	Command B2
Ground	GND	159	160	GND	Ground
Command 0 -	BCS#0	161	162	BCA1	Command B1
Reset	RESET	163	164	BCA0	Command B0
Command 1 -	BCS#1	165	166	GND	Ground
Ground	GND	167	168	BCB0	Data line B35
Data Strobe B4 -	BDQS#4	169	170	GND	Ground
Data Strobe B4 +	BDQS4	171	172	BCB1	Data line B34
Ground	GND	173	174	GND	Ground
Data line B33	BCB3	175	176	BCB2	Data line B32
Ground	GND	177	178	GND	Ground
Data line B1	BDQ0	179	180	BDQ1	Data line B0
Ground	GND	181	182	GND	Ground
Data line B3	BDQ2	183	184	BDQ3	Data line B2
Ground	GND	185	186	GND	Ground

Pin assignment memory socket U601/U701					
Description	**Signal**	**Pin1**		**Signal**	**Description**
Ground	BDM0	187	188	BDQS#0	Data Strobe B0 -
Ground	GND	189	190	BDQS0	Data Strobe B0 +
Data line B5	BDQ4	191	192	GND	Ground
Ground	GND	193	194	BDQ5	Data line B4
Data line B6	BDQ6	195	196	GND	Ground
Ground	GND	197	198	BDQ7	Data line B7
Data line B11	BDQ8	199	200	GND	Ground
Ground	GND	201	202	BDQ9	Data line B10
Data line B8	BDQ10	203	204	GND	Ground
Ground	GND	205	206	BDQ11	Data line B9
Data Strobe B1 -	BDQS#1	207	208	GND	Ground
Data Strobe B1 +	BDQS1	209	210	BDM1	Ground
Ground	GND	211	212	GND	Ground
Data line B13	BDQ12	213	214	BDQ13	Data line B15
Ground	GND	215	216	GND	Ground
Data line B14	BDQ14	217	218	BDQ15	Data line B12
Ground	GND	219	220	GND	Ground
Data line B17	BDQ16	221	222	BDQ17	Data line B16
Ground	GND	223	224	GND	Ground
Data line B19	BDQ18	225	226	BDQ19	Data line B21
Ground	GND	227	228	GND	Ground
Ground	BDM2	229	230	BDQS#2	Data Strobe B2 -
Ground	GND	231	232	BDQS2	Data Strobe B2 +
Data line B20	BDQ20	233	234	GND	Ground
Ground	GND	235	236	BDQ21	Data line B22
Data line B23	BDQ22	237	238	GND	Ground
Ground	GND	239	240	BDQ23	Data line B18
Data line B25	BDQ24	241	242	GND	Ground
Ground	GND	243	244	BDQ25	Data line B24
Data line B27	BDQ26	245	246	GND	Ground
Ground	GND	247	248	BDQ27	Data line B26
Data Strobe B3 -	BDQS#3	249	250	GND	Ground
Data Strobe B3 +	BDQS3	251	252	BDM3	Ground
Ground	GND	253	254	GND	Ground
Data line B28	BDQ28	255	256	BDQ29	Data line B30
Ground	GND	257	258	GND	Ground
Data line B31	BDQ30	259	260	BDQ31	Data line B29
Ground	GND	261	262	GND	Ground

6.9 Power supply (P1614/P1616)

The connection for the power supply is implemented as a 2x12-pin standard ATX socket ("ATX24"). This is supplemented by a 2x4-pin housing socket via which the CORE-IN voltage must be provided.

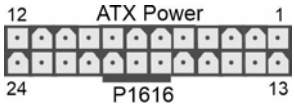


Fig. 10: CB1076 2x12-pin ATX Power

Pin assignment 2x12-pin socket ATX-Power					
Description	**Name**	**Pin**		**Name**	**Description**
Supply voltage 3.3 V	3.3 V	1	13	3.3 V	Supply voltage 3.3 V
Supply voltage 3.3 V	3.3 V	2	14	-12 V	Supply voltage -12 V
Ground	GND	3	15	GND	Ground
Supply voltage 5 V	VCC	4	16	PS_ON	On/Off signal
Ground	GND	5	17	GND	Ground
Supply voltage 5 V	VCC	6	18	GND	Ground
Ground	GND	7	19	GND	Ground
ATX Powergood	PWR_ON	8	20	-5 V	Supply voltage -5 V
Standby 5 V	SVCC	9	21	VCC	Supply voltage 5 V
Supply voltage 12 V	12 V	10	22	VCC	Supply voltage 5 V
Supply voltage 12 V	12 V	11	23	VCC	Supply voltage 5 V
Supply voltage 3.3 V	3.3 V	12	24	GND	Ground

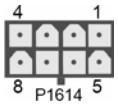


Fig. 11: CB1076 2x4-pin MiniFit

Pin assignment 2x4-in socket MiniFit					
Description	**Name**	**Pin**		**Name**	**Description**
Ground	GND	1	5	COREIN	Supply voltage 12 V
Ground	GND	2	6	COREIN	Supply voltage 12 V
Ground	GND	3	7	COREIN	Supply voltage 12 V
Ground	GND	4	8	COREIN	Supply voltage 12 V

6.10 SATA (P1603 – P1608)

Six SATA sockets are available for the connection of SATA devices. All SATA channels support the speed modes 1.5 Gbit/s, 3 Gbit/s and 6 Gbit/s.

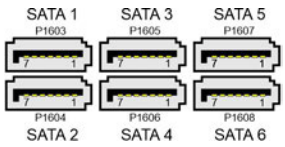


Fig. 12: CB1076 SATA sockets

Pin assignment SATA sockets		
Pin	**Name**	**Description**
1	GND	Ground
2	SATATX	SATA Transmit +
3	SATATX#	SATA Transmit -
4	GND	Ground
5	SATARX#	SATA Receive -
6	SATARX	SATA Receive +
7	GND	Ground

6.11 System Port (P1610)

The board has a 2x13-pin standard pin contact strip for piercing connection with a spacing of 2.54 mm, via which the signals for power button, speaker, reset and various status LEDs are provided. This connector is coded for Beckhoff.

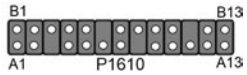


Fig. 13: CB1076 System Port

Pin assignment connector system 1					
Description	**Name**	**Pin**		**Name**	**Description**
On/Suspend button	PWRBTN#	A1	B1	GND	Ground
Ground	SVCC	A2	B2	N/C	Not connected
Not available	N/C	A3	B3	PWLED#	Power LED
Ground	GND	A4	B4	N/C	Not connected
Supply voltage 5 V	VCC	A5	B5	PWLED	Supply voltage 3.3 V
Hard disk LED	HDLED#	A6	B6	N/C	Not available
Supply voltage 5 V	VCC	A7	B7	VCC	Supply voltage 5 V
Not available	N/C	A8	B8	GND	Ground
Not connected	N/C	A9	B9	N/C	Not connected
Ground	GND	A10	B10	BEEP	Speaker
Not connected	N/C	A11	B11	N/C	Not available
Not connected	N/C	A12	B12	GND	Ground
Supply voltage 5 V	VCC	A13	B13	RESET#	Reset

System Port 2

The board is prepared for an additional 2x9-pin System Port (P1612) and can be fitted with it.

6.12 M.2 Key-M (P1700)

The CB1076 is equipped with an M.2 Key-M socket. SATA and PCIe signals are led out via these sockets. SATA SSD and SATA NVME cards (M.2-2280) can be operated. SATA RAID 0, 1, 5 and 10 are supported. Adapter cards with standard connectors are available as accessories. Please contact your distributor for this.

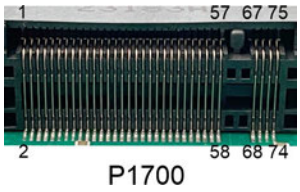


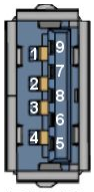
Fig. 14: CB1076 M.2M P1700

Pin assignment M.2 Key-M (P1700):					
Description	**Signal**	**Pin**		**Signal**	**Description**
Ground	GND	1	2	3.3 V1	Standby Supply voltage S3.3 V
Ground	GND	3	4	3.3 V2	Standby Supply voltage S3.3 V
PCIe Lane 3 Receive -	PER3#	5	6	N/C	(not led out)
PCIe Lane 3 Receive +	PER3	7	8	N/C	(not led out)
Ground	GND	9	10	GPIO9 DAS DDS LED1	NVMELED-
PCIe Lane 3 Transmit -	PET3#	11	12	3.3 V3	Standby Supply voltage S3.3 V
PCIe Lane 3 Transmit +	PET3	13	14	3.3 V4	Standby Supply voltage S3.3 V
Ground	GND	15	16	3.3 V5	Standby Supply voltage S3.3 V
PCIe Lane 2 Receive -	PER2#	17	18	3.3 V6	Standby Supply voltage S3.3 V
PCIe Lane 2 Receive +	PER2	19	20	N/C	(not led out)
Ground	GND	21	22	N/C	(not led out)
PCIe Lane 2 Transmit -	PET2#	23	24	N/C	(not led out)
PCIe Lane 2 Transmit +	PET2	25	26	N/C	(not led out)
Ground	GND	27	28	N/C	(not led out)
PCIe Lane 1 Receive -	PER1#	29	30	N/C	(not led out)
PCIe Lane 1 Receive	PER1	31	32	N/C	(not led out)
Ground	GND	33	34	N/C	(not led out)
PCIe Lane 1 Transmit -	PET1#	35	36	N/C	(not led out)
PCIe Lane 1 Transmit +	PET1	37	38	DEVSLP	(not led out)
Ground	GND	39	40	N/C	(not led out)
PCIe Lane 0 Receive +	PER0# SATAB	41	42	N/C	(not led out)
PCIe Lane 0 Receive -	PER0 SATAB#	43	44	N/C	(not led out)
Ground	GND	45	46	N/C	(not led out)
PCIe Lane 0 Transmit -	PET0# SATAA#	47	48	N/C	(not led out)
PCIe Lane 0 Transmit +	PET0 SATAA	49	50	PRST#	PCIe Reset active low

Pin assignment M.2 Key-M (P1700):					
Description	**Signal**	**Pin**		**Signal**	**Description**
Ground	GND	51	52	CLKREQ#	PCIe Clock Enable active low
PCIe Lane Reference Clock -	REFCLK#	53	54	PEWAKE#	Link Reactivation active low
PCIe Lane Reference Clock +	REFCLK	55	56	N/C	(not led out)
Ground	GND	57	58	N/C	(not led out)
(not led out)	N/C	59	60	N/C	(not led out)
(not led out)	N/C	61	62	N/C	(not led out)
(not led out)	N/C	63	64	N/C	(not led out)
(not led out)	N/C	65	66	N/C	(not led out)
(not led out)	N/C	67	68	SUSCLK	System clock
Configuration pin	CFG_PCIe/ SATA	69	70	3.3 V	Standby Supply voltage S3.3 V
Ground	GND	71	72	3.3 V	Standby Supply voltage S3.3 V
Ground	GND	73	74	3.3 V	Standby Supply voltage S3.3 V
Ground	GND	75			

6.13 USB3.1 Gen2 Typ A (P1613)

USB3.0 is made available via this internal USB interface.



P1613

Fig. 15: CB 1076 USB 3.1 type A

Pin assignment internal USB 3.1 connector		
Pin	**Name**	**Description**
1	VCC	5 V for USB
2	USB-D#	Minus data channel USB
3	USB-D	Plus data channel USB
4	GND1	Ground
5	SSRX-	SuperSpeed Receiver -
6	SSRX+	SuperSpeed Receiver +
7	GND2	Ground
8	SSTX-	SuperSpeed Transmitter -
9	SSTX+	SuperSpeed Transmitter +

6.14 GPIO (P1615)

The board has a general purpose input/output interface that feeds the signals out via a 2x10-pin connector. By programming the associated chip (Super-IO) accordingly, I/O functions can be created here in a very flexible manner. Ask your distributor about appropriate software support.

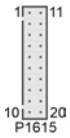


Fig. 16: CB1076 GPIO socket

Pin assignment GPIO connector					
Description	**Name**	**Pin**		**Name**	**Description**
Supply voltage 5 V	VCC	1	11	VCC	Supply voltage 5 V
GP Input/Output 0	GPIO0	2	12	N/C	Not connected
GP Input/Output 1	GPIO1	3	13	N/C	Not connected
GP Input/Output 2	GPIO2	4	14	N/C	Not connected
GP Input/Output 3	GPIO3	5	15	N/C	Not connected
GP Input/Output 4	GPIO4	6	16	N/C	Not connected
GP Input/Output 5	GPIO5	7	17	N/C	Not connected
GP Input/Output 6	GPIO6	8	18	N/C	Not connected
GP Input/Output 7	GPIO7	9	19	N/C	Not connected
Ground	GND	10	20	GND	Ground

6.15 SMB/I²C (P1600)

The module can communicate with other switching elements via the SMBus or I²C protocol. The connections for this are realized in a 2x5-pin socket. The SMBus signals are processed by the chipset, the I²C signals by the SIO chip.

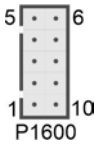


Fig. 17: CB1076 SMB-I2C socket

Pin assignment SMB/I²C connector					
Description	**Name**	**Pin**		**Name**	**Description**
Supply voltage 3.3 V	3.3 V	1	6	GND	Ground
SMBus Clock	SMBCLK	2	7	SMBDAT	SMBus Data
SMBus Alarm	SMBALERT#	3	8	SVCC	Standby supply 5 V
I²C-Bus Clock	I2CLK	4	9	I2DAT	I²C-Bus Data
Supply voltage 5 V	VCC	5	10	GND	Ground

6.16 PCIe x4 (P1205/P1206/P1204/P1201)

Four PCI-Express x4 expansion card slots are available on the CB1076 board. x1 expansion cards can also be operated in these slots.

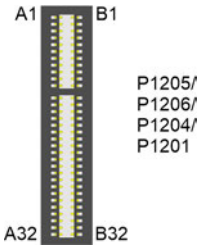


Fig. 18: CB1076 PCIe x4 socket

Pin assignment PCI-Express x4 socket					
Description	**Name**	**Pin**		**Name**	**Description**
Hot Plug Detect 1	PRSNT1	A1	B1	12 V	Supply voltage 12 V
Supply voltage 12 V	12 V	A2	B2	12 V	Supply voltage 12 V
Supply voltage 12 V	12 V	A3	B3	RSVD	Not connected
Ground	GND	A4	B4	GND	Ground
Not connected	TCK	A5	B5	SMBCLK	SMBus Clock PCIe
Not connected	TDI	A6	B6	SMBDAT	SMBus Data PCIe
Not connected	TDO	A7	B7	GND	Ground
Not connected	TMS	A8	B8	3.3 V	Supply voltage 3.3 V
Supply voltage 3.3 V	3.3 V	A9	B9	TRST	Not connected
Supply voltage 3.3 V	3.3 V	A10	B10	S3.3V	Standby voltage 3.3 V
PCIe Reset -	PERST#	A11	B11	WAKE#	Link Reactivation -
Ground	GND	A12	B12	RSVD	Not connected
Reference Clock +	REFCLK	A13	B13	GND	Ground
Reference Clock -	REFCLK#	A14	B14	PET0	Transmit Lane 0 +
Ground	GND	A15	B15	PET0#	Transmit Lane 0 -
Receive Lane 0 +	PER0	A16	B16	GND	Ground
Receive Lane 0 -	PER0#	A17	B17	PRSNT2#	PCIe Clock Enable -
Ground	GND	A18	B18	GND	Ground
Not connected	RSVD	A19	B19	PET1	Transmit Lane 1 +
Ground	GND	A20	B20	PET1#	Transmit Lane 1 -
Receive Lane 1 +	PER1	A21	B21	GND	Ground
Receive Lane 1 -	PER1#	A22	B22	GND	Ground
Ground	GND	A23	B23	PET2	Transmit Lane 2 +
Ground	GND	A24	B24	PET2#	Transmit Lane 2 -
Receive Lane 2 +	PER2	A25	B25	GND	Ground
Receive Lane 2 -	PER2#	A26	B26	GND	Ground
Ground	GND	A27	B27	PET3	Transmit Lane 3 +
Ground	GND	A28	B28	PET3#	Transmit Lane 3 -
Receive Lane 3 +	PER3	A29	B29	GND	Ground
Receive Lane 3 -	PER3#	A30	B30	RSVD	Not connected
Ground	GND	A31	B31	PRSNT2#	Hot Plug Detect 1
Not connected	RSVD	A32	B32	GND	Ground

6.17 PCIe x1 (P1200/P1203)

Two PCI-Express x1 expansion card slots are available on the CB1076 board.

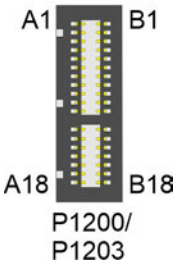


Fig. 19: CB1076 PCIe x1 socket

NOTICE

Observe pin assignment

In the pin assignment table below, note that for certain signals there are necessary differences between the different PCIe-x1 connectors on the board. This applies to the clock signals (A13, A14), the receive signals (A16, A17) and the transmit signals (B14, B15).

Pin assignment PCI-Express x1 socket

Description	Name	Pin		Name	Description
Hot Plug Detect 1	PRSNT1#	A1	B1	12 V	Supply voltage 12 V
Supply voltage 12 V	12 V	A2	B2	12 V	Supply voltage 12 V
Supply voltage 12 V	12 V	A3	B3	RSVD	Not connected t
Ground	GND	A4	B4	GND	Ground
Not connected	TCK	A5	B5	SMBCLK	SMBus Clock PCIe
Not connected	TDI	A6	B6	SMBDAT	SMBus Data PCIe
Not connected	TDO	A7	B7	GND	Ground
Not connected	TMS	A8	B8	3.3 V	Supply voltage 3.3 V
Supply voltage 3.3 V	3.3 V	A9	B9	TRST	Not connected
Supply voltage 3.3 V	3.3 V	A10	B10	S3.3V	Standby voltage 3.3 V
PCIe Reset -	PERST#	A11	B11	PEWAKE#	Link Reactivation
Ground	GND	A12	B12	RSVD	Not connected
Reference Clock +	REFCLK	A13	B13	GND	Ground
Reference Clock -	REFCLK#	A14	B14	PET0	Transmit Lane 0 +
Ground	GND	A15	B15	PET0#	Transmit Lane 0 -
Receive Lane 0 +	PER0	A16	B16	GND	Ground
Receive Lane 0 -	PER0#	A17	B17	PRSNT2#	Hot Plug Detect 1
Ground	GND	A18	B18	GND	Ground

6.18 PCIe x16 (P1202)

A slot for a PCIe x16 card is available on the CB1076 board. PCIe x16 graphics cards, x1 or x4 expansion cards can be used in this slot.

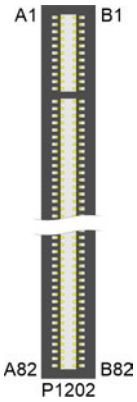


Fig. 20: CB1076 PCIe x16 socket

Pin assignment PCI-Express x16 socket					
Description	**Name**	**Pin**		**Name**	**Description**
Hot Plug Detect 1 -	PRSNT1#	A1	B1	12 V	Supply voltage 12 V
Supply voltage 12 V	12 V	A2	B2	12 V	Supply voltage 12 V
Supply voltage 12 V	12 V	A3	B3	RSVD	Reserved
Ground	GND	A4	B4	GND	Ground
Test Clock	TCK	A5	B5	SMBCLK	SMBus Clock PCIe
Not connected	TDI	A6	B6	SMBDAT	SMBus Data PCIe
Not connected	TDO	A7	B7	GND	Ground
Not connected	TMS	A8	B8	3.3 V	Supply voltage 3.3 V
Supply voltage 3.3 V	3.3 V	A9	B9	TRST	Not connected
Supply voltage 3.3 V	3.3 V	A10	B10	S3.3V	Standby voltage 3.3 V
PCIe Reset	PERST#	A11	B11	WAKE#	Link Reactivation -
Ground	GND	A12	B12	RSVD	Not connected
Reference Clock +	REFCLK	A13	B13	GND	Ground
Reference Clock -	REFCLK#	A14	B14	PET0	Transmit Lane 0 +
Ground	GND	A15	B15	PET0#	Transmit Lane 0 -
Receive Lane 0 +	PER0	A16	B16	GND	Ground
Receive Lane 0 -	PER0#	A17	B17	PRSNT2#	Hot Plug Detect 2 -
Ground	GND	A18	B18	GND	Ground
Not connected	RSVD	A19	B19	PET1	Transmit Lane 1 +
Ground	GND	A20	B20	PET1#	Transmit Lane 1 -
Receive Lane 1 +	PER1	A21	B21	GND	Ground
Receive Lane 1 -	PER1#	A22	B22	GND	Ground
Ground	GND	A23	B23	PET2	Transmit Lane 2 +
Ground	GND	A24	B24	PET2#	Transmit Lane 2 -
Receive Lane 2 +	PER2	A25	B25	GND	Ground
Receive Lane 2 -	PER2#	A26	B26	GND	Ground
Ground	GND	A27	B27	PET3	Transmit Lane 3 +
Ground	GND	A28	B28	PET3#	Transmit Lane 3 -
Receive Lane 3 +	PER3	A29	B29	GND	Ground
Receive Lane 3 -	PER3#	A30	B30	RSVD	Not connected
Ground	GND	A31	B31	PRSNT2#	Hot Plug Detect 2 -
Not connected	RSVD	A32	B32	GND	Ground
Not connected	RSVD	A33	B33	PET4	Transmit Lane 4 +
Ground	GND	A34	B34	PET4#	Transmit Lane 4 -
Receive Lane 4 +	PER4	A35	B35	GND	Ground
Receive Lane 4 -	PER4#	A36	B36	GND	Ground
Ground	GND	A37	B37	PET5	Transmit Lane 5 +
Ground	GND	A38	B38	PET5#	Transmit Lane 5 -
Receive Lane 5 +	PER5	A39	B39	GND	Ground
Receive Lane 5 -	PER5#	A40	B40	GND	Ground
Ground	GND	A41	B41	PET6	Transmit Lane 6 +
Ground	GND	A42	B42	PET6#	Transmit Lane 6 -
Receive Lane 6 +	PER6	A43	B43	GND	Ground
Receive Lane 6 -	PER6#	A44	B44	GND	Ground
Ground	GND	A45	B45	PET7	Transmit Lane 7 +
Ground	GND	A46	B46	PET7#	Transmit Lane 7 -
Receive Lane 7 +	PER7	A47	B47	GND	Ground

Pin assignment PCI-Express x16 socket					
Description	**Name**	**Pin**		**Name**	**Description**
Receive Lane 7 -	PER7#	A48	B48	PRSNT2#	Hot Plug Detect 2 -
Ground	GND	A49	B49	GND	Ground
Not connected	N/C	A50	B50	PET8	Transmit Lane 8 +
Ground	GND	A51	B51	PET8#	Transmit Lane 8 -
Receive Lane 8 +	PER8	A52	B52	GND	Ground
Receive Lane 8 -	PER8#	A53	B53	GND	Ground
Ground	GND	A54	B54	PET9	Transmit Lane 9 +
Ground	GND	A55	B55	PET9#	Transmit Lane 9 -
Receive Lane 9 +	PER9	A56	B56	GND	Ground
Receive Lane 9 -	PER9#	A57	B57	GND	Ground
Ground	GND	A58	B58	PET10	Transmit Lane 10 +
Ground	GND	A59	B59	PET10#	Transmit Lane 10 -
Receive Lane 10 +	PER10	A60	B60	GND	Ground
Receive Lane 10 -	PER10#	A61	B61	GND	Ground
Ground	GND	A62	B62	PET11	Transmit Lane 11 +
Ground	GND	A63	B63	PET11#	Transmit Lane 11 -
Receive Lane 11 +	PER11	A64	B64	GND	Ground
Receive Lane 11 -	PER11#	A65	B65	GND	Ground
Ground	GND	A66	B66	PET12	Transmit Lane 12 +
Ground	GND	A67	B67	PET12#	Transmit Lane 12 -
Receive Lane 12 +	PER12	A68	B68	GND	Ground
Receive Lane 12 -	PER12#	A69	B69	GND	Ground
Ground	GND	A70	B70	PET13	Transmit Lane 13 +
Ground	GND	A71	B71	PET13#	Transmit Lane 13 -
Receive Lane 13+	PER13	A72	B72	GND	Ground
Receive Lane 13-	PER13#	A73	B73	GND	Ground
Ground	GND	A74	B74	PET14	Transmit Lane 14 +
Ground	GND	A75	B75	PET14#	Transmit Lane 14 -
Receive Lane 14 +	PER14	A76	B76	GND	Ground
Receive Lane 14 -	PER14#	A77	B77	GND	Ground
Ground	GND	A78	B78	PET15	Transmit Lane 15 +
Ground	GND	A79	B79	PET15#	Transmit Lane 15 -
Receive Lane 15 +	PER15	A80	B80	GND	Ground
Receive Lane 15 -	PER15#	A81	B81	DDAT-PRSNT	Reserved
Ground	GND	A82	B82	RSVD	Not connected

6.19 LAN 2.5 Gbit and USB 3.1Gen2 (P1402/P1401/P1400)

The USB socket and LAN socket are implemented as combined sockets, each providing two USB ports and one LAN port. In this way, six USB channels and three LAN ports are led out with all board variants.

All USB channels support the 3.1 Gen2 specification.

All necessary settings for USB can be made by the BIOS. Note that the "USB Mouse and Keyboard" functionality of the BIOS setup is only required if the operating system does not provide USB support. Do not select this function for settings in the setup and for booting Windows with a connected USB mouse and keyboard, because this would result in significant performance limitations.

The individual USB interfaces can supply a current of up to 900 mA and are electronically protected.

You can connect 10BaseT, 100BaseT, 1000BaseT and 2500BaseT-compatible network components to the P1401 A and P1402 A LAN ports. The required speed is selected automatically. TSN, Auto-Cross and Auto-Negotiate are available as well as PXE and RPL functionality. Controller is Intel® i219 for Lan1 1Gbit with WOL (P1400 A) and i226 for LAN2 and 3, 2.5Gbit (P1401 A and P1402 A).

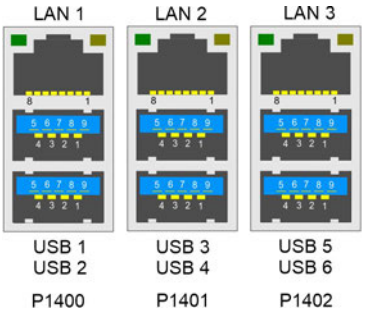


Fig. 21: CB1076 LAN USB socket

Pin assignment LAN socket i219 (P1400)		
Pin	**Name**	**Description**
1	LAN10	LAN line 1 +
2	LAN10#	LAN line 1 -
3	LAN11	LAN line 2 +
4	LAN11#	LAN line 2 -
5	LAN12	LAN line 3 +
6	LAN12#	LAN line 3 -
7	LAN13	LAN line 4 +
8	LAN13#	LAN line 4 -

Pin assignment LAN socket i226 (P1401/P1402)		
Pin	**Name**	**Description**
1	LAN20/30	LAN line 1 +
2	LAN20#/30#	LAN line 1 -
3	LAN21/31	LAN line 2 +
4	LAN21#/31#	LAN line 2 -
5	LAN22/32	LAN line 3 +
6	LAN22#/32	LAN line 3 -
7	LAN23//33	LAN line 4 +
8	LAN23#/33#	LAN line 4 -

Real-time applications

The Ethernet port connected via PCIe is usually suitable for cycle times <= 1 ms and for distributed clock applications with EtherCAT.
The Ethernet port integrated in the chipset is usually suitable for real-time Ethernet applications with cycle times > 1 ms (without distributed clocks).

Pin assignment USB3.1 Gen2 socket (P1400/P1401/P1402):		
Pin	**Signal**	**Description**
1	VCC	Supply voltage 5 V
2	D-	Data - (USB 3.1)
3	D+	Data + (USB 3.1)
4	GND	Ground
5	SSRX-	Receive line - (USB 3.1)
6	SSRX+	Receive line + (USB 3.1)
7	GND	Ground
8	SSTX-	Transmit line - (USB 3.1)
9	SSTX+	Transmit line + (USB 3.1)

6.20 DVI-D (P1500A/B)

The CB1076 has two DVI-D sockets in a combined component (Foxconn QH11121-DBDF-4F). You can connect digital DVI or HDMI displays to both sockets. Analog signals are not available on this connector. The CPU graphics support a maximum of three independent displays.

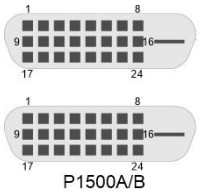


Fig. 22: CB1076 DVI-D socket

Pin assignment DVI-D:		
Pin	**Name**	**Description**
1	TMDSDAT2#	DVI data 2 -
2	TMDSDAT2	DVI data 2 +
3	GND	Ground
4	N/C	Reserved
5	N/C	Reserved
6	DDC CLK	DDC Clock (DVI/VGA)
7	DDC DAT	DDC Data (DVI/VGA)
8	N/C	Reserved
9	TMDSDAT1#	DVI data 1 -
10	TMDSDAT1	DVI data 1 +
11	GND	Ground
12	N/C	Reserved
13	N/C	Reserved
14	VCC	Supply voltage 5 V
15	GND	Ground
16	HP_DETECT	Hot Plug Detect
17	TMDSDAT0#	DVI data 0 -
18	TMDSDAT0	DVI data 0 +
19	GND	Ground
20	N/C	Reserved
21	N/C	Reserved
22	GND	Ground
23	TMDS CLK	DVI-Clock
24	TMDS CLK#	DVI-Clock

6.21 Serial interface COM1 (P1403)

The serial interface COM1 is led out via a 9-pin standard DSUB socket. The signals correspond to the RS232 standard.

You can set the port address and the interrupt used with the help of the BIOS setup.

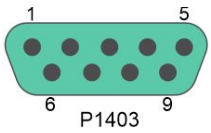


Fig. 23: CB1076 COM1 socket

Pin assignment COM1:					
Description	**Name**	**Pin**		**Name**	**Description**
Data Carrier Detect	DCD#	1	6	DSR#	Data Set Ready
Receive Data	RXD	2	7	RTS#	Request to Send
Transmit Data	TXD	3	8	CTS#	Clear to Send
Data Terminal Ready	DTR#	4	9	RI#	Ring Indicator
Ground	GND	5			

6.22 Display Port (P1501)

A corresponding standard socket
(Foxconn 3VC11203-D7AB-4H) is available for devices with a DisplayPort connection.

The interface additionally provides HDMI/DVI signals that can be used with aid of an adapter. Please consult your distributor with regard to a suitable adapter.

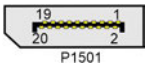


Fig. 24: CB1076 Display Port

Pin assignment Display Port					
Description	**Signal**	**Pin**		**Signal**	**Description**
Display Port Lane 0 +	L0	1	2	GND	Ground
Display Port Lane 0 -	L#0	3	4	L1	Display Port Lane 1 +
Ground	GND	5	6	L#1	Display Port Lane 1 -
Display Port Lane 2 +	L2	7	8	GND	Ground
Display Port Lane 2 -	L#2	9	10	L3	Display Port Lane 3 +
Ground	GND	11	12	L#3	Display Port Lane 3 -
DP / HDMI -	HDMI#	13	14	GND	Ground
Auxiliary plus	AUX	15	16	GND	Ground
Auxiliary minus	AUX#	17	18	HPD	Hot Plug Detect
Ground	GND	19	20	3.3 V	Supply voltage 3.3 V

7 BIOS

7.1 Using the setup

Within the individual setup pages the last saved settings can be restored can at any time with F2 ("Previous Values"). Use F3 ("Optimized Defaults") to load the factory defaults. Use F2/F3 to load the complete set of settings and F4 to save them (“Save & Reset”).

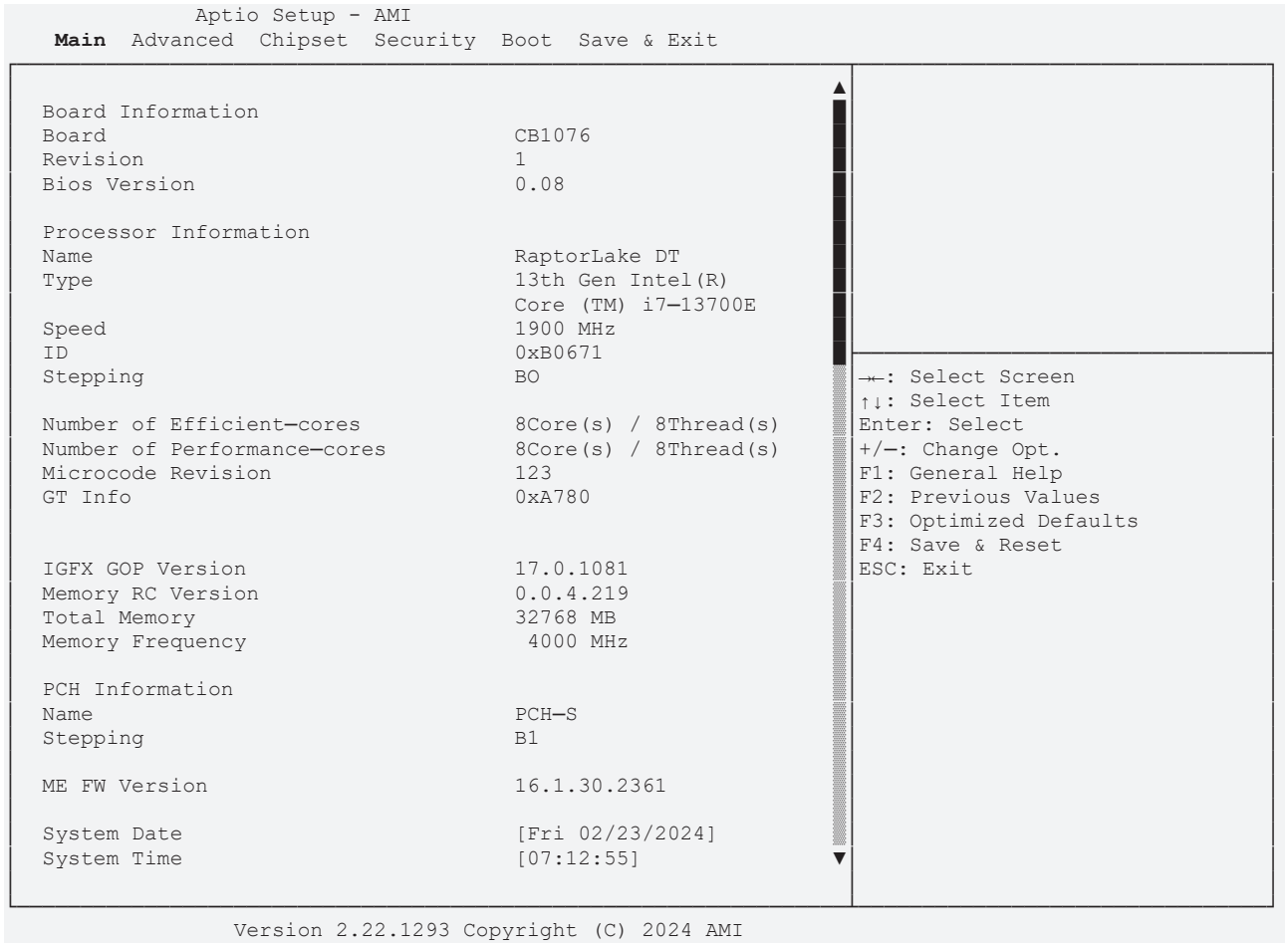
A "►" sign in front of the menu item indicates that a submenu is available. Use the arrow keys to navigate between menu items. Use the Enter key to select menu items and call submenus or selection dialogs.

For each setup option a help text is displayed at the top right, which in many cases contains useful information about the option and permitted values, etc.

Note on Setup Documentation

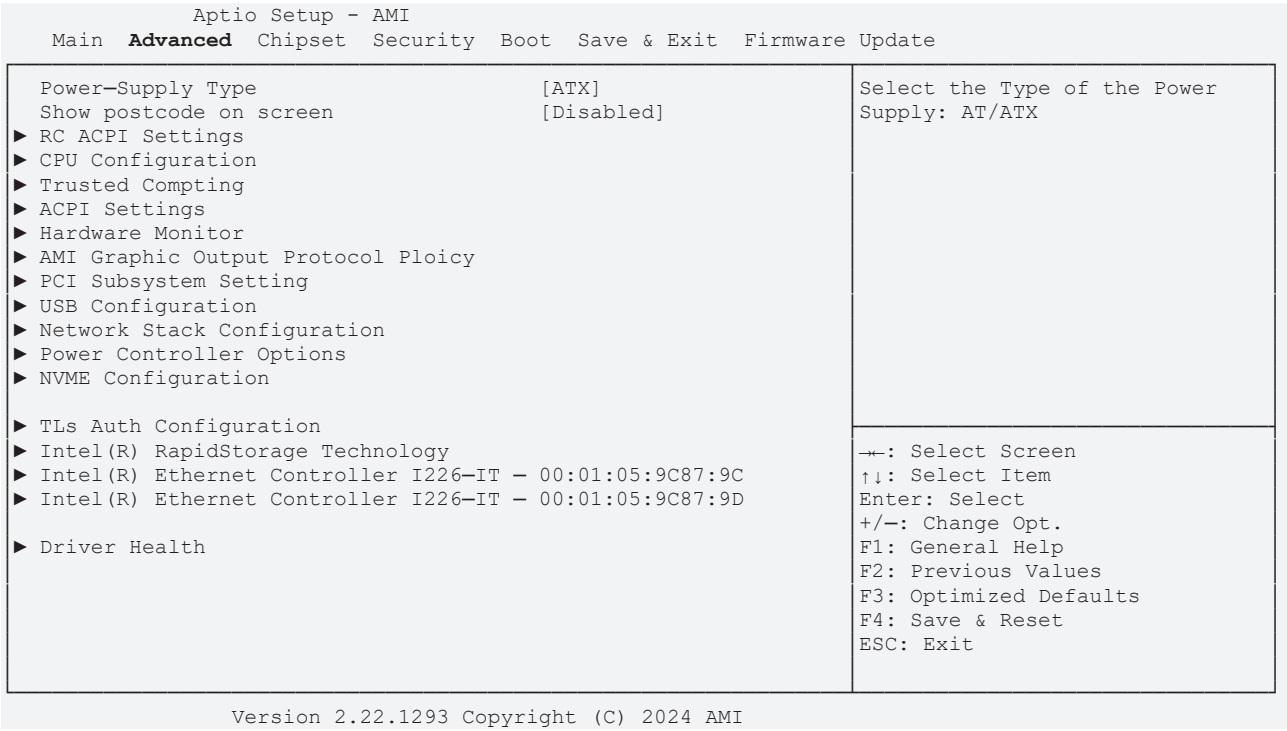
The BIOS is regularly updated so that the available setup options can change at any time without notice. This may result in differences between the options actually available and those described below. It should also be noted that the settings shown in the setup menus below are not necessarily the recommended or default settings. Which settings must be selected depends on the application scenario in which the board is operated.

7.2 Main


Aptio Setup - AMI
Main Advanced Chipset Security Boot Save & Exit
Board Information
Board CB1076
Revision 1
Bios Version 0.08
Processor Information
Name RaptorLake DT
Type 13th Gen Intel(R) Core (TM) i7—13700E
Speed 1900 MHz
ID 0xB0671
Stepping BO
Number of Efficient—cores 8Core(s) / 8Thread(s)
Number of Performance—cores 8Core(s) / 8Thread(s)
Microcode Revision 123
GT Info 0xA780
IGFX GOP Version 17.0.1081
Memory RC Version 0.0.4.219
Total Memory 32768 MB
Memory Frequency 4000 MHz
PCH Information
Name PCH—S
Stepping B1
ME FW Version 16.1.30.2361
System Date [Fri 02/23/2024]
System Time [07:12:55]
→←: Select Screen
↑↓: Select Item
Enter: Select
+/—: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Reset
ESC: Exit
Version 2.22.1293 Copyright (C) 2024 AMI

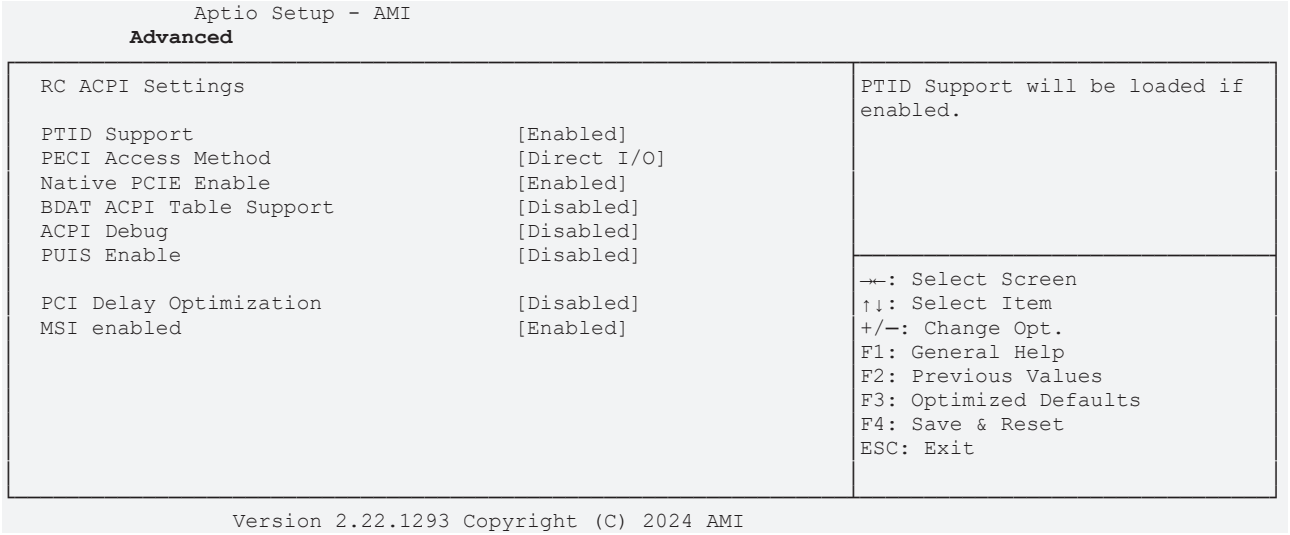
BIOS entry	Option
Board information	
Board	None
Revision	None
Bios Version	None
Processor Information	
Name	None
Type	None
Speed	None
ID	None
Stepping	None
Number of Efficient-cores	None
Number of Performance-cores	None
Microcode Revision	None
GT Info	None
IGFX GOP Version	None
Memory RC Version	None
Total Memory	None
Memory Frequency	None
PCH Information	
Name	None
Stepping	None
ME FW Version	None
System Date	Here you can change the system date.
System Time	Here you can change the system time.

7.3 Advanced Menu



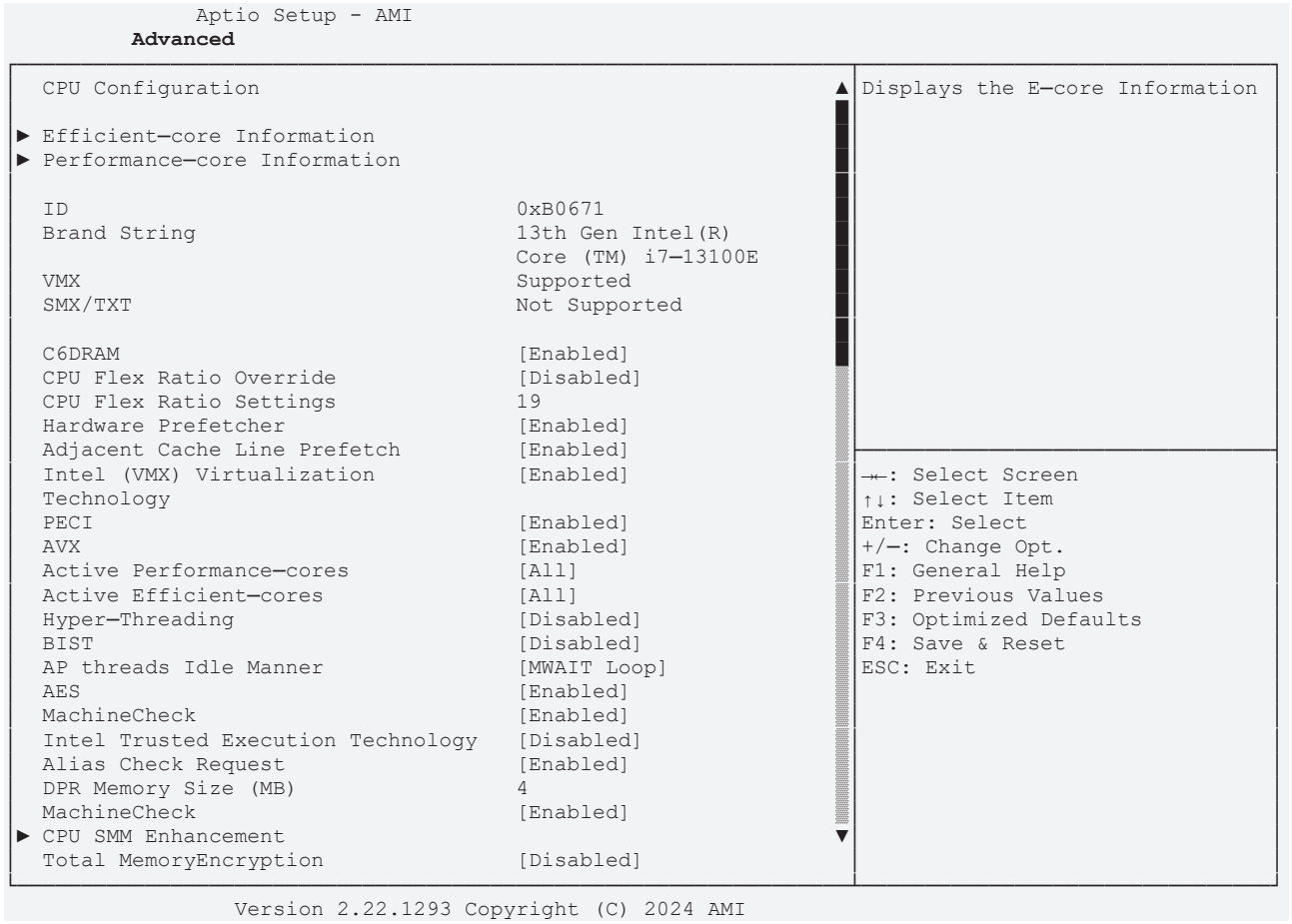
BIOS entry	Option
Power-Supply Type	ATX / AT
Show Postcode on screen	Disabled / Enabled
RC ACPI Settings	Submenu see: RC ACPI Settings [▶ 48]
CPU Configuration	Submenu see: CPU Configuration [▶ 49]
Trusted Computing	Submenu see: Trusted Computing [▶ 53]
ACPI Settings	Submenu see: ACPI Settings Disabled [▶ 54]
Hardware Monitor	Submenu see: Hardware Monitor [▶ 55]
AMI Graphic Output Protocol Policy	Submenu see: AMI Graphic Output Protocol Policy [▶ 56]
PCI Subsystem Settings	Submenu see: PCI Subsystem Settings [▶ 56]
USB Configuration	Submenu see: USB Configuration [▶ 57]
Network Stack Configuration	Submenu see: Network Stack Configuration enabled [▶ 58]
Power Controller Options	Submenu see: Power Controller Options [▶ 59]
NVMe Configuration	Submenu see: NVMe Configuration [▶ 60]
Tls Auth Configuration	Submenu see: TLs Auth Configuration [▶ 61]
Intel ® Rapid Storage Technology	Submenu see: Intel Rapid Storage Technology [▶ 63]
Intel® Ethernet Controller I226-IT – 00:01:05:9C:87:9C	Submenu see: Intel Ethernet Controller I226-IT [▶ 64]
Intel® Ethernet Controller I226-IT – 00:01:05:9C:87:9D	Submenu see: Intel Ethernet Controller I226-IT [▶ 65]
Driver Health	None

7.3.1 RC ACPI Settings



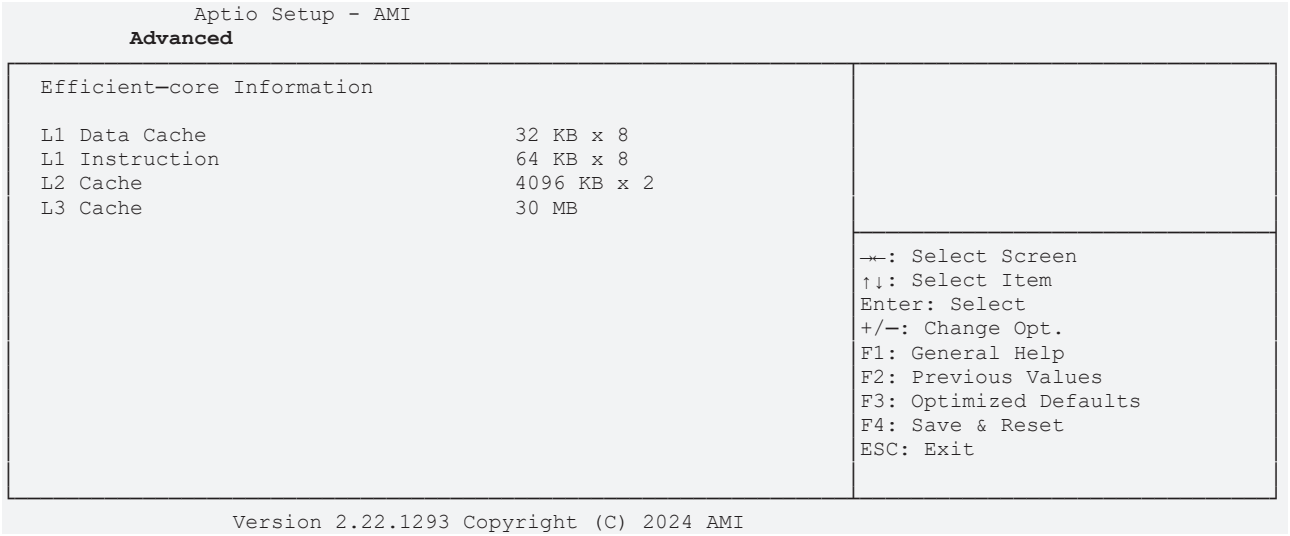
BIOS entry	Options
RC ACPI Settings	
PTID Support	Enabled / Disabled
PECI Access Method	Direct I/O / ACPI
Native PCIE Enable	Enabled / Disabled
BDAT ACPI Table Support	Disabled / Enabled
ACPI Debug	Disabled / Enabled
PUIS Enable	None
PCI Delay Optimization	Disabled / Enabled
MSI enabled	Enabled / Disabled

7.3.2 CPU Configuration



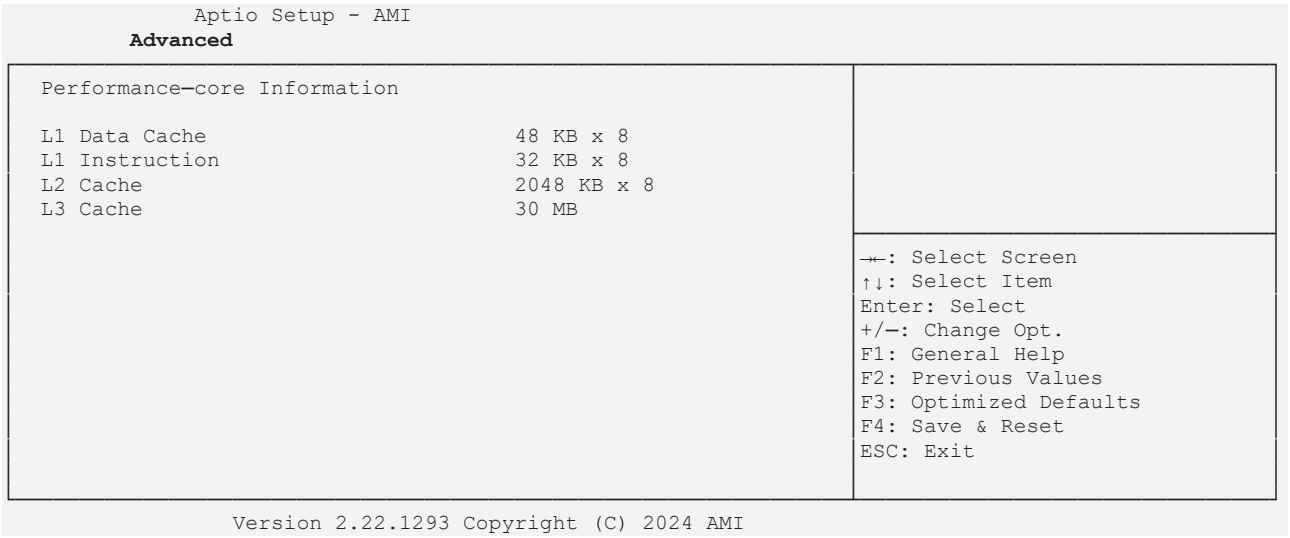
BIOS entry	Options
CPU Configuration	
Efficient-core Information	Submenu see:
Performance-core Information	Submenu see: Efficient-core Information [▶ 51]
ID	None
Brand String	None
VMX	None
SMX/TXT	None
C6DRAM	Enabled / Disabled
CPU Flex Ratio Override	Disabled / Enabled
CPU Flex Ratio Settings	None
Hardware Prefetcher	Enabled / Disabled
Adjacent Cache Line Prefetch	Enabled / Disabled
Intel (VMX) Virtualization Technology	Enabled / Disabled
PECI	Enabled / Disabled
AVX	Enabled / Disabled
Active Performance-cores	All / 1 / 2 / 3
Efficient Performance-cores	All / 1 / 2 / 3
Hyper-Threading	Disabled / Enabled
BIST	Disabled / Enabled
AP threads Idle Manner	MWAIT Loop / HALT Loop / Run Loop
AES	Enabled / Disabled
MachineCheck	Enabled / Disabled
Intel Trusted Execution Technology	Disabled / Enabled
Alias Check Request	Disabled / Enabled
DPR Memory Size (MB)	None
Reset Aux Comment	None
CPU SMM Enhancement	Submenu see: CPU SMM Enhancement [▶ 52]
Total Memory Encryption	Disabled / Enabled

7.3.2.1 Efficient-core Information



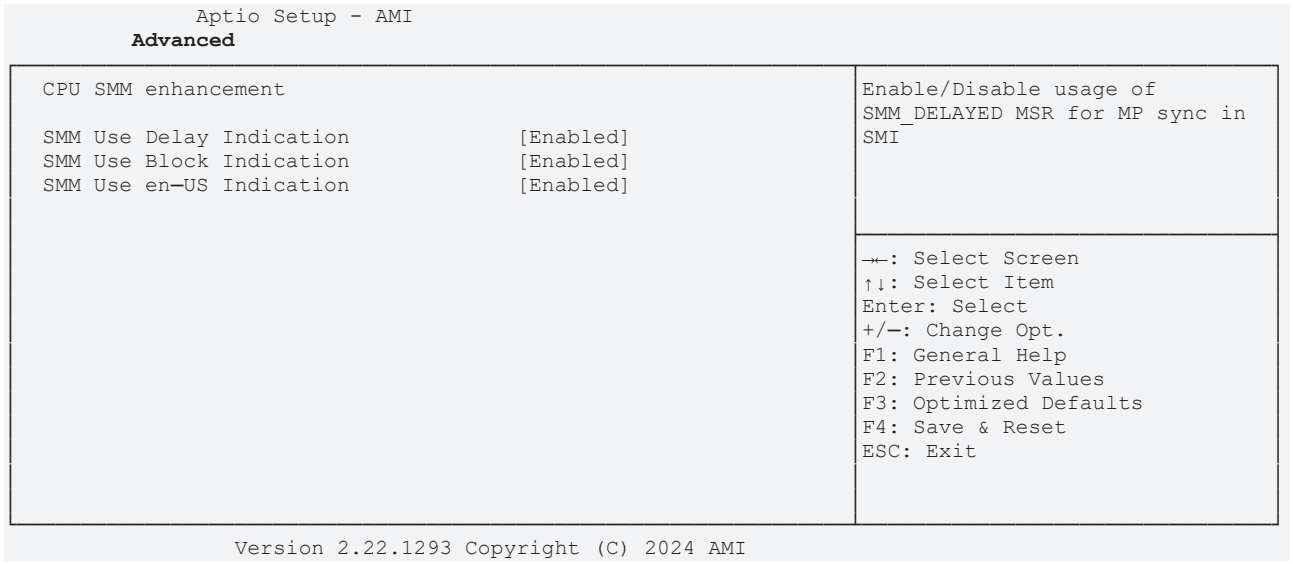
BIOS entry	Options
Efficient-core Information	
L1 Data Cache	None
L1 Instruction	None
L2 Cache	None
L3 Cache	None

7.3.2.2 Performance-core Information



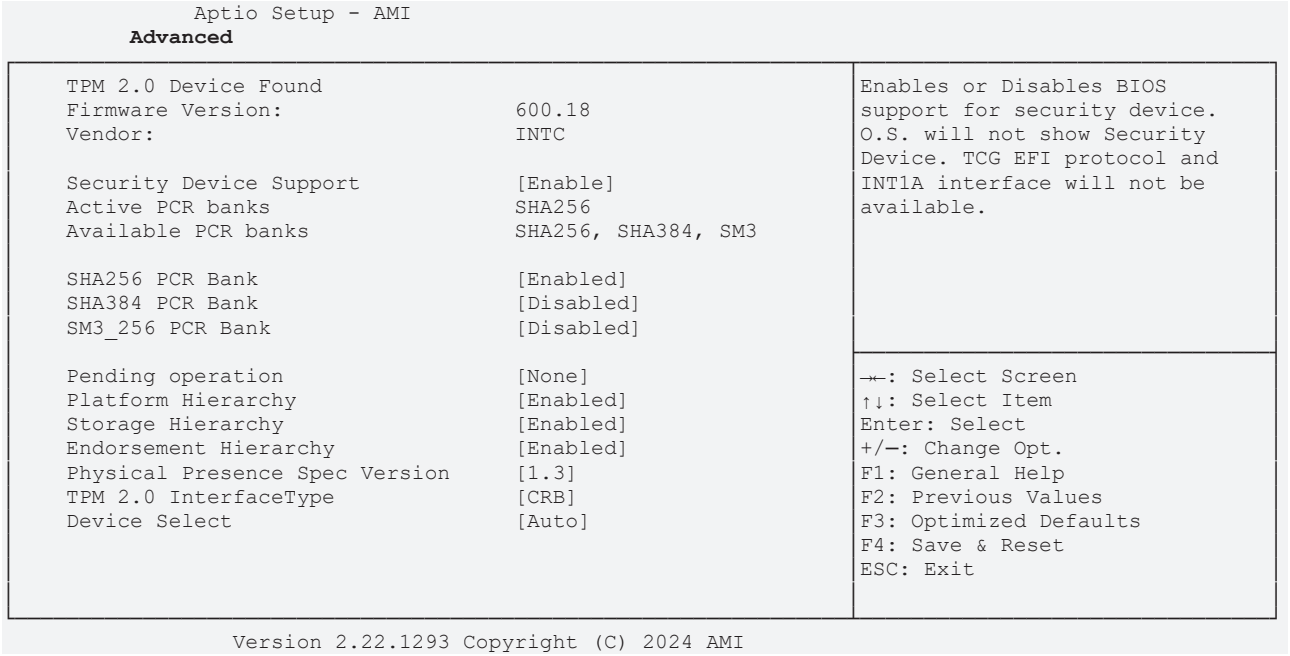
BIOS entry	Options
Performance-core Information	
L1 Data Cache	None
L1 Instruction	None
L2 Cache	None
L3 Cache	None

7.3.2.3 CPU SMM Enhancement



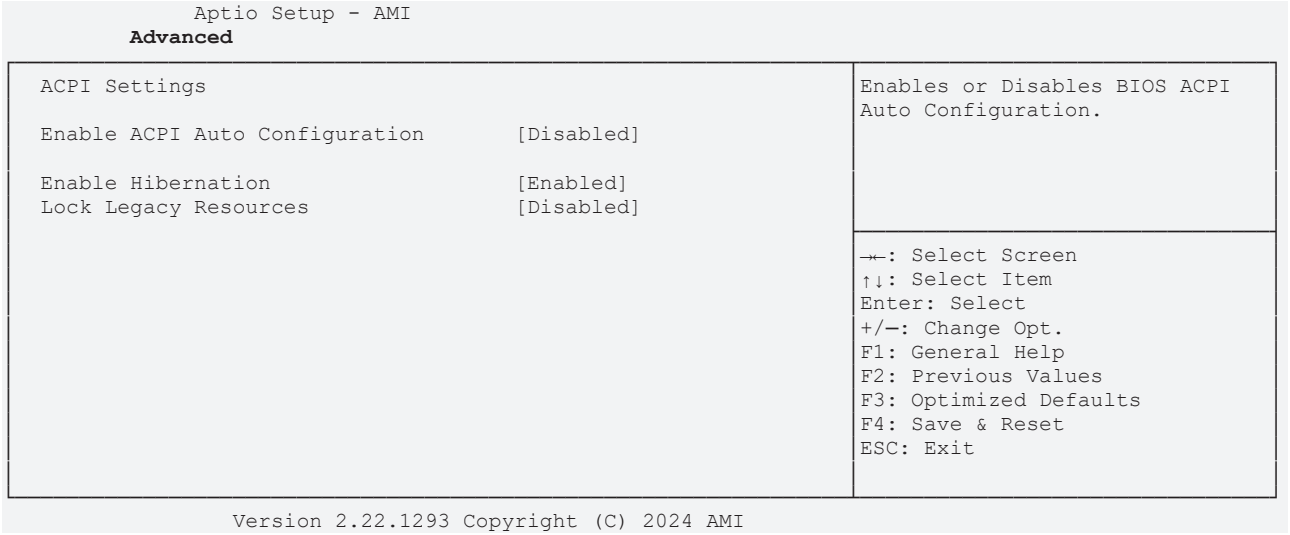
BIOS entry	Options
CPU SMM Enhancement	
SMM Use Delay Indication	Enabled / Disabled
SMM Use Block Indication	Enabled / Disabled
SMM Use en-US Indication	Enabled / Disabled

7.3.3 Trusted Computing



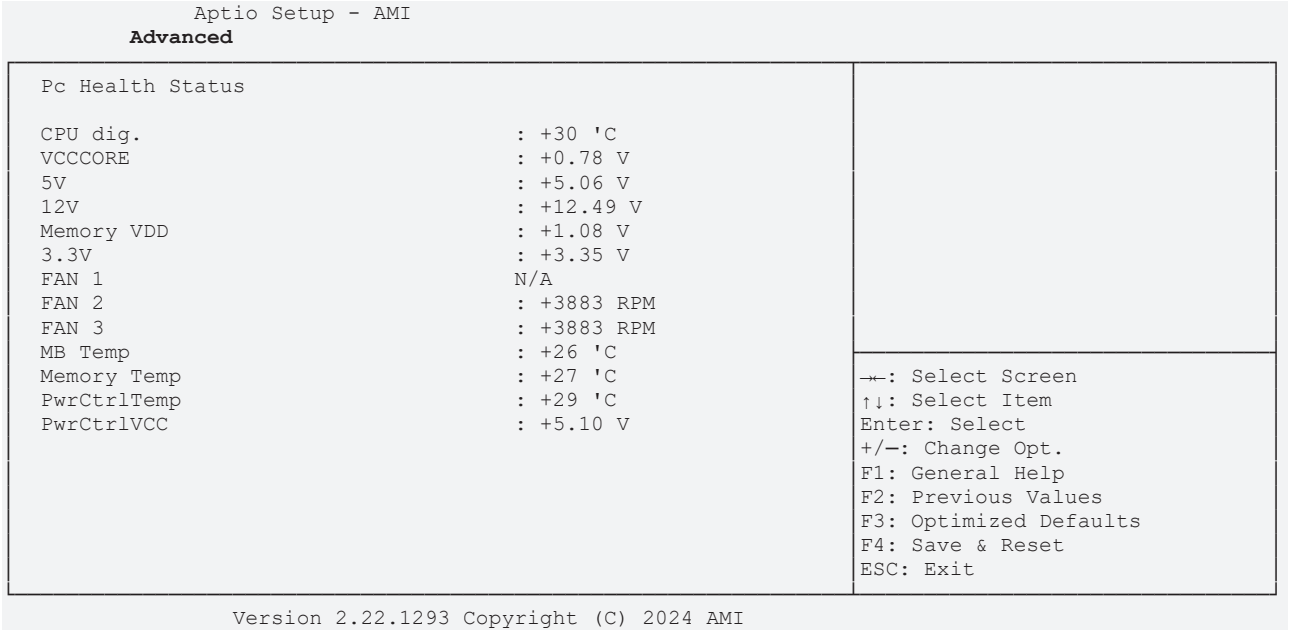
BIOS entry	Options
TPM 2.0 Device Found	
Firmware Version: 600.18	None
Vendor: INTC	None
Security Device Support	Enable / Disable
Active PCR banks	None
Available PCR banks	None
SHA256 PCR Bank	Enabled / Disabled
SHA384 PCR Bank	Disabled / Enabled
SM3_256 PCR Bank	Disabled / Enabled
Pending operation	None / TPM Clear
Platform Hierarchy	Enabled / Disabled
Storage Hierarchy	Enabled / Disabled
Endorsement Hierarchy	Enabled / Disabled
Physical Presence Spec Version	1.3 / 1.2
TPM 2.0 InterfaceType	None
Device Select	Auto / TPM 1.2 / TPM 2.0

7.3.4 ACPI Settings Disabled



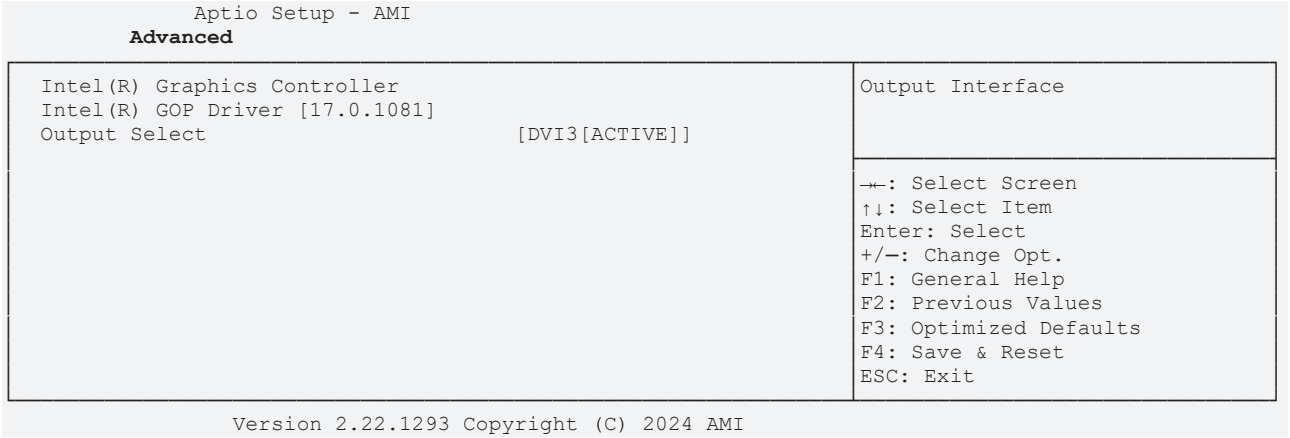
BIOS entry	Options
ACPI Settings	
Enable ACPI Auto Configuration	Disabled / Enabled
Enable Hibernation	Enabled / Disabled
Lock Legacy Resources	Disabled / Enabled

7.3.5 Hardware Monitor



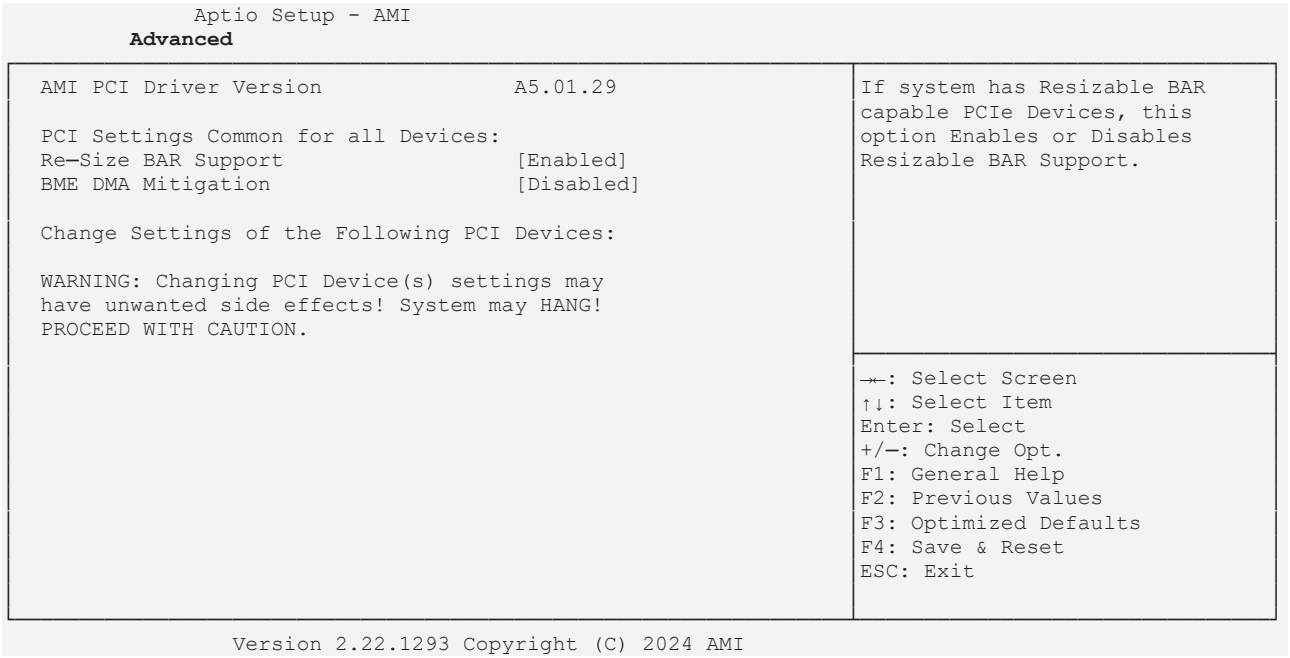
BIOS entry	Options
PC Health Status	
CPU dig.	None
VCCCORE	None
5 V	None
12 V	None
Memory VDD	None
3.3 V	None
FAN1	None
FAN 2	None
FAN 2	None
MB Temp	None
Memory Temp	None
PwrCtrlTemp	None
PwrCtrlVCC	None

7.3.6 AMI Graphic Output Protocol Policy



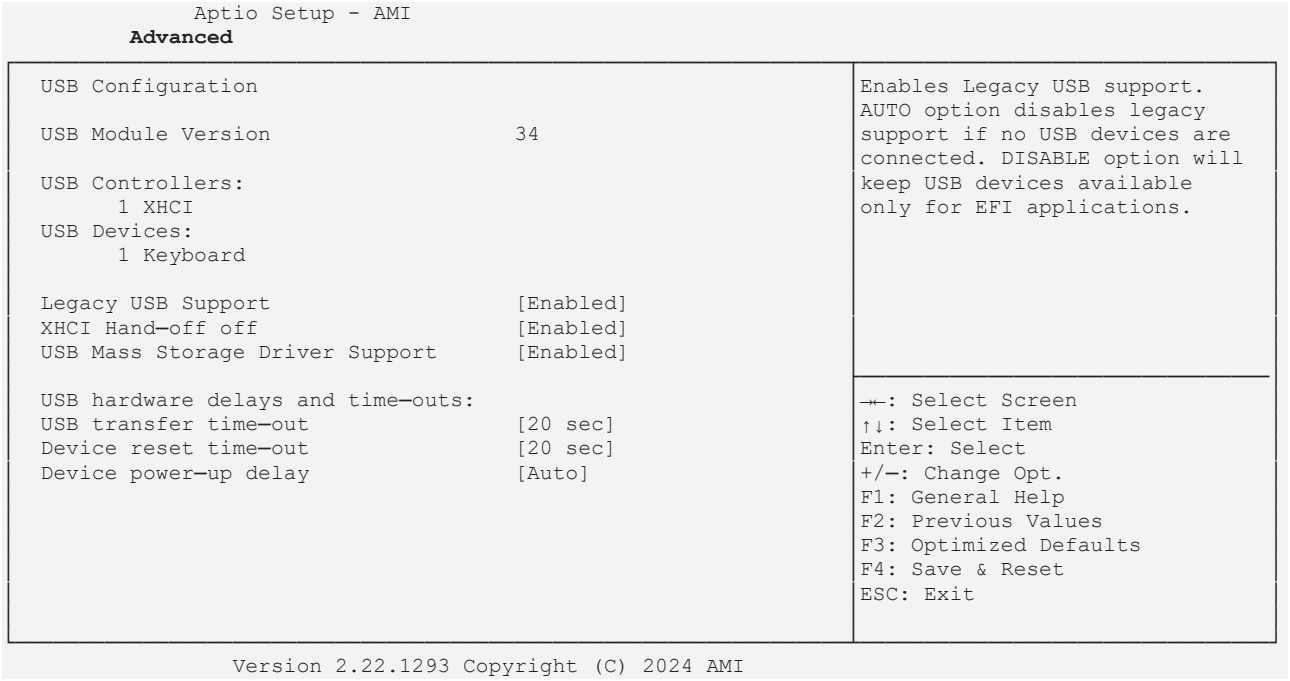
BIOS entry	Options
Intel® Graphics Controller Intel® GOP Driver [17.0.1081]	
Output Select	None

7.3.7 PCI Subsystem Settings



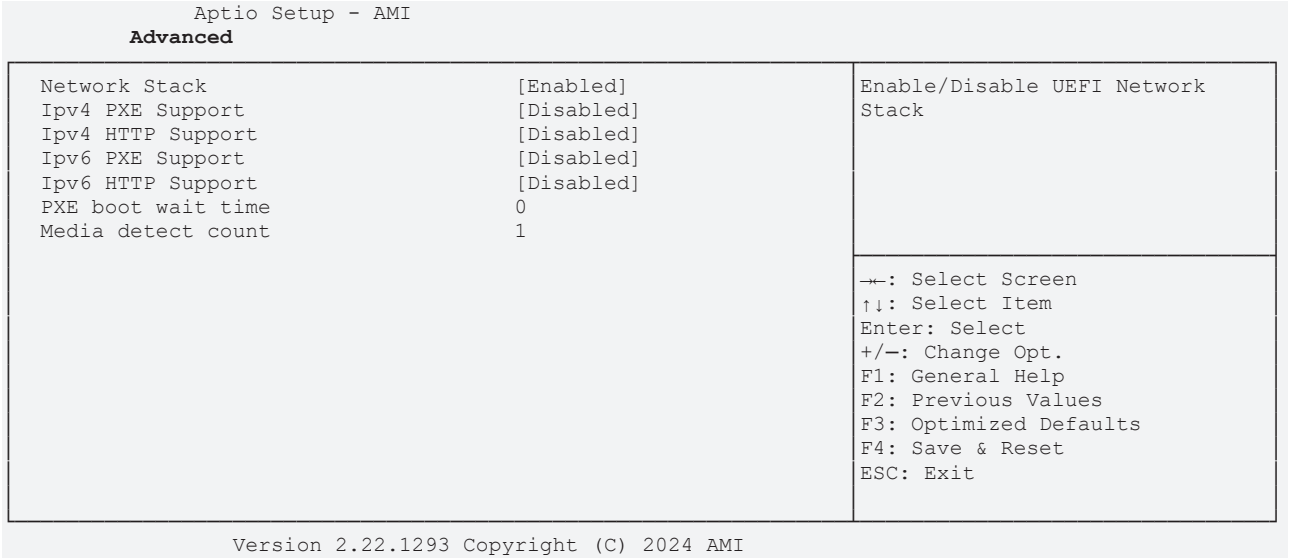
BIOS entry	Options
AMI PCI Bus Driver Version	None
PCI Device Common Settings:	
Re-Size BAR Support	Enabled / Disabled
BME DMA Mitigation	Disabled / Enabled

7.3.8 USB Configuration



BIOS entry	Options
USB Configuration	
USB Module Version	None
USB Controllers: 1XHCI	None
USB Devices: 1 Keyboard	None
Legacy USB Support	Enabled / Disabled / Auto
XHCI Hand-off	Enabled / Disabled
USB Mass Storage Driver Support	Enabled / Disabled
USB hardware delays and time-outs:	
USB transfer time-out	1 / 5 / 10 / 20 sec
Device reset time-out	10 / 20 / 30 / 40 sec
Device power-up delay	Auto / Manual

7.3.9 Network Stack Configuration enabled



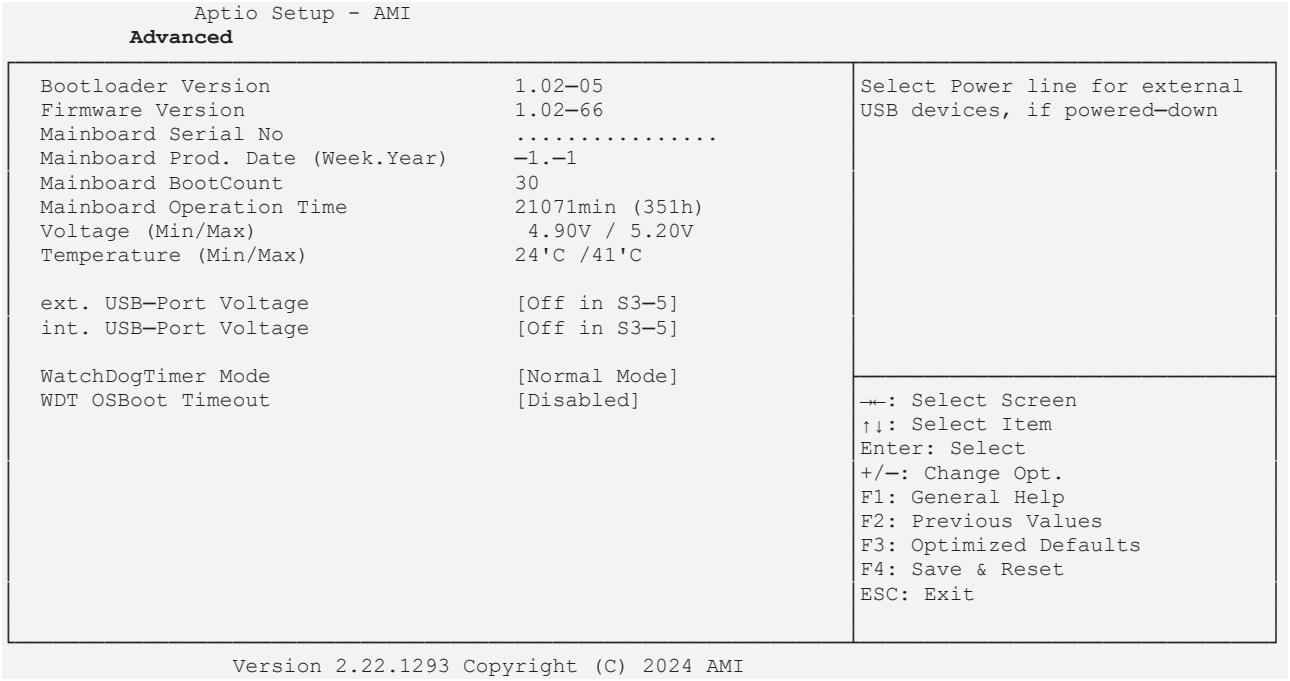
BIOS entry	Options
Network Stack	Disabled / Enabled
Ipv4 PXE Support	Disabled / Enabled
Ipv4 HTTP Support	Disabled / Enabled
Ipv6 PXE Support	Disabled / Enabled
Ipv6 HTTP Support	Disabled / Enabled
PXE boot wait time	None
Media detect count	None

NOTICE

PXE Boot available

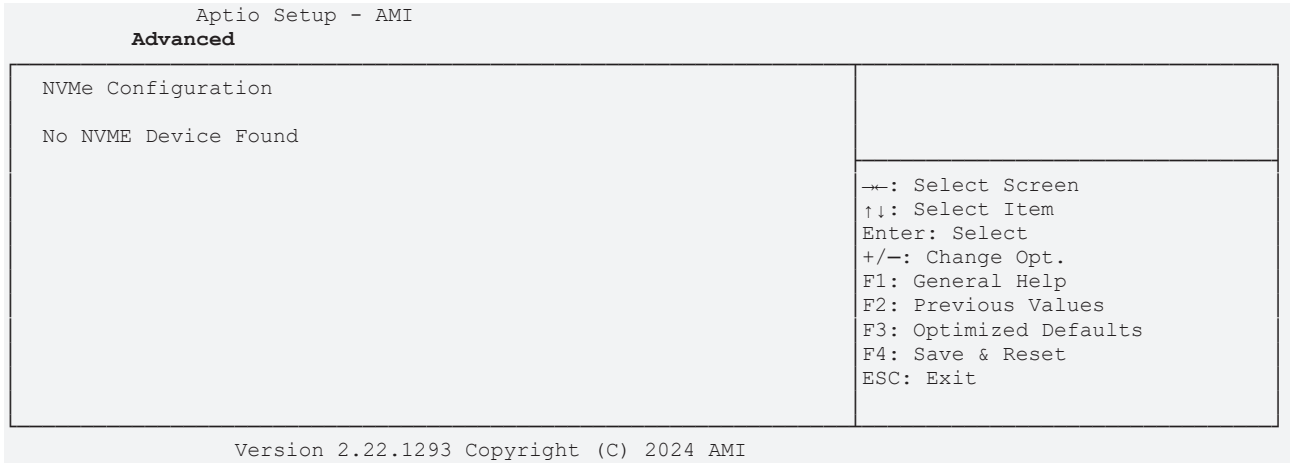
PXE Boot is available if you set Network Stack and Ipv4 PXE support to "Enable".

7.3.10 Power Controller Options



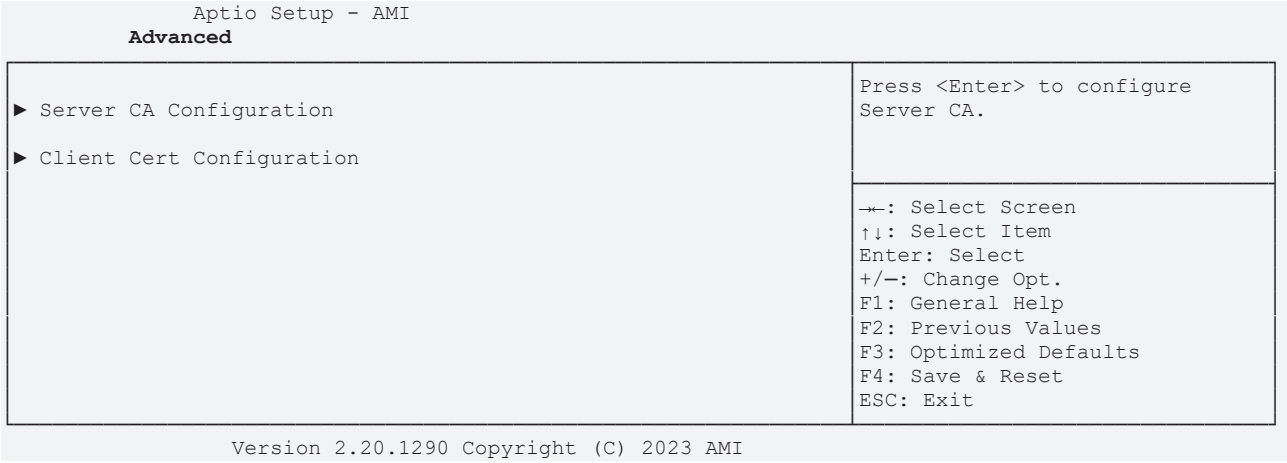
BIOS entry	Options
Bootloader Version	None
Firmaware Version	None
Mainboard Serial No	None
Mainboard Prod. Date (Week.Year)	None
Mainboard BootCount	None
Mainboard Operation Time	None
Voltage /Min/Max)	None
Temperature (Min/Max)	None
ext. USB-Port Voltage	Off in S3 - 5 / by SVCC
int. USB-Port Voltage	Off in S3 - 5 / by SVCC
WatchDogTimer Mode	Nomal Mode / Compatibility Mode
WDT OSBoot Timeout	Disabled / 45 / 60 / ... / 255 Seconds

7.3.11 NVMe Configuration



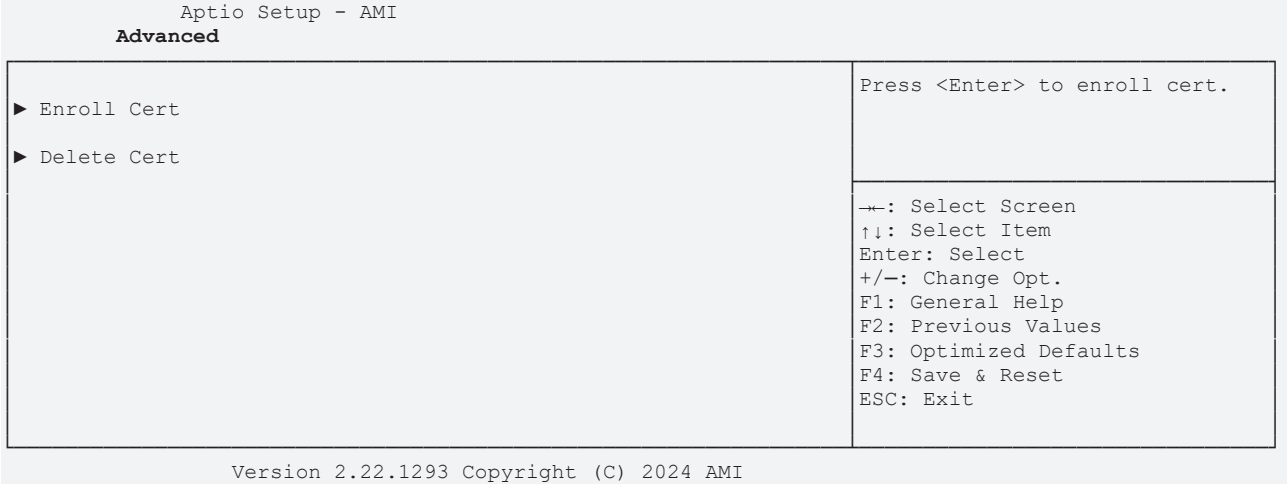
BIOS entry	Options
NVMe Configuration	
No NVME Device Found	None

7.3.12 TLs Auth Configuration



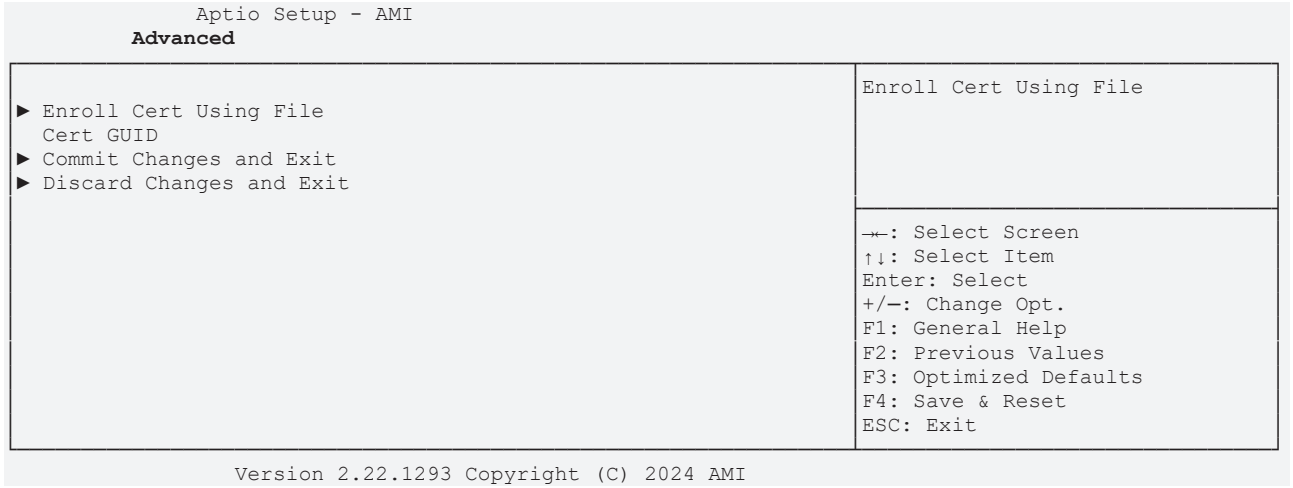
BIOS entry	Options
Server CA Configuration	Submenu see: Server CA Configuration [▶ 61]
Client Cert Configuration	None

7.3.12.1 Server CA Configuration



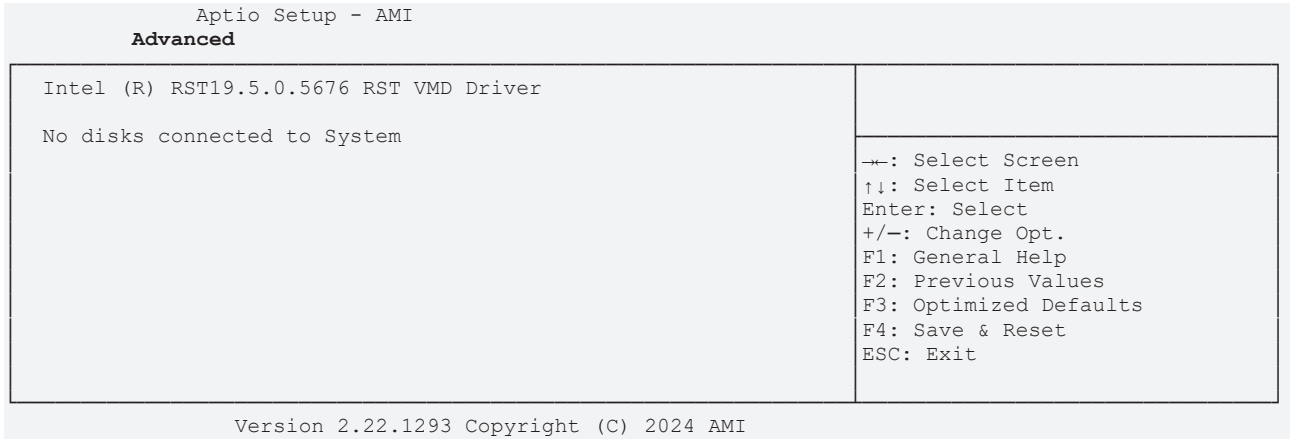
BIOS entry	Options
Enroll Cert	Submenu see: Enroll Cert [▶ 62]
Delete Cert	None

7.3.12.1.1 Enroll Cert



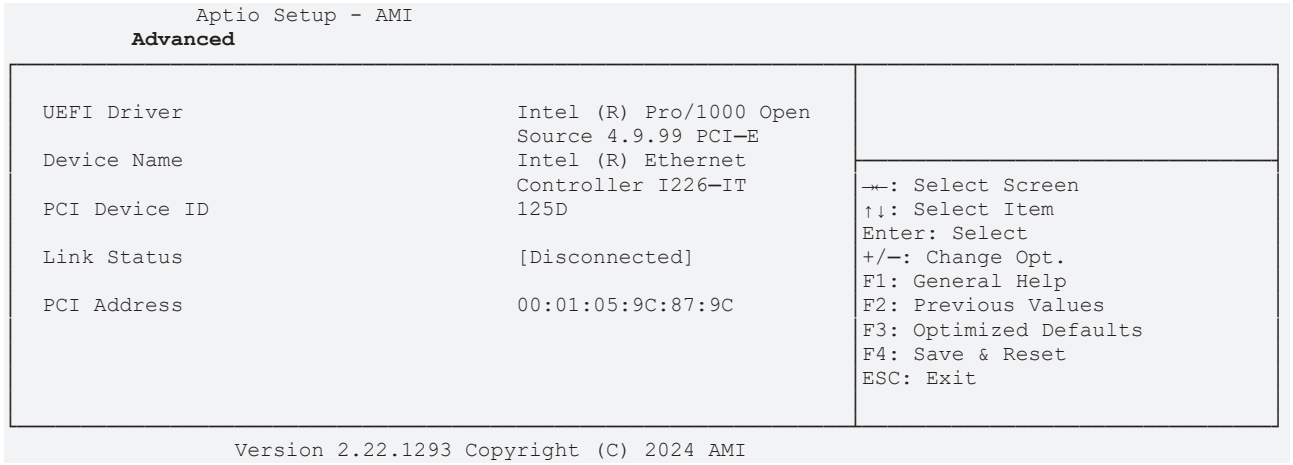
BIOS entry	Options
Enroll Cert Using File	None
Cert GUID	None
Commit Changes and Exit	None
Discard Changes and Exit	None

7.3.13 Intel Rapid Storage Technology



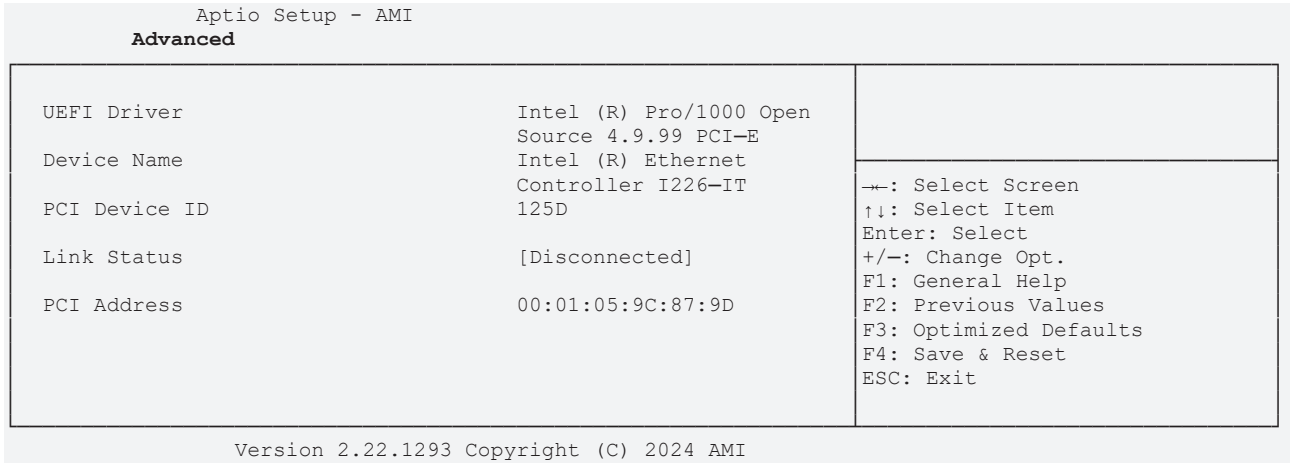
BIOS entry	Options
Intel(R) RST 19.5.0.5676 RST VMD Driver	
No disks connected to system	None

7.3.14 Intel Ethernet Controller I226-IT



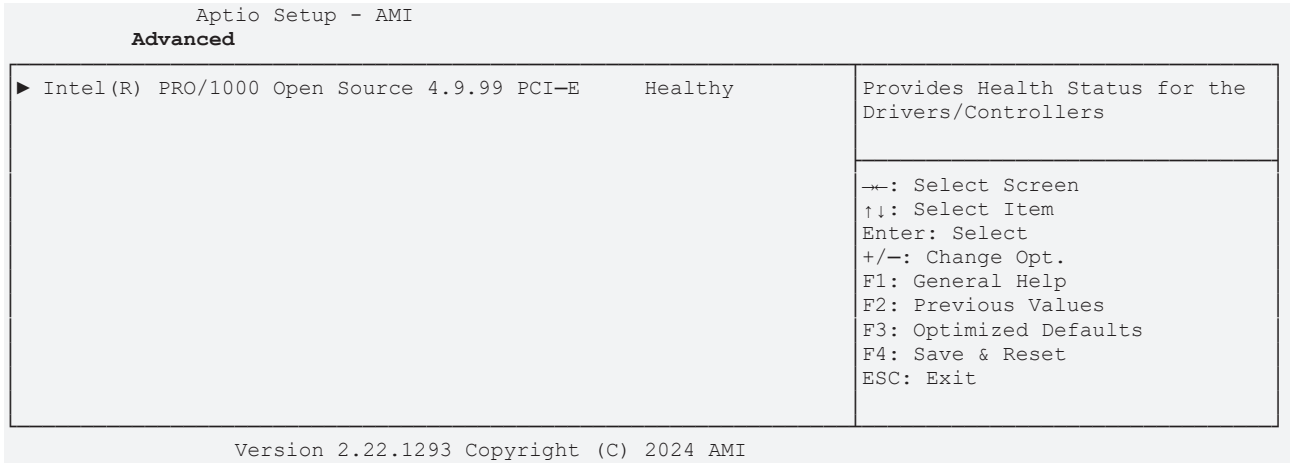
BIOS entry	Options
UEFI Driver	None
Device Name	None
PCI Device ID	None
Link Status	None
MAC Address	None

7.3.15 Intel Ethernet Controller I226-IT



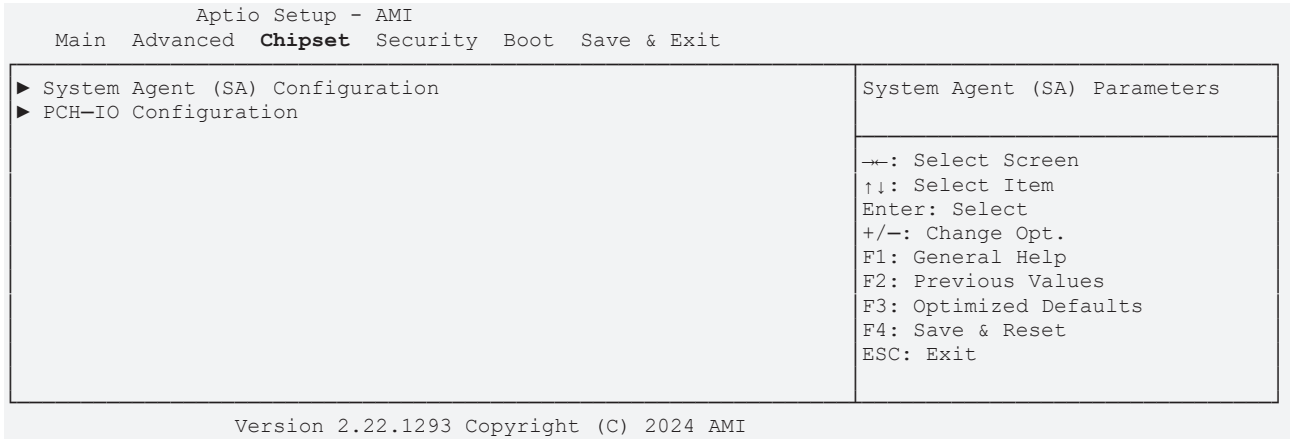
BIOS entry	Options
UEFI Driver	None
Device Name	None
PCI Device ID	None
Link Status	None
MAC Address	None

7.3.16 Driver Health



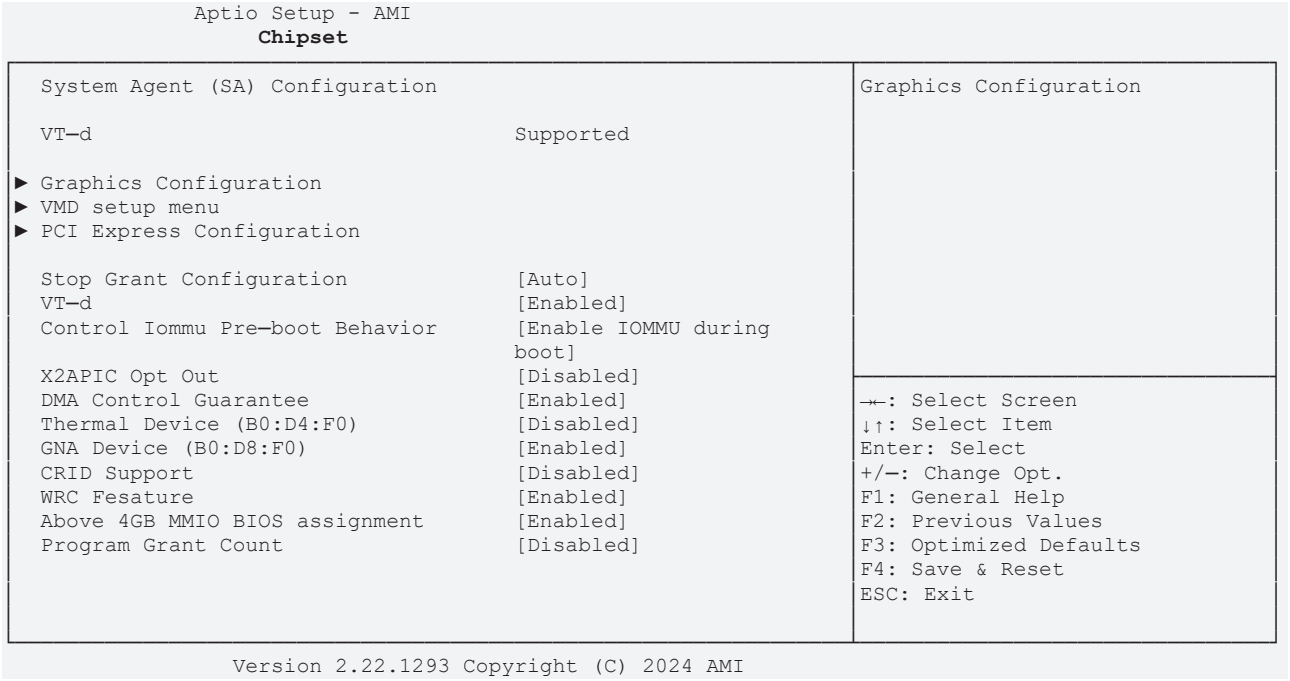
BIOS entry	Options
►Intel® PRO/1000 Open Source 4.9.99 PCI-E	None

7.4 Chipset



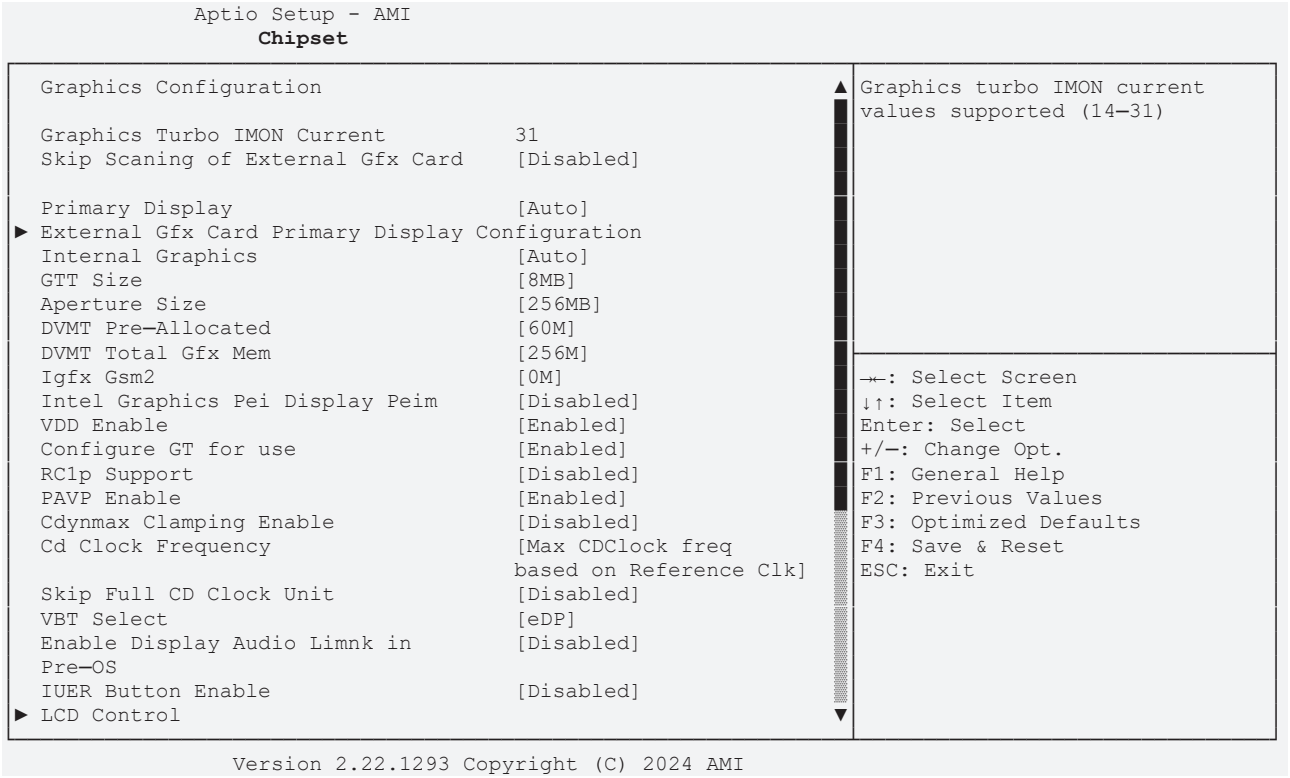
BIOS entry	Options
System Agent (SA) Configuration	Submenu see: System Agent (SA) Configuration [▶ 68]
PCH-IO Configuration	Submenu see: PCH-IO Configuration [▶ 80]

7.4.1 System Agent (SA) Configuration



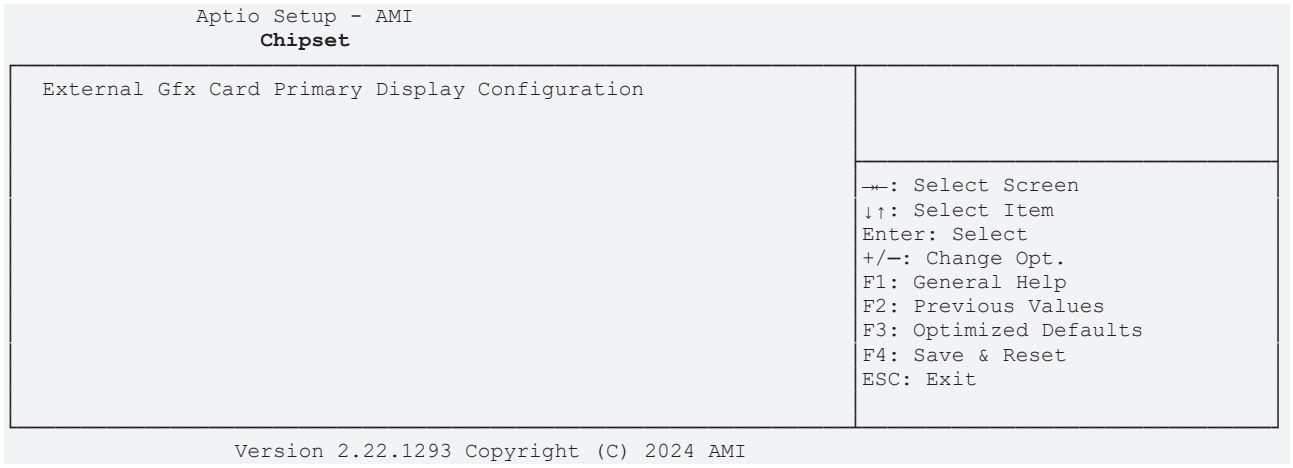
BIOS entry	Options
System Agent (SA) Configuration	
VT-d	None
Graphics Configuration	Submenu see: Graphics Configuration [▶ 69]
VMD setup menu	Submenu see: VMD setup menu [▶ 72]
PCI Express Configuration	Submenu see: PCI Express Configuration [▶ 73]
Stop Grant Configuration	Auto / Manual
VT-d	Enabled / Disabled
Control Iommu Pre-boot Behavior	Enable / Disable
X2APIC Opt Out	Enabled / Disabled
DMA Control Guarantee	Enabled / Disabled
Thermal Device (B0:D4:F0)	Disabled / Enabled
GNA Device (B0:D8:F0)	Enabled / Disabled
CRID Support	Enabled / Disabled
WRC Feature	Enabled / Disabled
Above 4GB MMIO BIOS assignment	Enabled / Disabled
Program Grant Count	Disabled / Enabled

7.4.1.1 Graphics Configuration



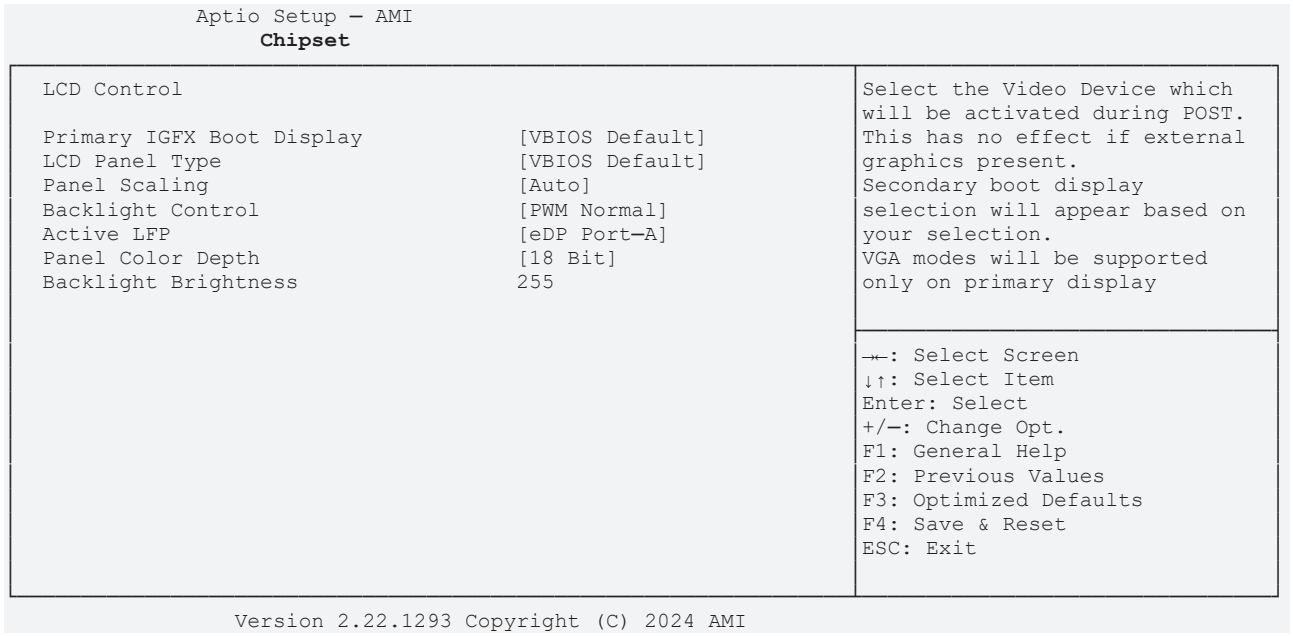
BIOS entry	Options
Graphics Configuration	
Graphics Turbo IMON Current	None
Skip Scaning of External Gfx Card	Disabled / Enabled
Primary Display	Auto / IGFX / PCI / SG
External Gfx Card Primary Display Configuration	None
Internal Graphics	Auto / Disabled / Enabled
GTT Size	2 / 4 / 8 MB
Aperture Size	128 / 256 / 512 / 1024 / 2048 MB
DVMT Pre-Allocated	0M, 32M…60M
DVMT Total Gfx Mem	128M / 256M / MAX
Igfx Gsm2	0GB, 2GB, 4GB, 6GB…32GB
Intel Graphics Pei Display Peim	Disabled / Enabled
VDD Enable	Enabled / Disabled
Configure GT for use	Enabled / Disabled
RC1p Support	Disabled / Enabled
PAVP Enable	Enabled / Disabled
Cdynmax Clamping Enable	Enabled / Disabled
Cd Clock Frequency	Max CdClock freq based on Reference Clk / 192 / 307.2 / 326.4 / 556.8 / 652.8 Mhz
Skip Full CD Clock Unit	Disabled / Enabled
VBT Select	eDP, MIPI, RPLS S17 RVP, RPLS S14 RVP
Enable Display Audio Link in Pre-OS	Disabled / Enabled
IUER Button Enable	Disabled / Enabled
► LCD Control	Submenu see:

7.4.1.1.1 External GFX Card Primary Display Configuration



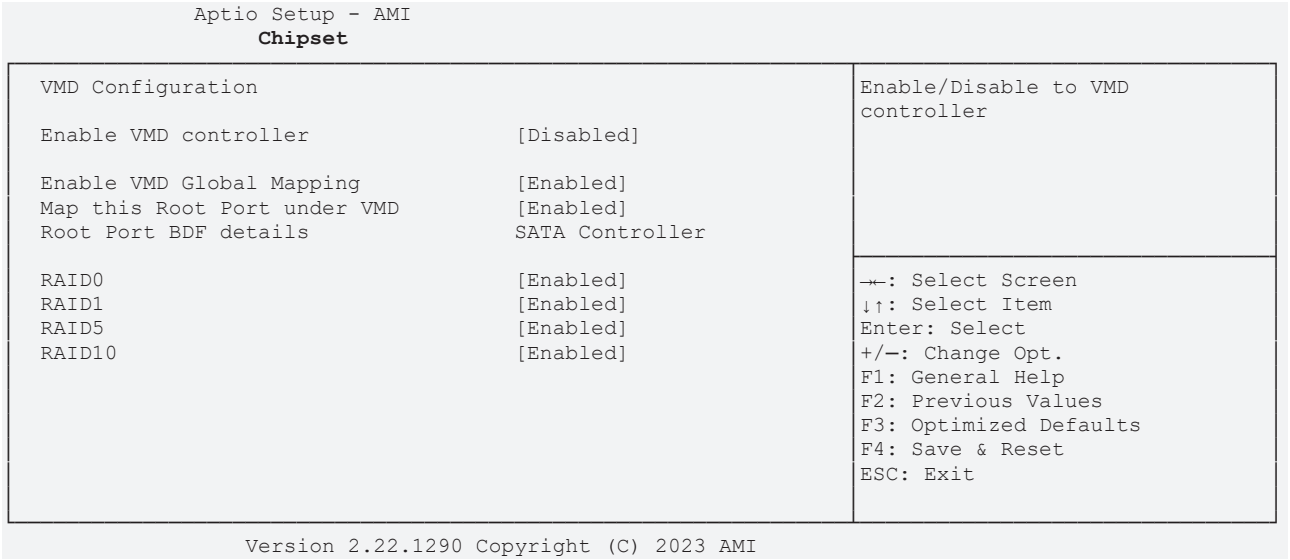
BIOS entry	Options
External Gfx Card Primary Display Configuration	

7.4.1.1.2 LCD Control



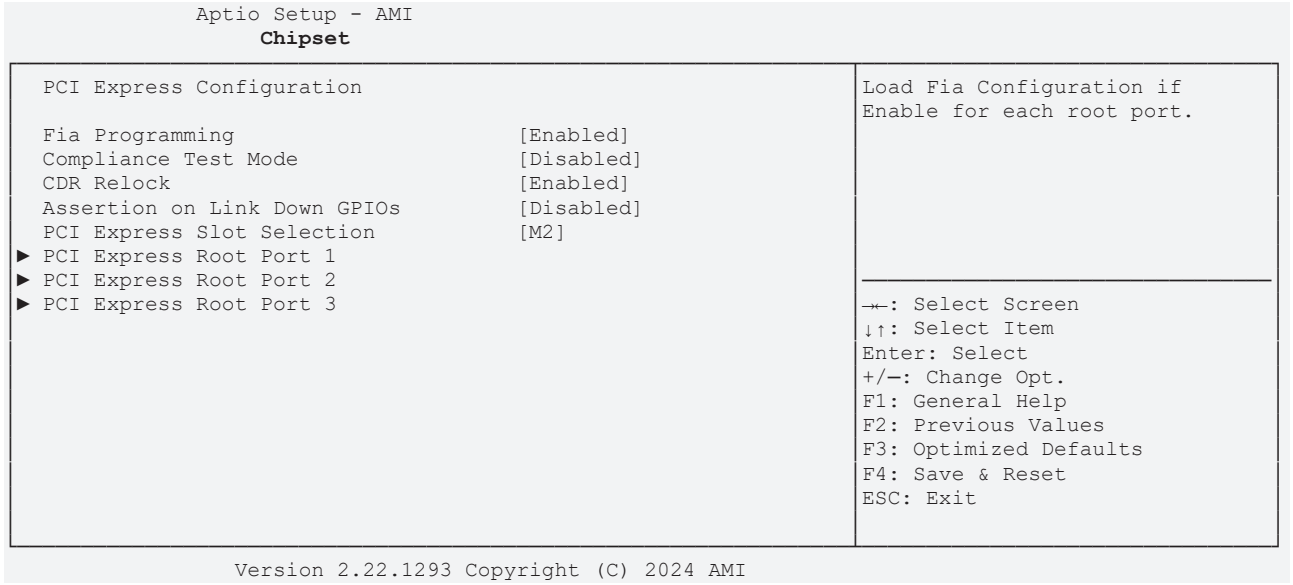
BIOS entry	Options
LCD Control	
Primary IGFX Boot Display	VBIOS / EFP / LFP / EFP3 / EFP 2 / EFP4
LCD Panel Type	VBIOS Default / Various LVDS
Panel Scaling	Auto / Off / Force Scaling
Backlight Control	PWM Normal / PWM Inverted
Active LFP	eDP Port-A / No eDP
Panel Color Depth	18 / 24 Bit
Backlight Brightness	None

7.4.1.2 VMD setup menu



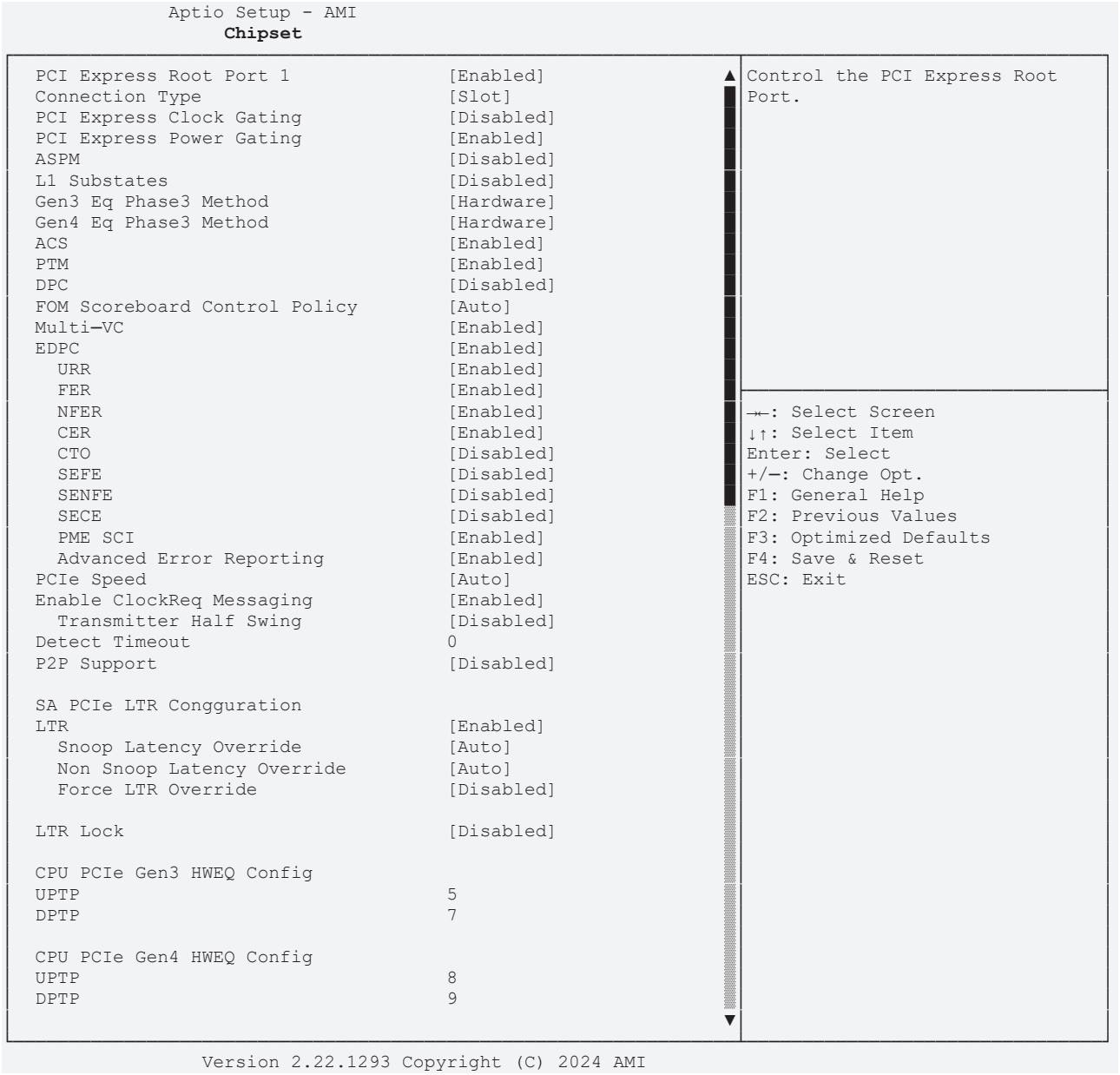
BIOS entry	Options
VMD Configuration	
Enable VMD controller	Disabled / Enabled
Enable VMD Global Mapping	Enabled / Disabled
Map this Root Port under VMD	Enabled / Disabled
Root Port BDF details	None
RAID0	Enabled / Disabled
RAID1	Enabled / Disabled
RAID5	Enabled / Disabled
RAID10	Enabled / Disabled

7.4.1.3 PCI Express Configuration



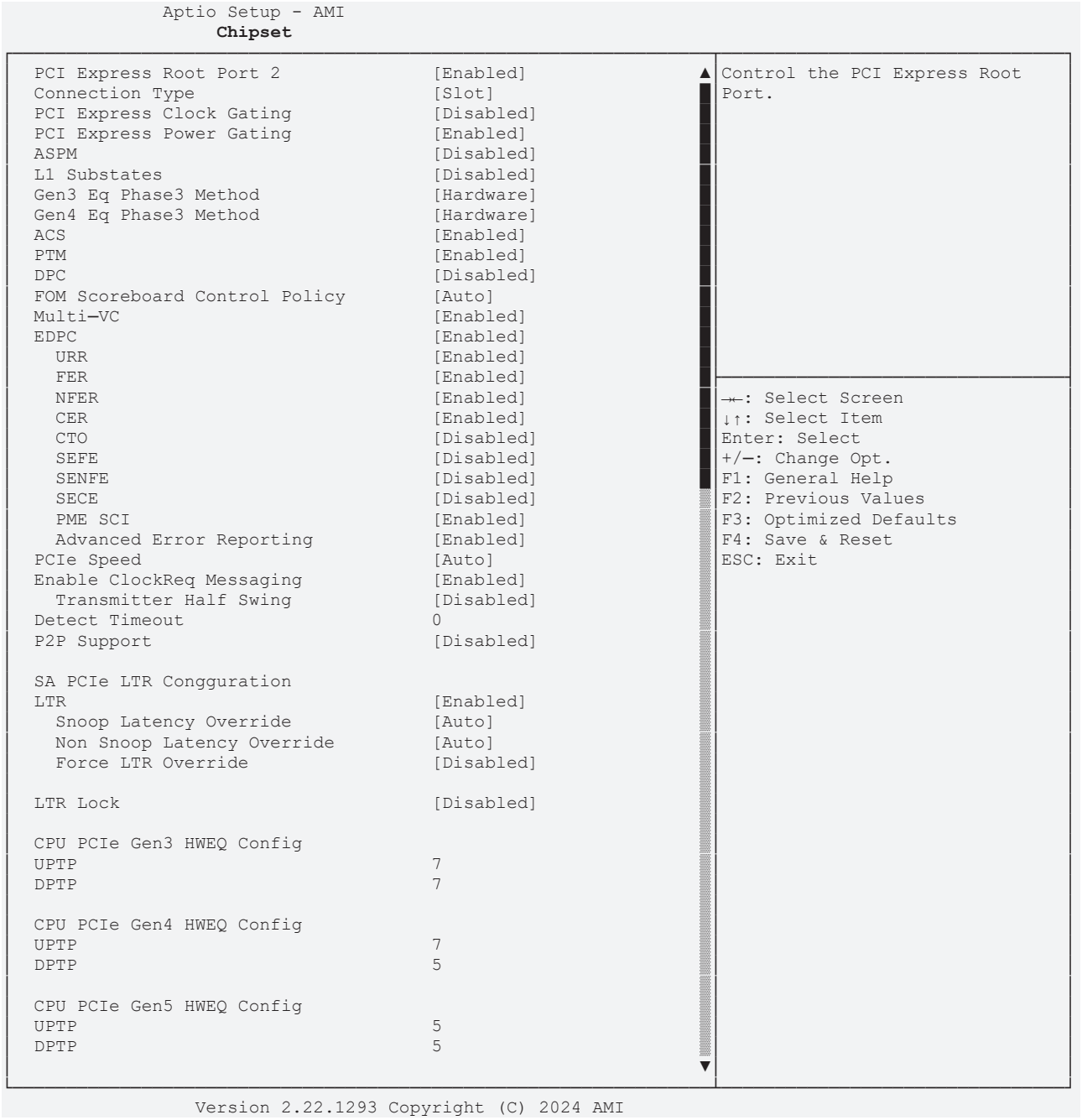
BIOS entry	Options
PCI Express Configuration	
Fia Programming	Enabled / Disabled
Compliance Test Mode	Disabled / Enabled
CDR Relock	Enabled / Disabled
Assertion on Link Down GPIOs	Disabled / Enabled
PCI Express Slot Selection	M2 / CEMx4 slot
PCI Express Root Port 1	Submenu see: PCI Express Root Port 1 [▶ 74]
PCI Express Root Port 2	Submenu see: PCI Express Root Port 2 [▶ 76]
PCI Express Root Port 3	Submenu see: PCI Express Root Port 3 [▶ 78]

7.4.1.3.1 PCI Express Root Port 1



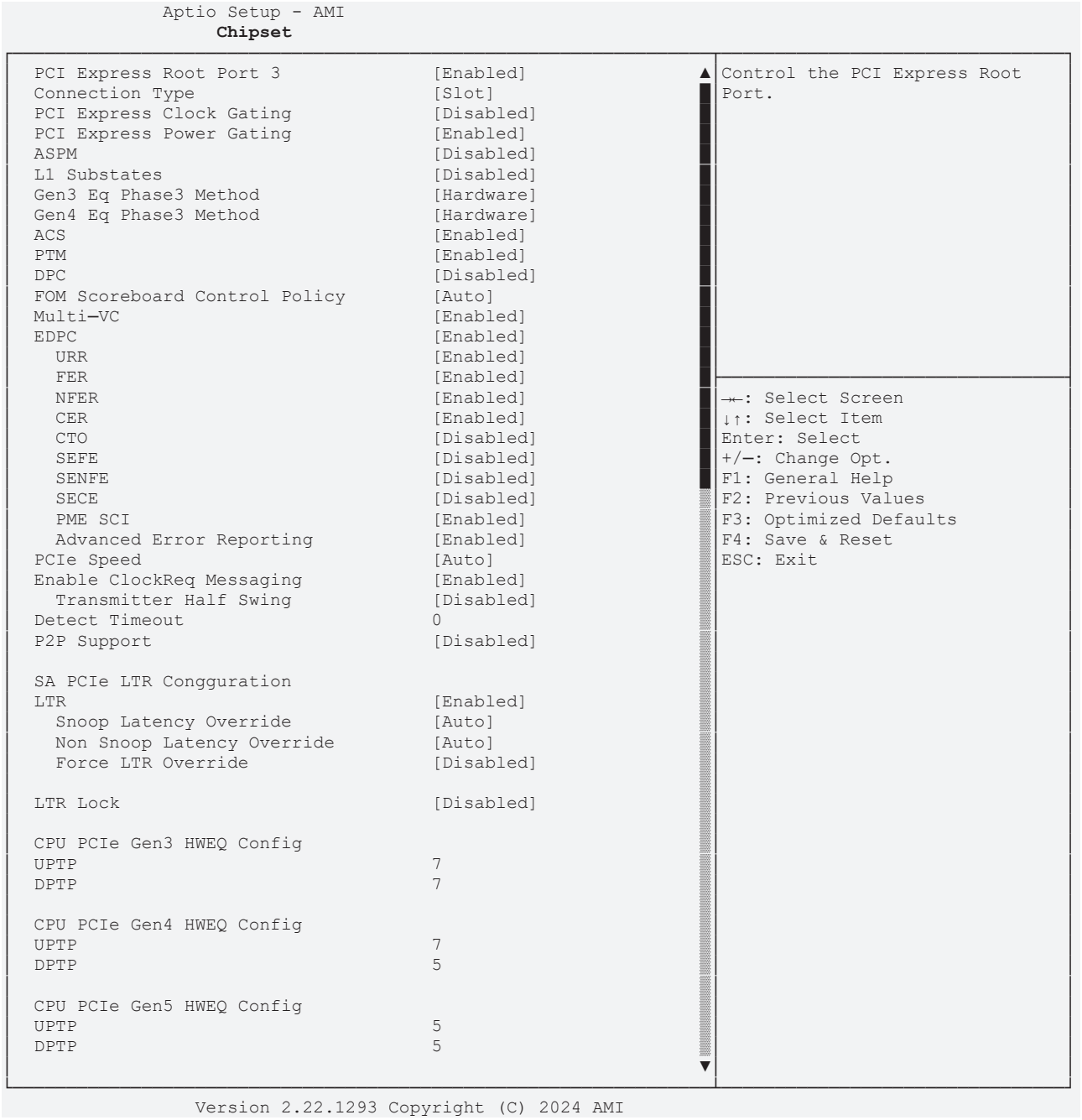
BIOS entry	Options
PCI Express Root Port 1	Enabled / Disabled
Connection Type	Slot / Built - in
PCI Express Clock Gating	None
PCI Express Power Gating	Enabled / Disabled
ASPM	None
L1 Substates	None
Gen3 Eq Phase3 Method	Hardware / Static Coeff.
Gen4 Eq Phase3 Method	Hardware / Static Coeff.
ACS	Enabled / Disabled
PTM	None
DPC	Enabled / Disabled
FOM Scoreboard Control Policy	Auto / Gen3 / Gen4 / Gen3/Gen4 / Gen5
Multi-VC	None
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
CTO	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Enabled / Disabled
Advanced Error Reporting	Disabled / Enabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3 / Gen4
Enable ClockReq Messaging	Enabled / Disabled
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
P2P Support	Disabled / Enabled
SA PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled
CPU PCIe Gen3 HWEQ Config	
UPTP	None
DPTP	None
CPU PCIe Gen4 HWEQ Config	
UPTP	None
DPTP	None

7.4.1.3.2 PCI Express Root Port 2



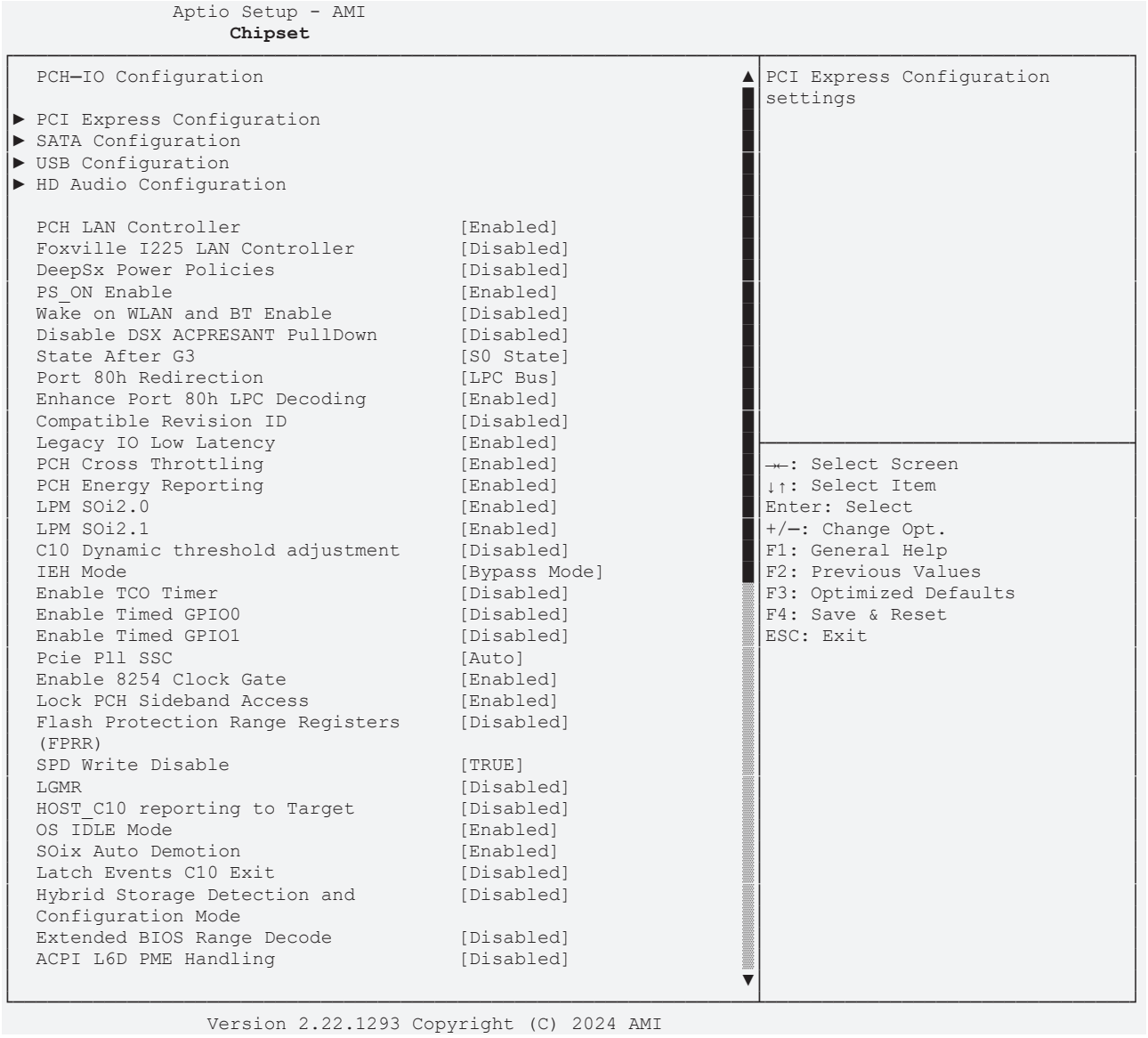
BIOS entry	Options
PCI Express Root Port 2	Enabled / Disabled
Connection Type	Slot / Built-in
PCI Express Clock Gating	Enabled / Disabled
PCI Express Power Gating	Enabled / Disabled
ASPM	Disabled / Enabled
L1 Substates	L1.1 & L1.2 / L1.1 / Disabled
Gen3 Eq Phase3 Method	Hardware / Static Coeff.
Gen4 Eq Phase3 Method	Hardware / Static Coeff.
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
FOM Scoreboard Control Policy	Auto / Gen3 / Gen4 / Gen3 / Gen4
Multi-VC	Disabled / Enabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
CTO	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Enabled / Disabled
Advanced Error Reporting	Disabled / Enabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3 / Gen4
Enable ClockReq Messaging	Enabled / Disabled
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
P2P Support	Disabled / Enabled
SA PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled
CPU PCIe Gen3 HWEQ Config	
UPTP	None
DPTP	None
CPU PCIe Gen4 HWEQ Config	
UPTP	None
DPTP	None
CPU PCIe Gen5 HWEQ Config	
UPTP	None
DPTP	None

7.4.1.3.3 PCI Express Root Port 3



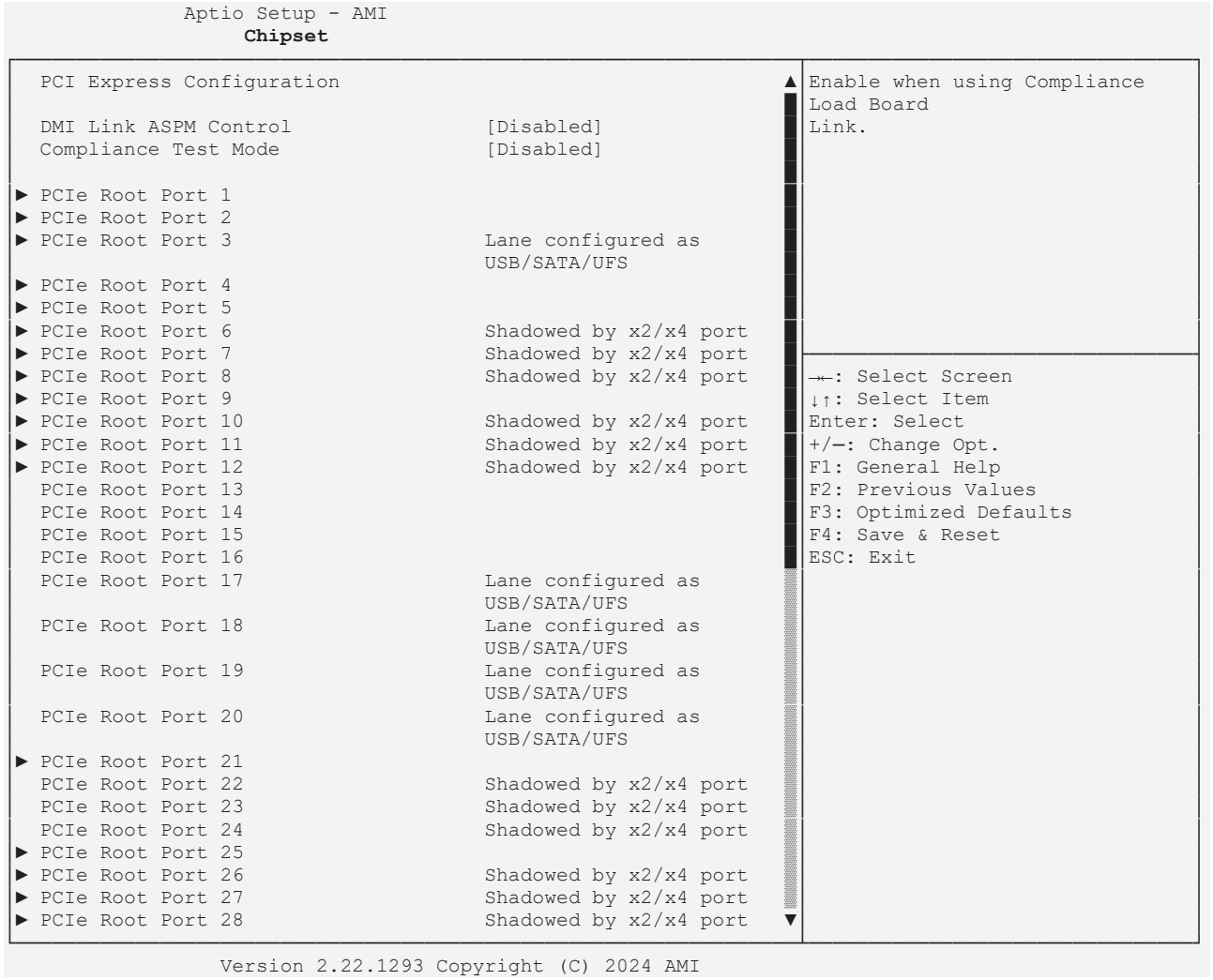
BIOS entry	Options
PCI Express Root Port 3	Enabled / Disabled
Connection Type	Slot / Built-in
PCI Express Clock Gating	None
PCI Express Power Gating	Enabled / Disabled
ASPM	None
L1 Substates	None
Gen3 Eq Phase3 Method	Hardware / Static Coeff.
Gen4 Eq Phase3 Method	Hardware / Static Coeff.
ACS	Enabled / Disabled
PTM	None
DPC	Enabled / Disabled
FOM Scoreboard Control Policy	Auto / Gen3 / Gen4 / Gen3/Gen4 / Gen5
Multi-VC	None
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
CTO	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
SECE	Disabled / Enabled
PME SCI	Enabled / Disabled
Advanced Error Reporting	Disabled / Enabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3 / Gen4 / Gen5
Enable ClockReq Messaging	Enabled / Disabled
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
P2P Support	Disabled / Enabled
SA PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Auto / Manual / Disabled
Non Snoop Latency Override	Auto / Manual / Disabled
Force LTR Override	Disabled / Enabled
LTR Lock	Disabled / Enabled
CPU PCIe Gen3 HWEQ Config	
UPTP	None
DPTP	None
CPU PCIe Gen4 HWEQ Config	
UPTP	None
DPTP	None
CPU PCIe Gen5 HWEQ Config	
UPTP	None
DPTP	None

7.4.2 PCH-IO Configuration



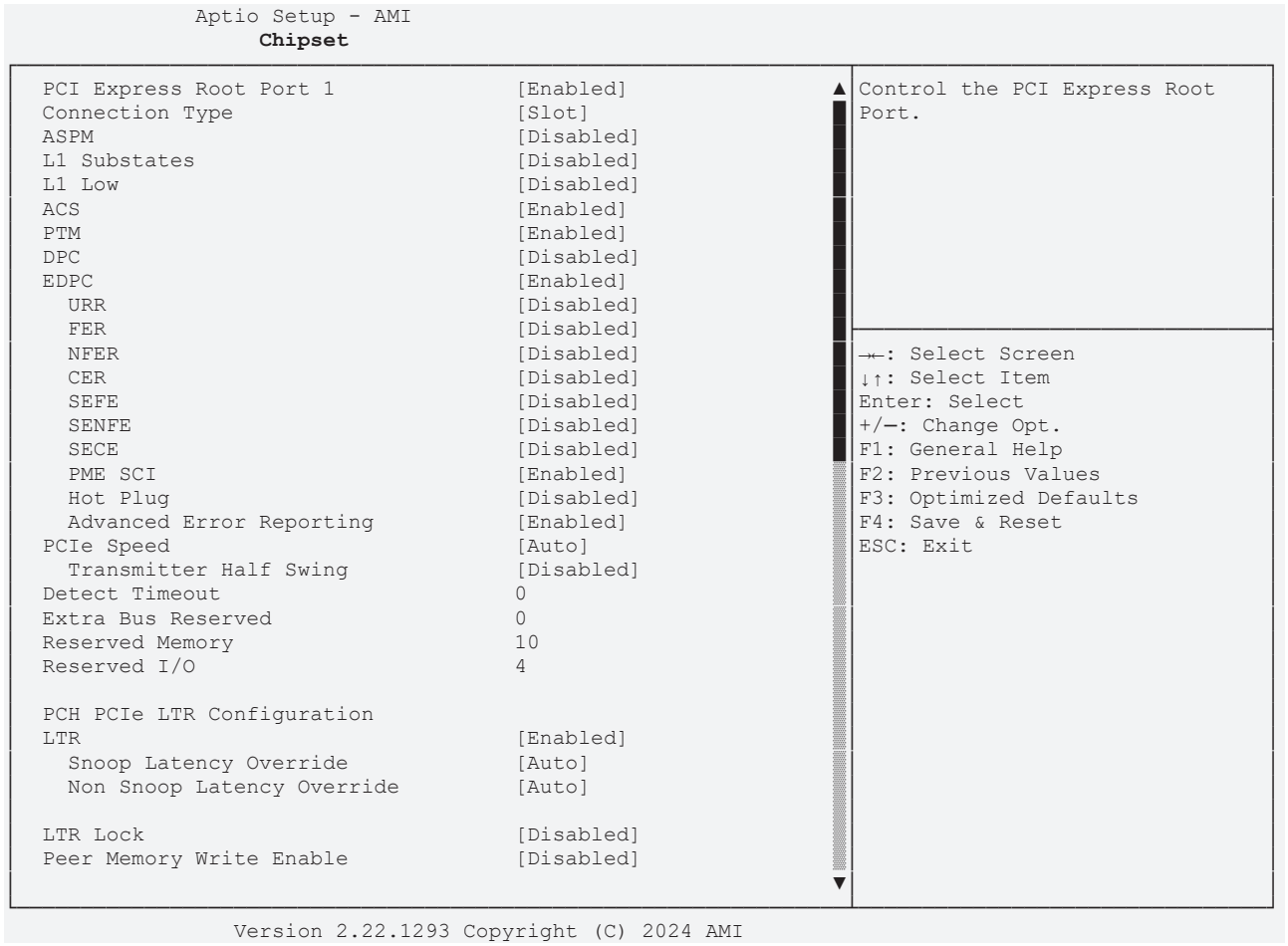
BIOS entry	Options
PCH-IO Configuration	
PCI Express Configuration	Submenu see: PCI Express Configuration [▶ 82]
SATA Configuration	Submenu see: SATA Configuration [▶ 85]
USB Configuration	Submenu see: USB Configuration [▶ 87]
HD Audio Configuration	Submenu see: HD Audio Configuration [▶ 89]
PCH LAN Controller	Enabled / Disabled
Foxville I225 LAN Controller	Enabled / Disabled
DeepSx Power Policies	Disabled / Enabled
PS_ON Enable	Disabled / Enabled
Wake on LAN and BT Enable	Disabled / Enabled
Disable DSX ACPRESENT Pull Down	Disable / Enabled
State After G3	S0 State / S5 State
Port 80h Redirection	LPC Bus / PCIE Bus
Enhance Port 80h LPC Decoding	Enabled / Disabled
Compatible Revision ID	None
Legacy IO Low Latency	None
PCH Cross Throttling	Enabled / Disabled
PCH Energy Reporting	Enabled / Disabled
LPM SOi2.0	Enabled / Disabled
LPM SOi2.1	Enabled / Disabled
Second LAN Controller	Enabled / Disabled
C10 Dynamic threshold adjustment	Disabled / Enabled
IEH Mode	Bypass Mode / Enabled
Enable TCO Timer	Disabled / Enabled
Enable Timed GPIO0	Enabled / Disabled
Enable Timed GPIO1	Enabled / Disabled
Pcie Pll SSC	Auto / 0.0%…0.5% / Disabled
Enable 8254 Clock Gate	Enabled / Disabled
Lock PCH Sideband Access	Enabled / Disabled
Flash Protection Range Registers (FPRR)	Disabled / Enabled
SPD Write Disable	True / False
LGMR	Disabled / Enabled
HOST_C10 reporting to Target	Disabled / Enabled
OS IDLE Mode	Enabled / Disabled
SOix Auto Demotion	Enabled / Disabled
Latch Events C10 Exit	Disabled / Enabled
Hybrid Storage Detection and Configuration Mode	Disabled / Enabled
Extended BIOS Range Decode	Disabled / Enabled
ACPI L6D PME Handling	Disabled / Enabled

7.4.2.1 PCI Express Configuration



BIOS entry	Options
PCI Express Configuration	
DMI Link ASPM Control	Disabled / Enabled
Compliance Test Mode	Disabled / Enabled
PCIe Root Port 1	Submenu see: PCI Express Root Port 1 [▶ 83]
PCIe Root Port 2	Submenu see: PCI Express Root Port 1 [▶ 83]
PCIe Root Port 3	None
PCIe Root Port 4, 5, 9, 13 - 16, 21, 25	Submenu see: PCI Express Root Port 1 [▶ 83]
PCIe Root Port 6 - 8, 10 - 12, 17 – 20, 22 - 24, 26 - 28	None

7.4.2.1.1 PCI Express Root Port 1



BIOS entry	Options
PCI Express Root Port 1	Disabled / Enabled
Connection Type	Built-in / Slot
ASPM	Disabled / Enabled
L1 Substates	Disabled / Enabled
L1 Low	Disabled / Enabled
ACS	Enabled / Disabled
PTM	Enabled / Disabled
DPC	Enabled / Disabled
EDPC	Enabled / Disabled
URR	Disabled / Enabled
FER	Disabled / Enabled
NFER	Disabled / Enabled
CER	Disabled / Enabled
SEFE	Disabled / Enabled
SENFE	Disabled / Enabled
PME SCI	Enabled / Disabled
Hot Plug	Disabled / Enabled
Advanced Error Reporting	Enabled / Disabled
PCIe Speed	Auto / Gen1 / Gen2 / Gen3 / Gen4
Transmitter Half Swing	Disabled / Enabled
Detect Timeout	None
Extra Bus Reserved	None
Reserved Memory	None
Reserved I/O	None
PCH PCIe LTR Configuration	
LTR	Enabled / Disabled
Snoop Latency Override	Disbaled / Manual / Auto
Non Snoop Latency Override	Disbaled / Manual / Auto
LTR Lock	Disabled / Enabled
Peer Memory Write Enable	Disabled / Enabled

NOTICE

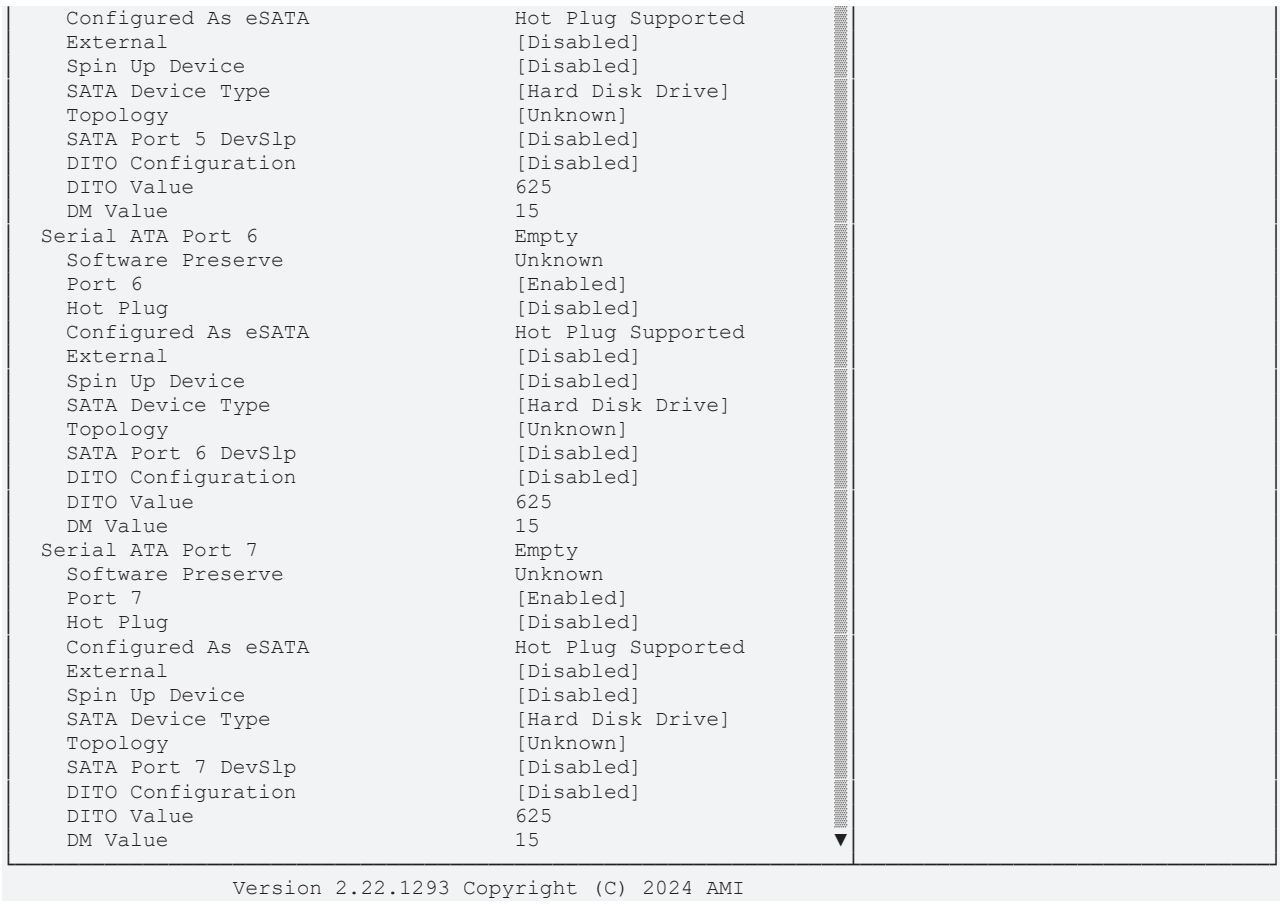
PCI Express Configuration

The BIOS entries and the options on ports 1 - 2, 4, 5, 9, 13 - 16, 21, 25 are identical. Port 1 is shown as an example

7.4.2.2 SATA Configuration

```
              Aptio Setup - AMI
                   Chipset
```

SATA Configuration		Enable/Disable SATA Device.
SATA Controller(s)	[Enabled]	
SATA Test Mode	[Disabled]	
Aggressive LPM Support	[Enabled]	
Serial ATA Port 0	Empty	
Software Preserve	Unknown	
Port 0	[Enabled]	→←: Select Screen
Hot Plug	[Disabled]	↓↑: Select Item
Configured as eSATA	Hot Plug Supported	Enter: Select
External	[Disabled]	+/-: Change Opt.
Spin Up Device	[Disabled]	F1: General Help
SATA Device Type	[Hard Disk Drive]	F2: Previous Values
Topology	[Unknown]	F3: Optimized Defaults
SATA Port 0 DevSlp	[Disabled]	F4: Save & Reset
DITO Configuration	[Disabled]	ESC: Exit
DITO Value	625	
DM Value	15	
Serial ATA Port 1	Empty	
Software Preserve	Unknown	
Port 1	[Enabled]	
Hot Plug	[Disabled]	
Configured As eSATA	Hot Plug Supported	
External	[Disabled]	
Spin Up Device	[Disabled]	
SATA Device Type	[Hard Disk Drive]	
Topology	[Unknown]	
SATA Port 1 DevSlp	[Disabled]	
DITO Configuration	[Disabled]	
DITO Value	625	
DM Value	15	
Serial ATA Port 2	Empty	
Software Preserve	Unknown	
Port 2	[Enabled]	
Hot Plug	[Disabled]	
Configured As eSATA	Hot Plug Supported	
External	[Disabled]	
Spin Up Device	[Disabled]	
SATA Device Type	[Hard Disk Drive]	
Topology	[Unknown]	
SATA Port 2 DevSlp	[Disabled]	
DITO Configuration	[Disabled]	
DITO Value	625	
DM Value	15	
Serial ATA Port 3	Empty	
Software Preserve	Unknown	
Port 3	[Enabled]	
Hot Plug	[Disabled]	
Configured As eSATA	Hot Plug Supported	
External	[Disabled]	
Spin Up Device	[Disabled]	
SATA Device Type	[Hard Disk Drive]	
Topology	[Unknown]	
SATA Port 3 DevSlp	[Disabled]	
DITO Configuration	[Disabled]	
DITO Value	625	
DM Value	15	
Serial ATA Port 4	Empty	
Software Preserve	Unknown	
Port 4	[Enabled]	
Hot Plug	[Disabled]	
Configured As eSATA	Hot Plug Supported	
External	[Disabled]	
Spin Up Device	[Disabled]	
SATA Device Type	[Hard Disk Drive]	
Topology	[Unknown]	
SATA Port 4 DevSlp	[Disabled]	
DITO Configuration	[Disabled]	
DITO Value	625	
DM Value	15	
Serial ATA Port 5	Empty	
Software Preserve	Unknown	
Port 5	[Enabled]	
Hot Plug	[Disabled]	



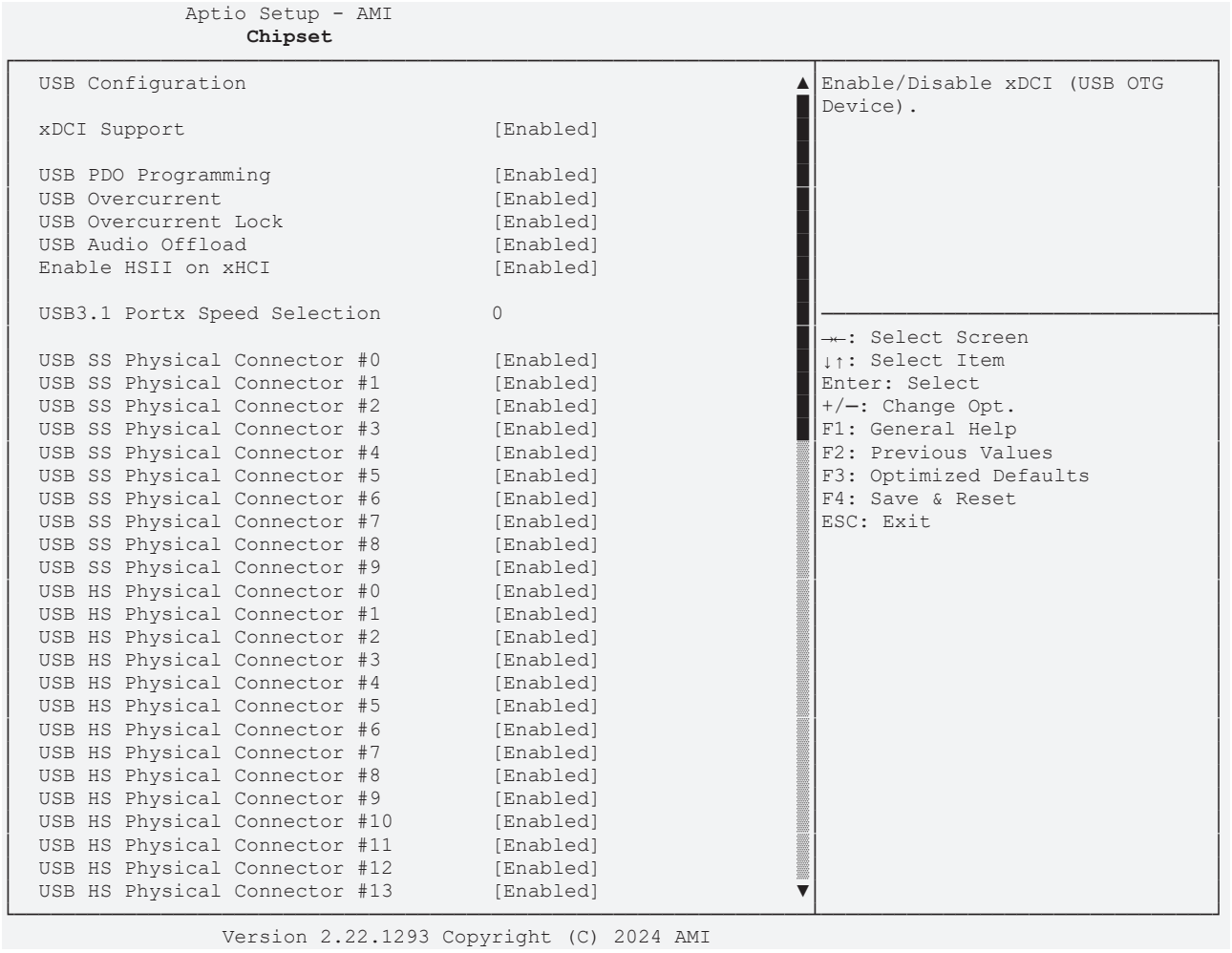
BIOS entry	Options
SATA Configuration	
SATA Controller(s)	Enabled / Disabled
SATA Test Mode	Disabled / Enabled
Serial ATA Port 0	None
Software Preserve	None
Port 0	Enabled / Disabled
Hot Plug	Disabled / Enabled
Configured as eSATA	None
External	Disabled / Enabled
Spin Up Device	Disabled / Enabled
SATA Device Type	Hard Disk Drive / Solid State Drive
Topology	Unknown / ISATA / Direct Connect / Flex / M2
SATA Port 0 DevSlp	Disabled / Enabled
DITO Configuration	Disabled / Enabled
DITO Value	None
DM Value	None

NOTICE

SATA Configuration

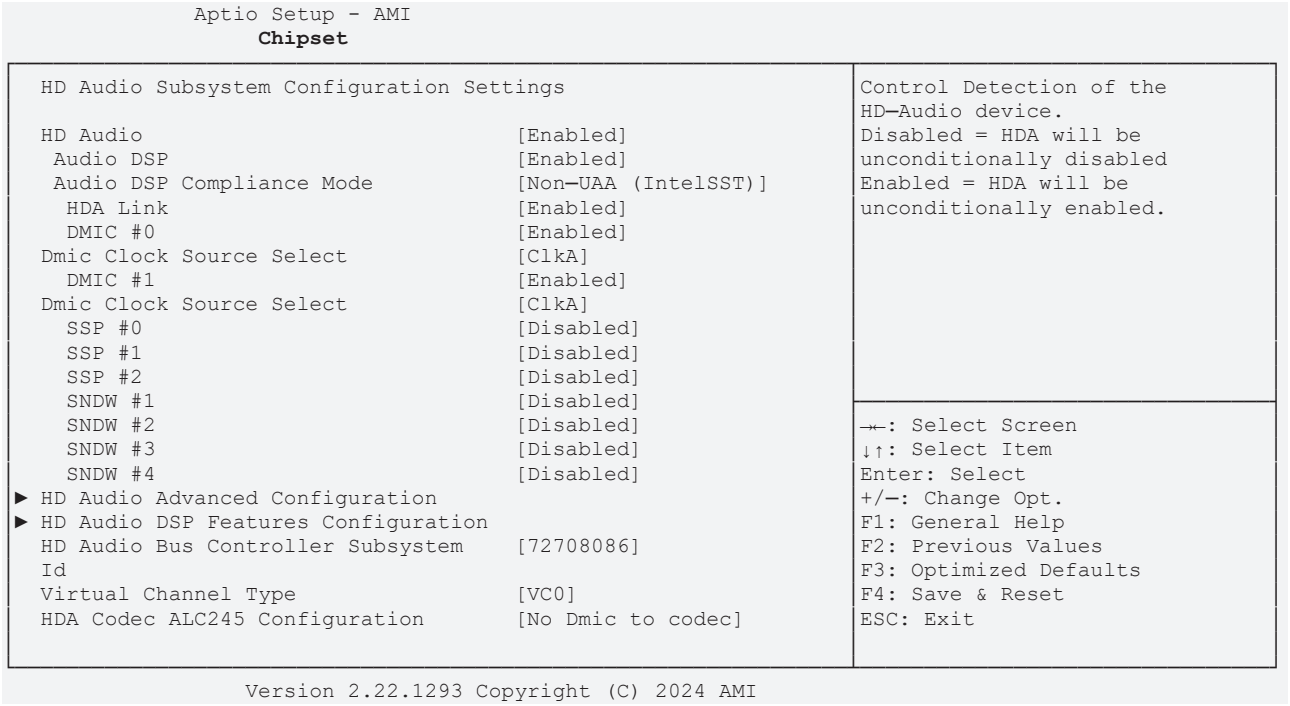
The BIOS entries and the options on the SATA ports 1 - 7 are identical. Port 0 is shown as an example.

7.4.2.3 USB Configuration



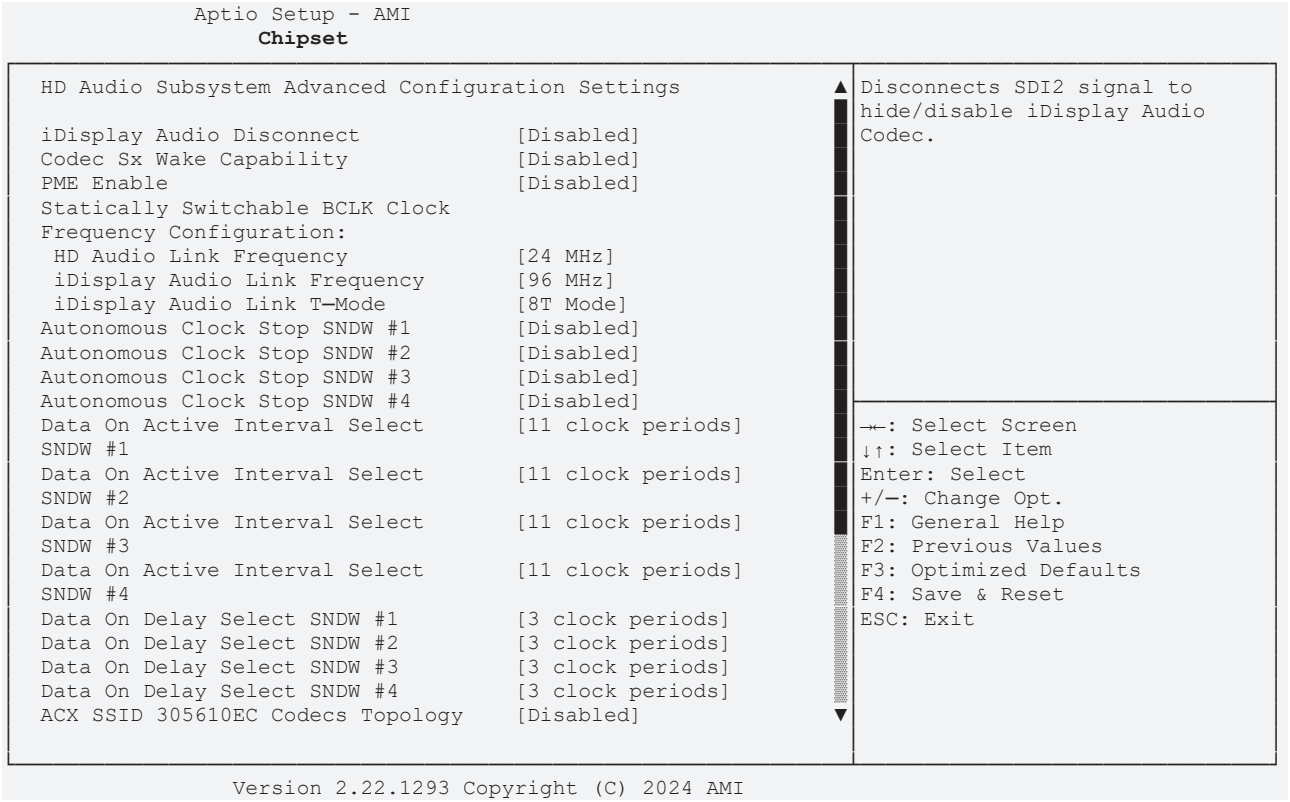
BIOS entry	Options
USB Configuration	
xDCI Support	Enabled / Disabled
USB PDO Programming	Enabled / Disabled
USB Overcurrent	Enabled / Disabled
USB Overcurrent Lock	Enabled / Disabled
USB Audio Offload	Enabled / Disabled
Enable HSII on xHCI	Enabled / Disabled
USB3.1 Portx Speed Selection	None
USB SS Physical Connector #0	Enabled / Disabled
USB SS Physical Connector #1	Enabled / Disabled
USB SS Physical Connector #2	Enabled / Disabled
USB SS Physical Connector #3	Enabled / Disabled
USB SS Physical Connector #4	Enabled / Disabled
USB SS Physical Connector #5	Enabled / Disabled
USB SS Physical Connector #6	Enabled / Disabled
USB SS Physical Connector #7	Enabled / Disabled
USB SS Physical Connector #8	Enabled / Disabled
USB SS Physical Connector #9	Enabled / Disabled
USB HS Physical Connector #1	Enabled / Disabled
USB HS Physical Connector #2	Enabled / Disabled
USB HS Physical Connector #3	Enabled / Disabled
USB HS Physical Connector #4	Enabled / Disabled
USB HS Physical Connector #5	Enabled / Disabled
USB HS Physical Connector #6	Enabled / Disabled
USB HS Physical Connector #7	Enabled / Disabled
USB HS Physical Connector #8	Enabled / Disabled
USB HS Physical Connector #9	Enabled / Disabled
USB HS Physical Connector #10	Enabled / Disabled
USB HS Physical Connector #11	Enabled / Disabled
USB HS Physical Connector #12	Enabled / Disabled
USB HS Physical Connector #13	Enabled / Disabled

7.4.2.4 HD Audio Configuration



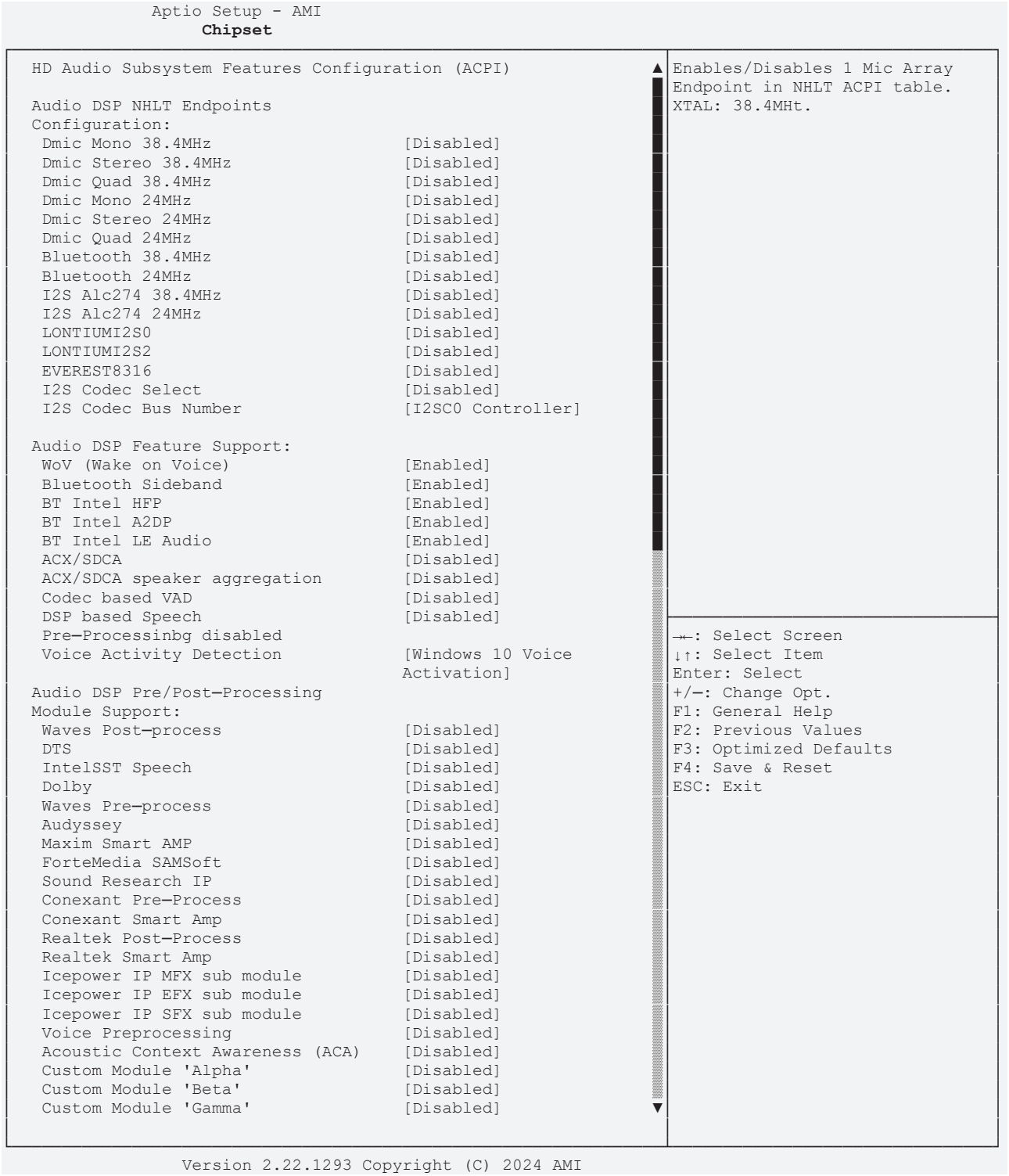
BIOS entry	Options
HD Audio Subsystem Configuration Settings	
HD Audio	Enabled / Disabled
Audio DSP	Enabled / Disabled
Audio DSP Compliance Mode	Non-UAA (IntelSST) / UAA (HDA Inbox/IntelSST)
HDA Link	Enabled / Disabled
DMIC #0	Enabled / Disabled
Dmic Clock Source Select	CLKA / CLB / Both
DMIC #1	Enabled / Disabled
Dmic Clock Source Select	CLKA / CLB / Both
SSP #0	None
SSP #1	Disabled / Enabled
SSP #2	Disabled / Enabled
SNDW #1	None
SNDW #2	Disabled / Enabled
SNDW #3	None
SNDW #4	None
HD Audio Advanced Configuration	Submenu see: HD Audio Subsystem Advanced Configuration Settings [▶ 90]
HD Audio DSP Features Configuration	Submenu see: HD Audio Subsystem Feature Configuration (ACPI) [▶ 92]
HD Audio Bus Controller Subsystem ID	Various
Virtual Channel Type	VC0 / VC1
HDA Codec ALC245 Configuration	No Dmic to codec / 4 Dmic to codec / 2 Dmic to codec

7.4.2.4.1 HD Audio Subsystem Advanced Configuration Settings



BIOS entry	Options
HD Audio Subsystem Advanced Configuration Settings	
iDisplay Audio Disconnect	Disabled / Enabled
Codec Sx Wake Capability	Disabled / Enabled
PME Enable	Disabled / Enabled
Statically Switchable BCLK Clock Frequency Configuration	
HD Audio Link Frequency	24 / 6 / 12 MHz
iDisplay Audio Link Frequency	96 / 48 MHz
iDisplay Audio Link T-Mode	8T Mode / 1T Mode / 2T Mode / 4T Mode / 16T Mode
Autonomous Clock Stop SNDW #1	Disabled / Enabled
Autonomous Clock Stop SNDW #2	Disabled / Enabled
Autonomous Clock Stop SNDW #3	Disabled / Enabled
Autonomous Clock Stop SNDW #4	Disabled / Enabled
Data On Active Interval Select SNDW #1	11 clock periods / 6, 7, 8 clock periods
Data On Active Interval Select SNDW #2	11 clock periods / 6, 7, 8 clock periods
Data On Active Interval Select SNDW #3	11 clock periods / 6, 7, 8 clock periods
Data On Active Interval Select SNDW #4	11 clock periods / 6, 7, 8 clock periods
Data On Delay Select SNDW #1	3 clock periods / 2 clock periods
Data On Delay Select SNDW #2	3 clock periods / 2 clock periods
Data On Delay Select SNDW #3	3 clock periods / 2 clock periods
Data On Delay Select SNDW #4	3 clock periods / 2 clock periods
ACX SSID 305610EC Codecs Topology	Disabled / Enabled

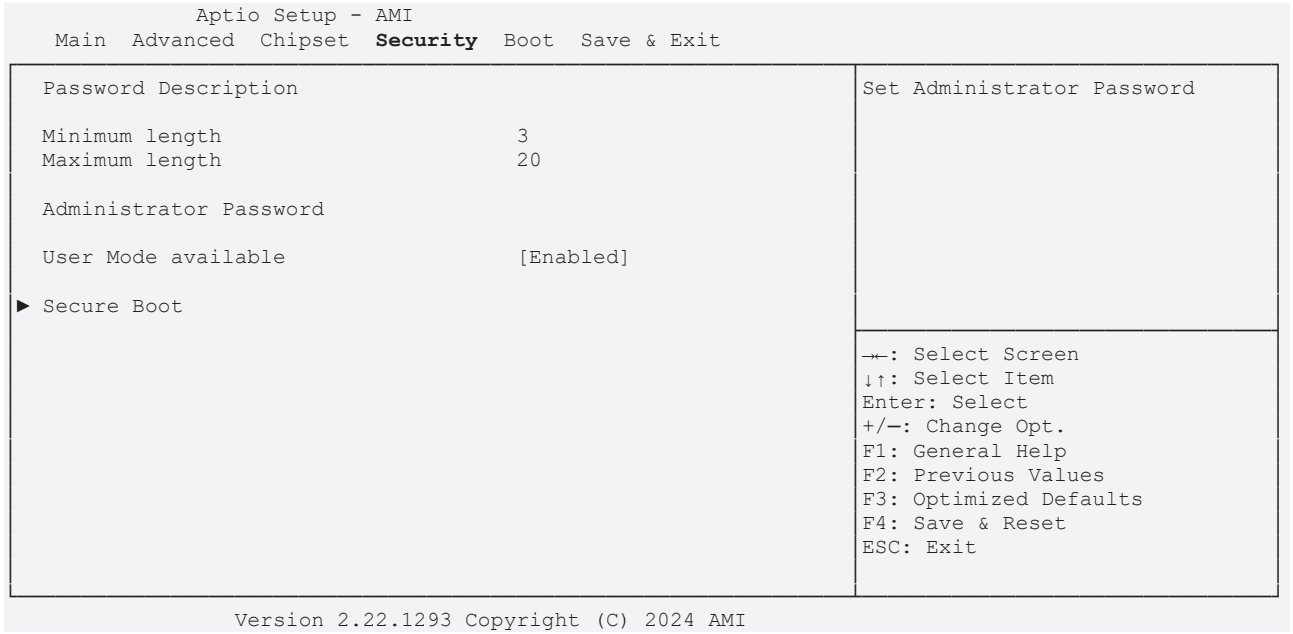
7.4.2.4.2 HD Audio Subsystem Feature Configuration (ACPI)



BIOS entry	Options
HD Audio Subsystem Features Configuration (ACPI)	
Audio DSP NHLT Endpoints Configuration:	
Dmic Mono 38.4MHz	Disabled / Enabled
Dmic Stereo 38.4MHz	Disabled / Enabled
Dmic Quad 38.4MHz	Disabled / Enabled
Dmic Mono 24MHz	Disabled / Enabled
Dmic Stereo 24MHz	Disabled / Enabled
Dmic Quad 24MHz	Disabled / Enabled
Bluetooth 38.4MHz	None
Bluetooth 24MHz	None
I2S Alc274 38.4MHz	None
I2S Alc274 24MHz	None
LONTIUMI2S0	None
LONTIUMI2S2	None
EVEREST8316	None
I2S Codec Select	None
I2S Codec Bus Number	None
Audio DSP Feature Support:	
WoV (Wake on Voice)	Enabled / Disabled
Bluetooth Sideband	Enabled / Disabled
BT Intel HFP	Enabled / Disabled
BT Intel A2DP	Enabled / Disabled
BT Intel LE Audio	Disabled / Enabled
ACX/SDCA	Disabled / Enabled
ACX/SDCA speaker aggregation	None
Codec based VAD	Disabled / Enabled
DSP based Speech	None
Pre-Processinbg Disabled	None
Voice Activity Detection	Windows 10 Voice Activation / Intel Wake on Voice
Audio DSP Pre/Post-Processing Module Support:	
Waves Post-process	Disabled / Enabled
DTS	Disabled / Enabled
IntelSST Speech	Disabled / Enabled
Dolby	Disabled / Enabled
Waves Pre-process	Disabled / Enabled
Audyssey	Disabled / Enabled
Maxim Smart AMP	Disabled / Enabled
ForteMedia SAMSoft	Disabled / Enabled
Sound Research IP	Disabled / Enabled
Conexant Pre-Process	Disabled / Enabled
Conexant Smart Amp	Disabled / Enabled
Realtek Post-Process	Disabled / Enabled
Realtek Post-Process	Disabled / Enabled

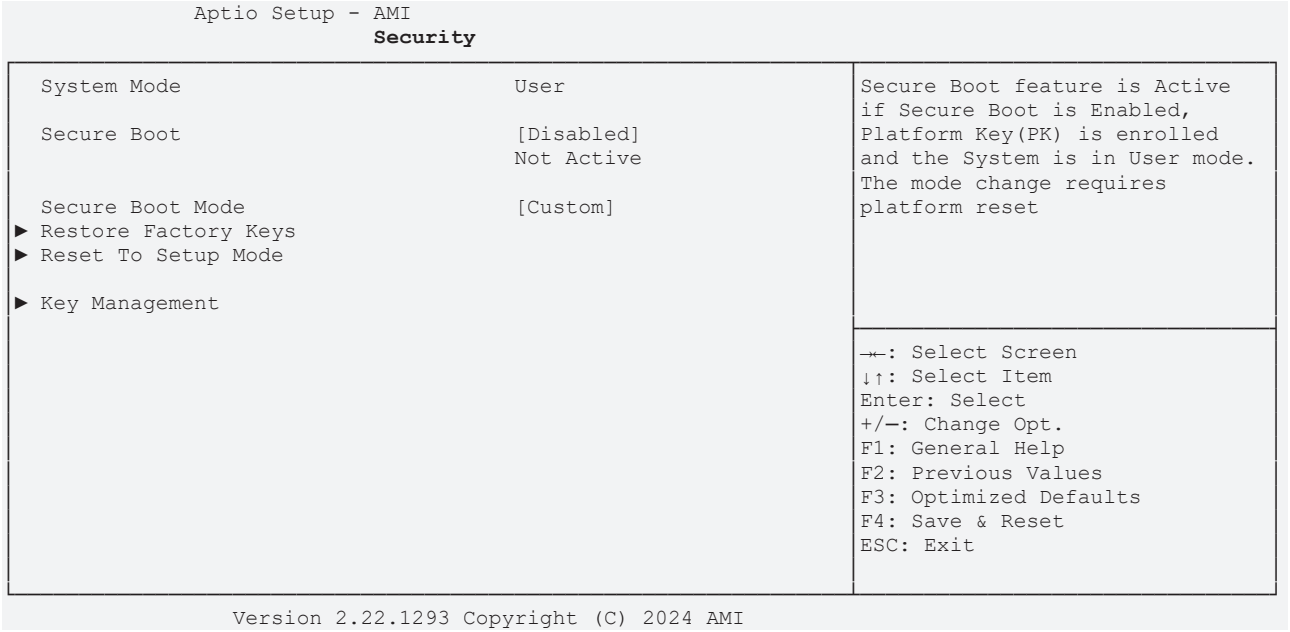
BIOS entry	Options
Icepower IP MFX sub module	Disabled / Enabled
Icepower IP EFX sub module	Disabled / Enabled
Icepower IP SFX sub module	Disabled / Enabled
Voice Preprocessing	Disabled / Enabled
Acoustic Context Awareness (ACA	Disabled / Enabled
Custom Module 'Alpha'	Disabled / Enabled
Custom Module 'Beta'	Disabled / Enabled
Custom Module 'Gamma'	Disabled / Enabled

7.5 Security



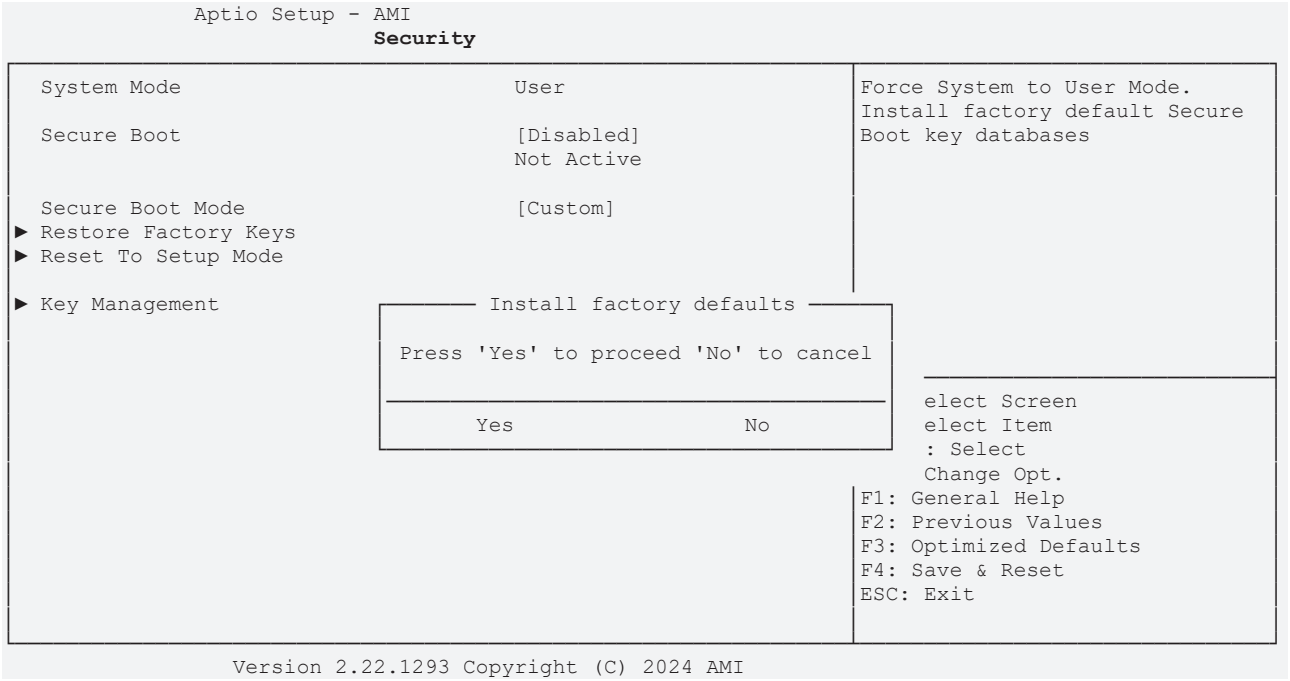
BIOS entry	Options
Password Description	
Minimum length	None
Maximum length	None
Administrator Password	Set an administrator password here.
User Mode available	Enabled / Disabled
Secure Boot	Submenu see: Secure Boot [▶ 96]

7.5.1 Secure Boot



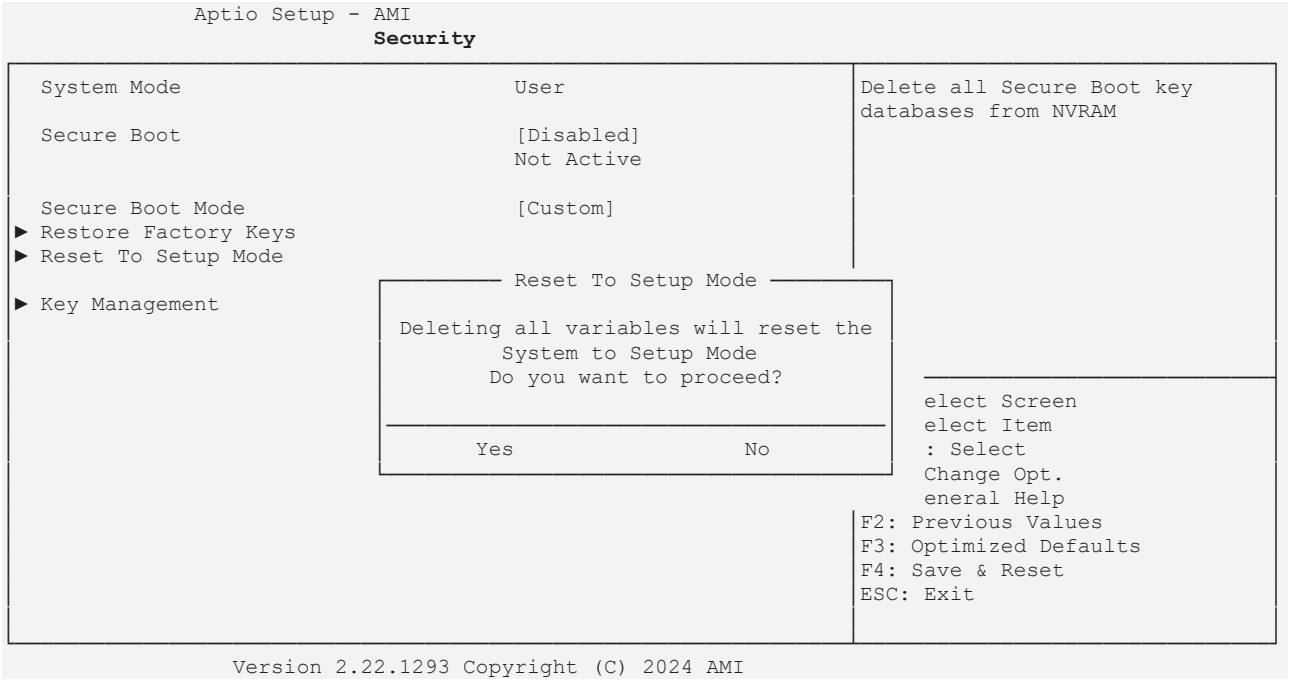
BIOS entry	Options
System Mode	None
Secure Boot	Disabled / Enabled Not Active
Secure Boot Mode	Custom / Standard
Restore Factory Keys	Submenu see: Restore Factory Keys [▶ 97]
Reset To Setup Mode	Submenu see: Reset To Setup Mode [▶ 98]
Key Management	Submenu see: Key Management [▶ 99]

7.5.1.1 Restore Factory Keys



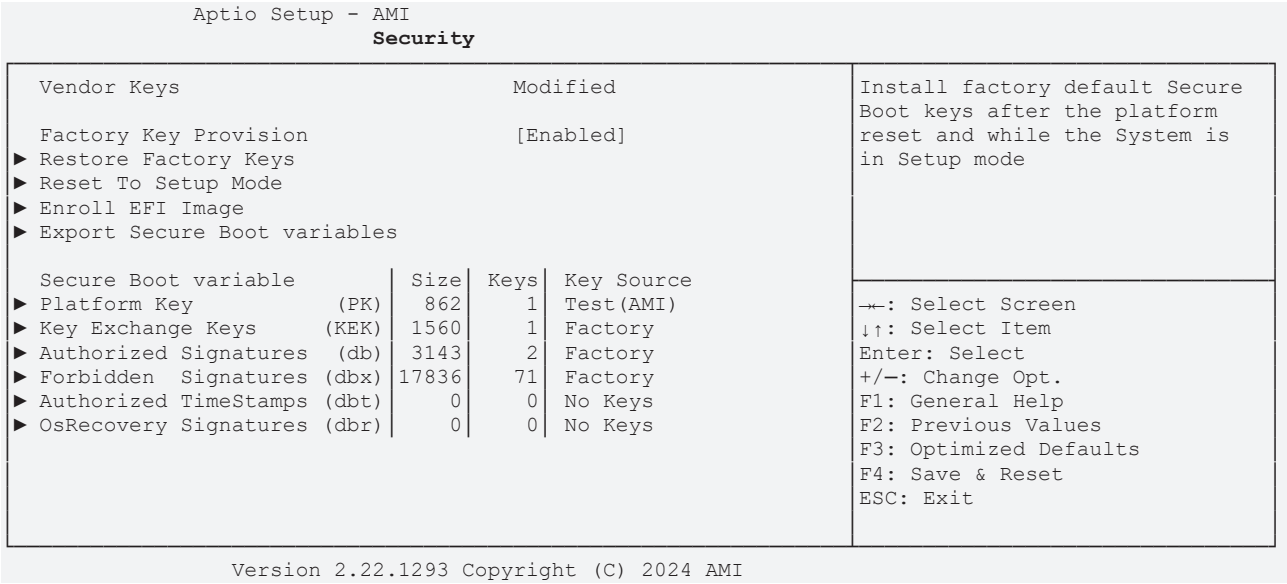
BIOS entry	Options
System Mode	None
Secure Boot	Disabled / Enabled
Secure Boot Mode	Custom / Standard
Restore Factory Keys	Install factory defaults, see box

7.5.1.2 Reset To Setup Mode



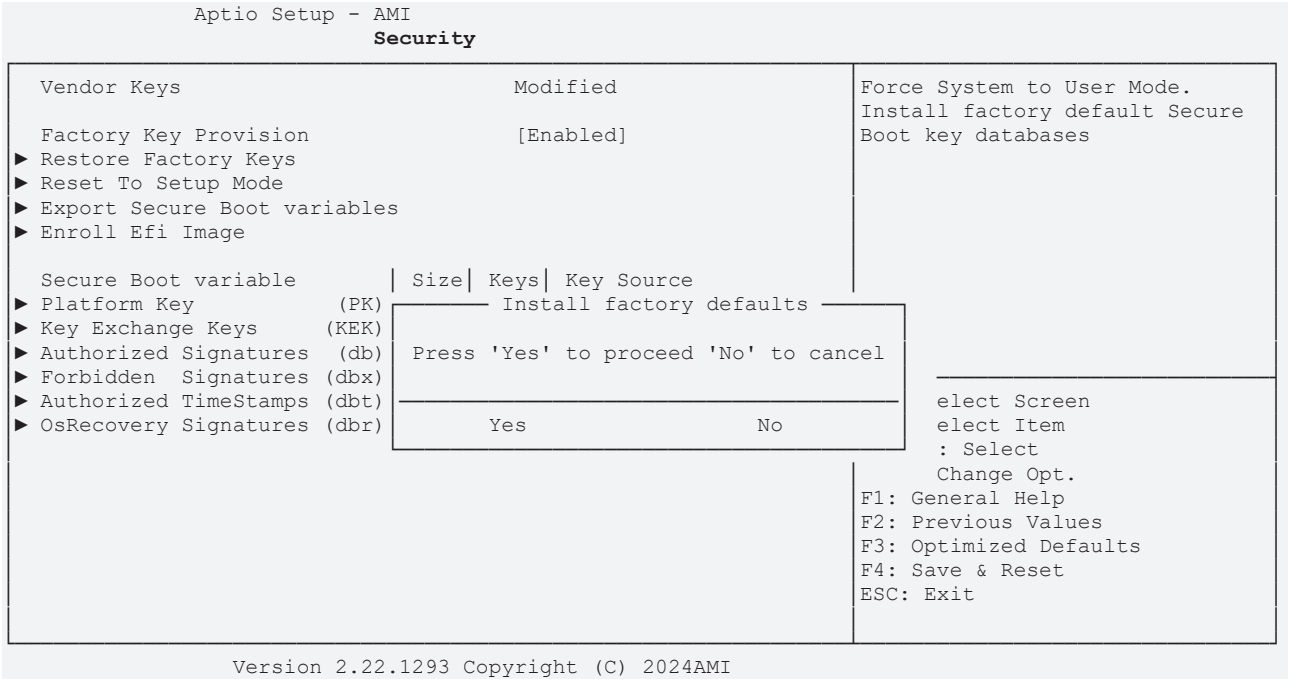
BIOS entry	Options
System Mode	none
Secure Boot	Disabled / Enabled Not Active
Secure Boot Mode	Custom / Standard
Reset To Setup Mode	Reset To Setup Mode, see box

7.5.1.3 Key Management



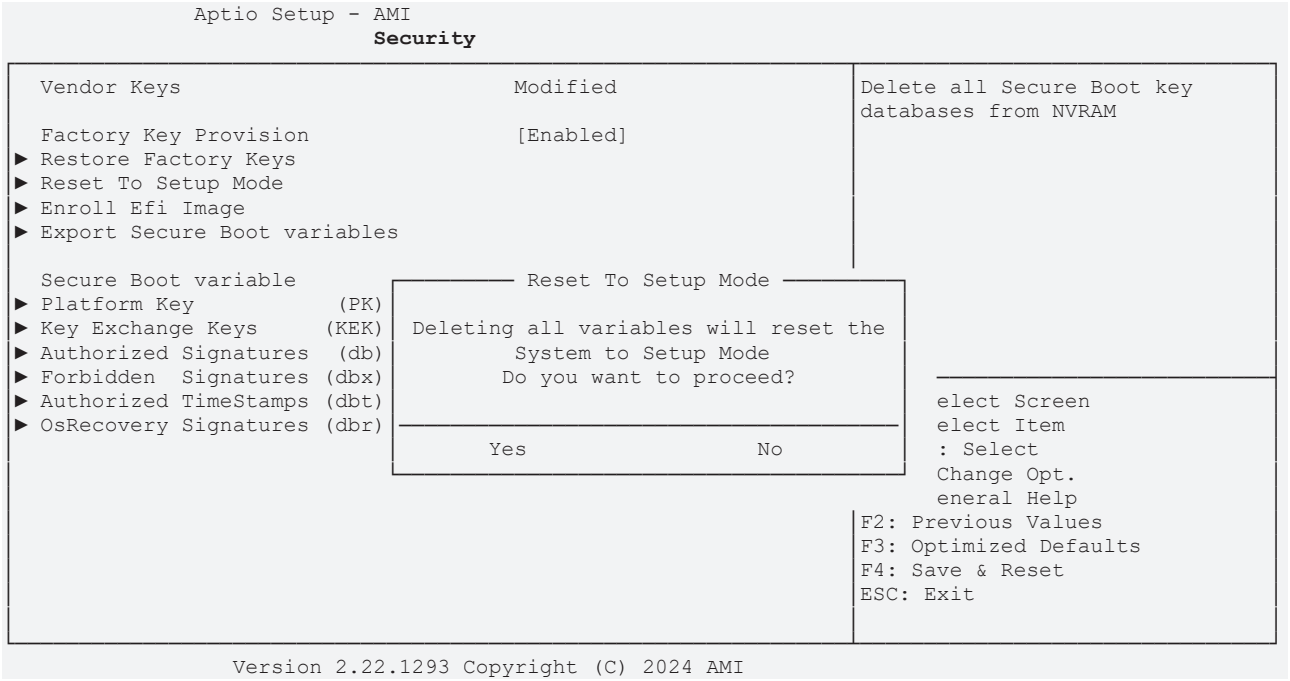
BIOS entry	Options
Vendor Keys	None
Factory Key Provision	Disabled / Enabled
Restore Factory Keys	Submenu see: Restore Factory Keys [▶ 100]
Reset To Setup Mode	Submenu see: Reset To Setup Mode [▶ 101]
Enroll Efi Image	Submenu see: Enroll Efi Image [▶ 102]
Export Secure Boot variables	Submenu see: Export Secure Boot variables [▶ 102]
Secure Boot variables	
PlatformKey(PK)	Press enter key
Key Exchange Keys (KEK)	Press enter key
Authorized Signatures (db)	Press enter key
Forbidden Signatures (dbx)	Press enter key
Authorized TimeStamps (dbt)	Press enter key
OsRecovery Signatures (dbr)	Press enter key

7.5.1.3.1 Restore Factory Keys



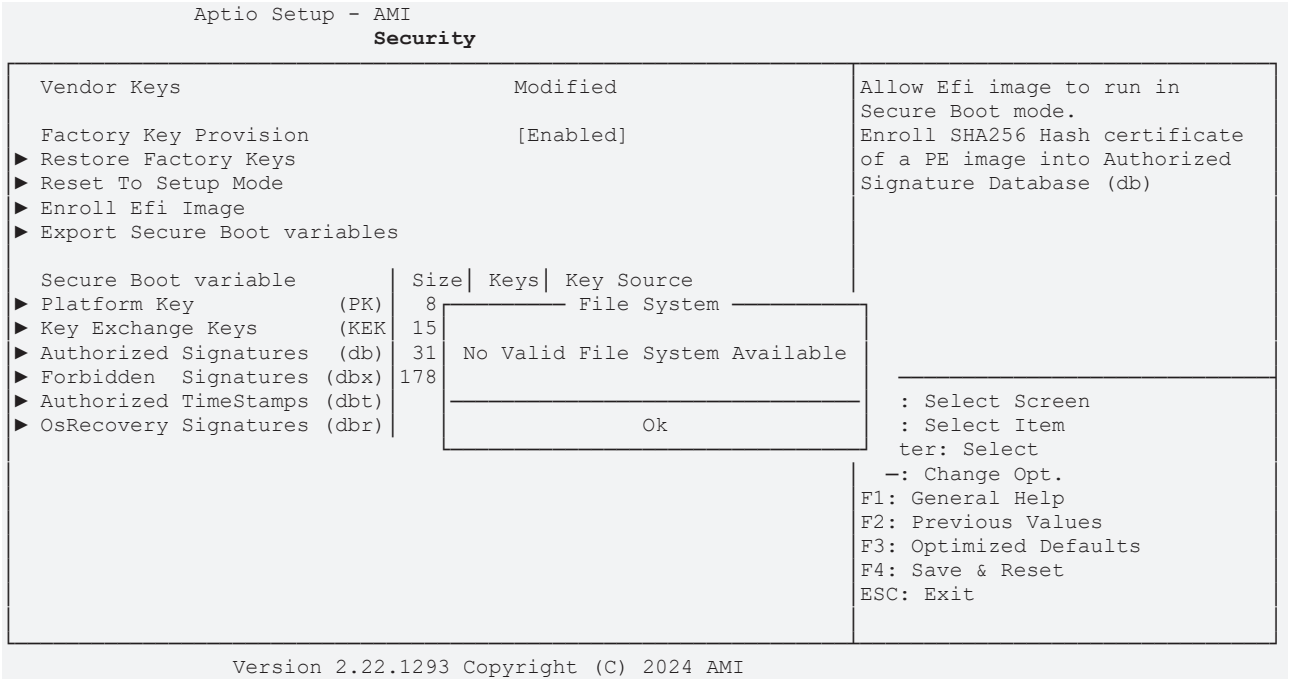
BIOS entry	Options
Vendor Keys	None
Restore Factory Keys	Restore Factory Keys, see box

7.5.1.3.2 Reset To Setup Mode



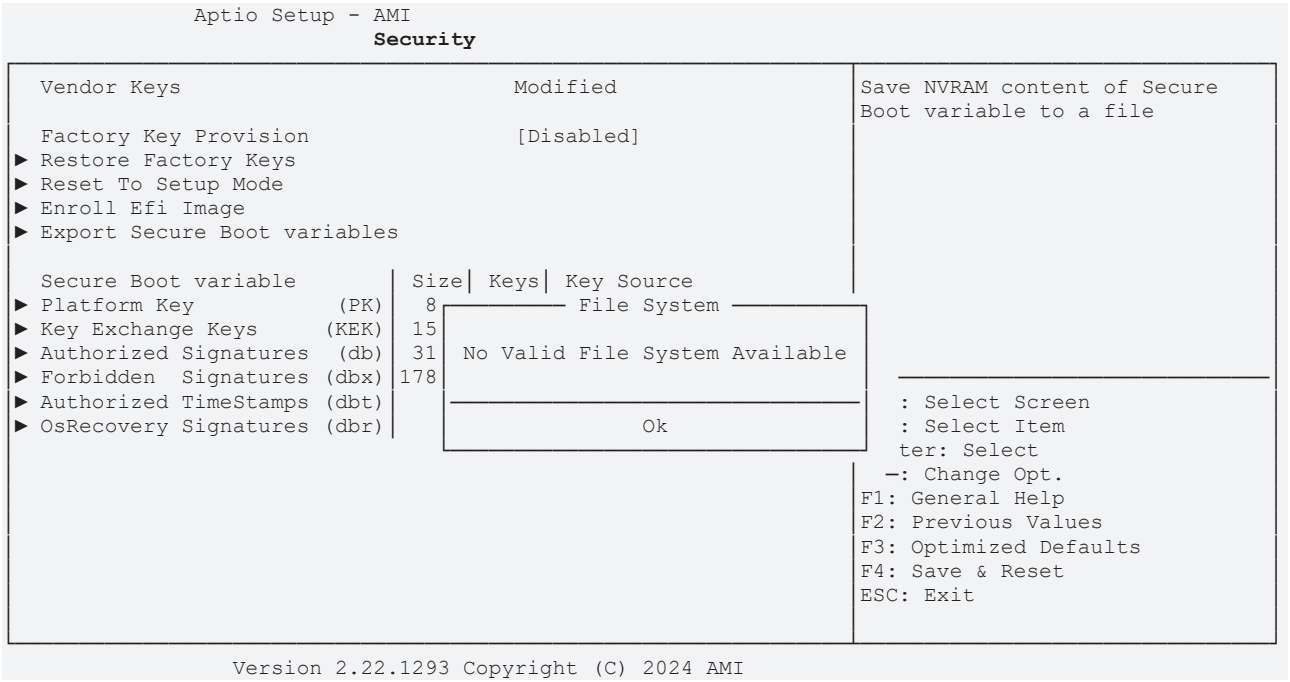
BIOS entry	Options
Vendor Keys	None
Reset To Setup Mode	Reset To Setup Mode, see box

7.5.1.3.3 Enroll Efi Image



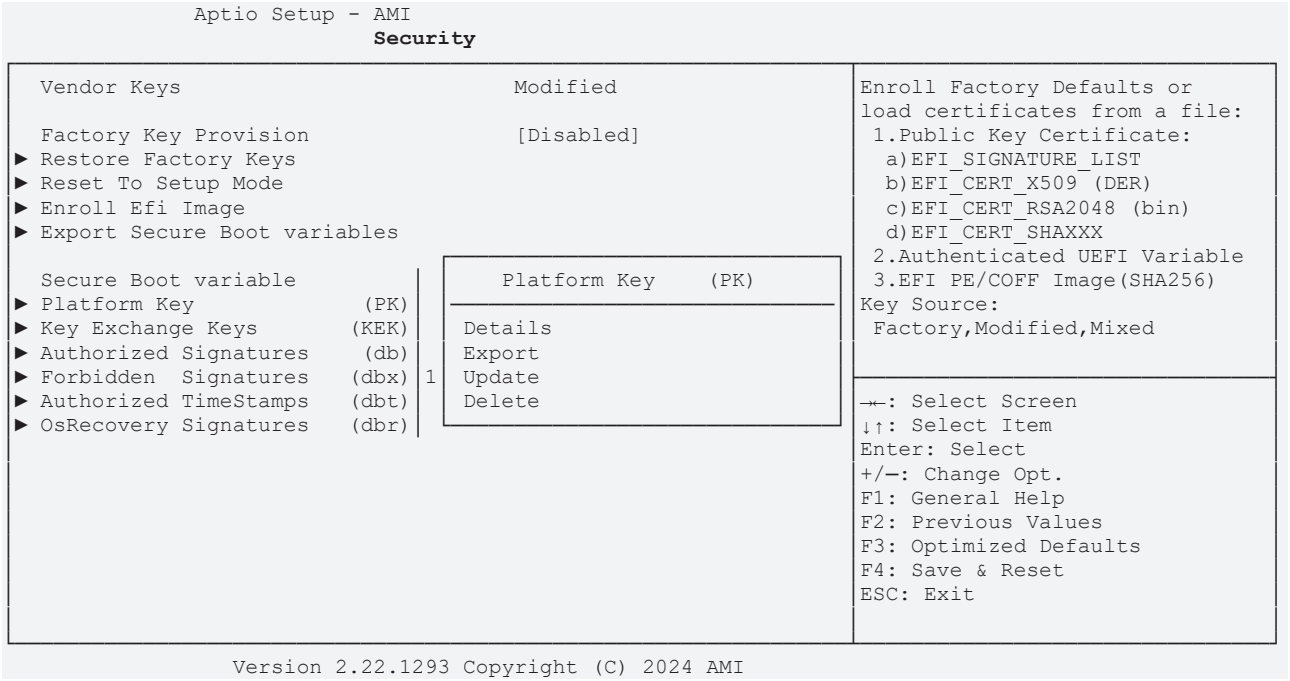
BIOS entry	Options
Vendor Keys	None
Enroll Efi Image	File System, see box

7.5.1.3.4 Export Secure Boot variables



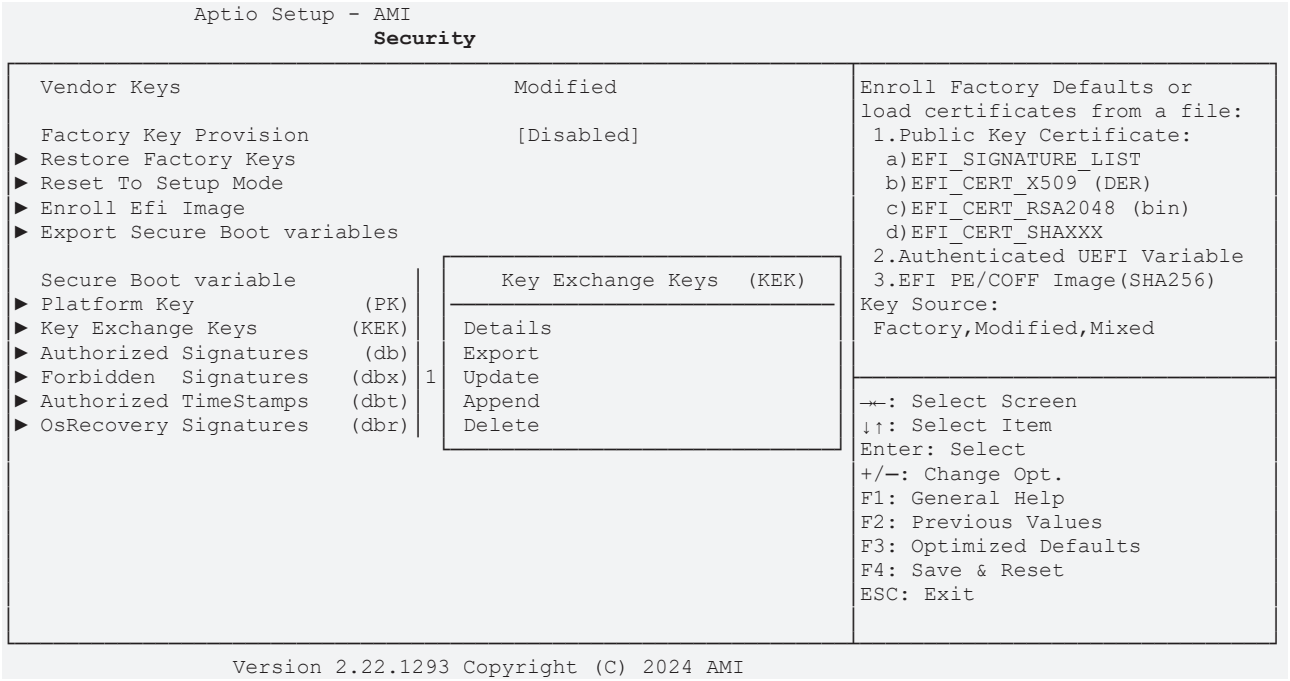
BIOS entry	Options
Vendor Keys	None
Export Secure Boot variables	File System, see box

7.5.1.3.5 Platform Key (PK)



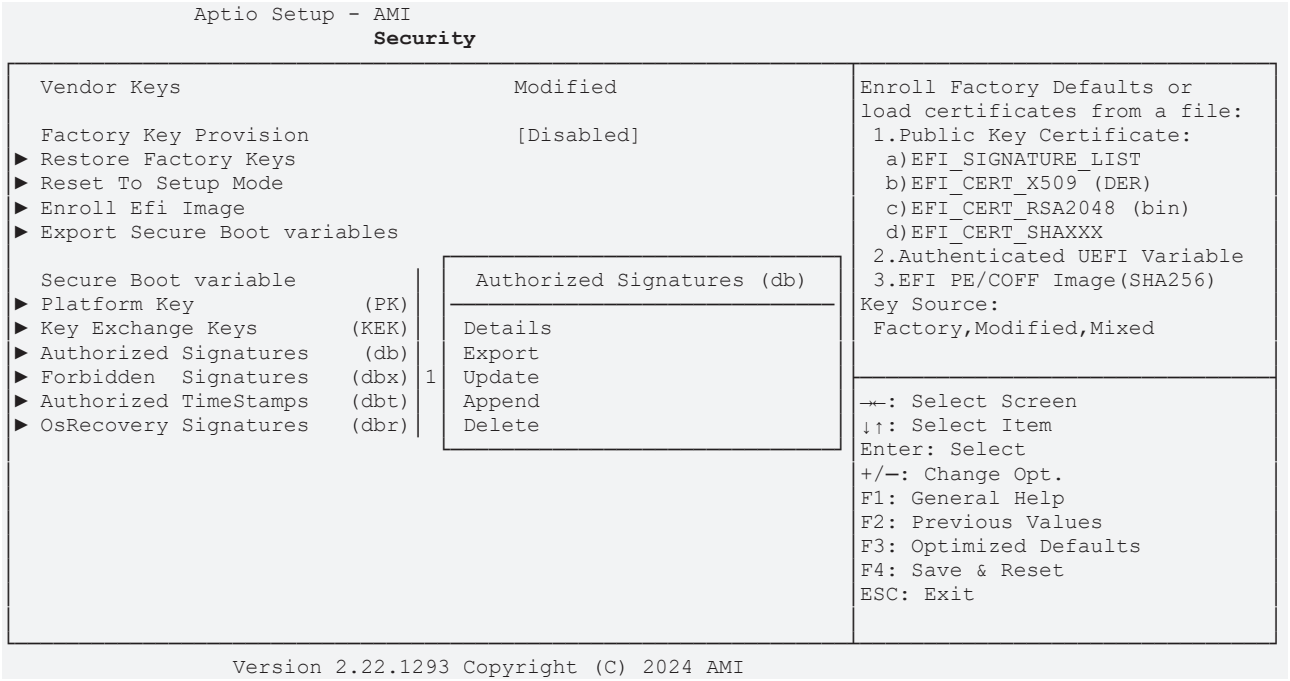
BIOS entry	Options
Vendor Keys	None
Platform Key (PK)	Platform Key (PK), see box

7.5.1.3.6 Key Exchange Keys



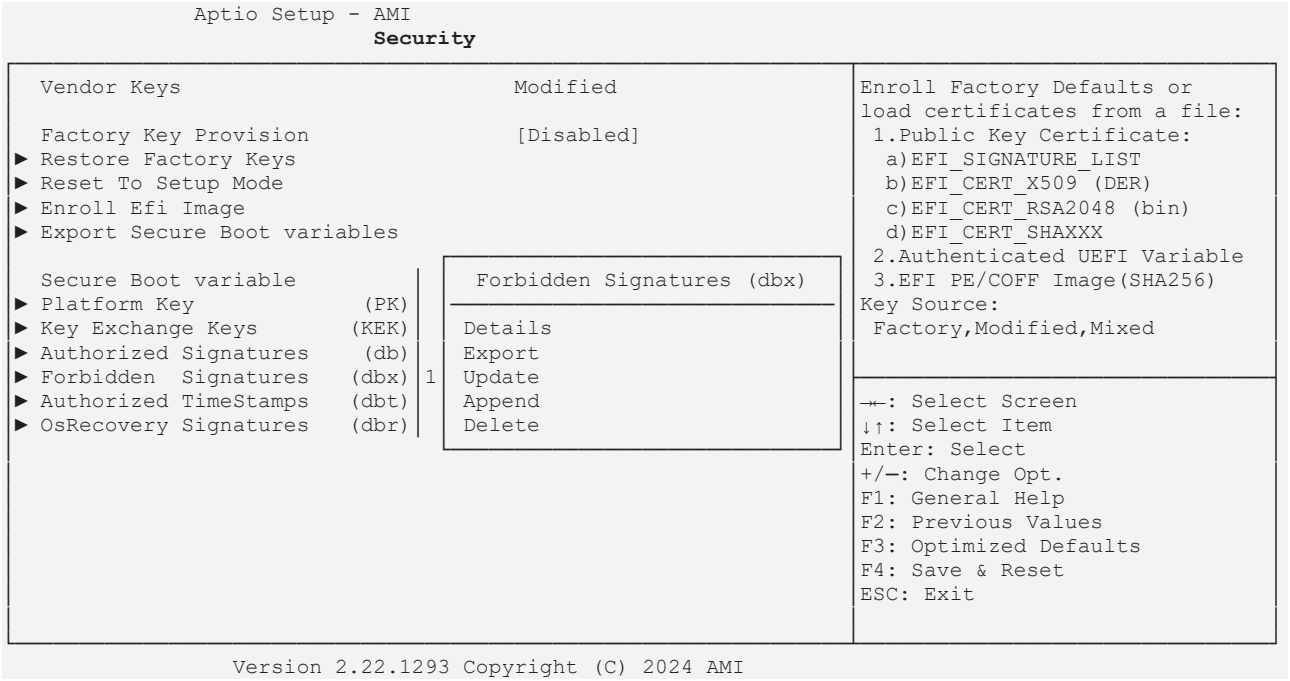
BIOS entry	Options
Vendor Keys	None
Key Exchange Keys	Key Exchange Keys, see box

7.5.1.3.7 Authorized Signatures



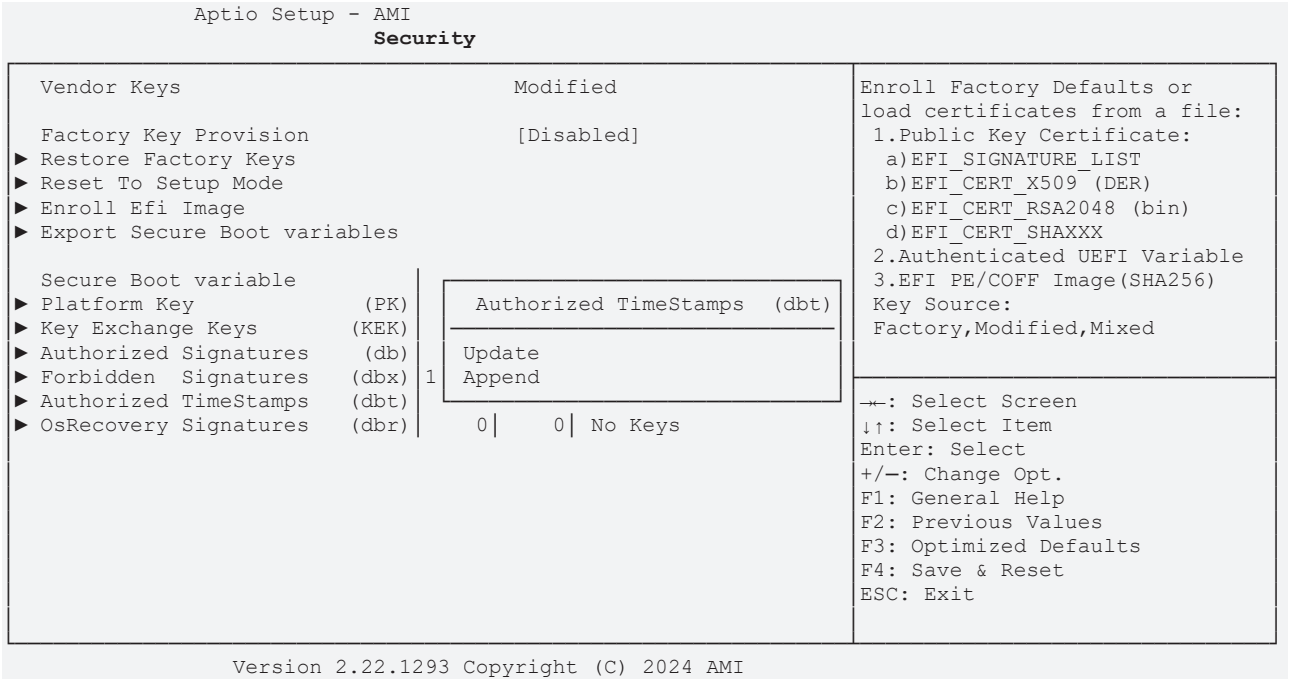
BIOS entry	Options
Vendor Keys	None
Authorized Signatures	Authorized Signatures, see box

7.5.1.3.8 Forbidden Signatures



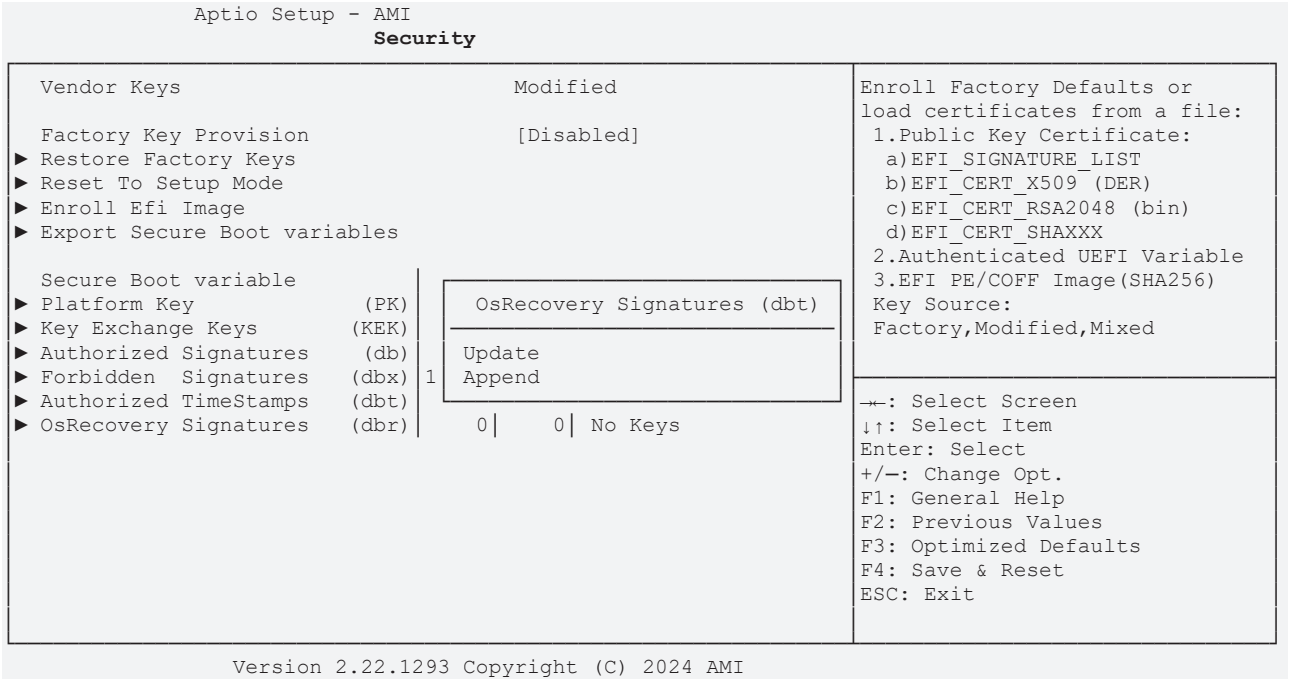
BIOS entry	Options
Vendor Keys	None
Forbidden Signatures	Forbidden Signatures, see box

7.5.1.3.9 Authorized TimeStamps



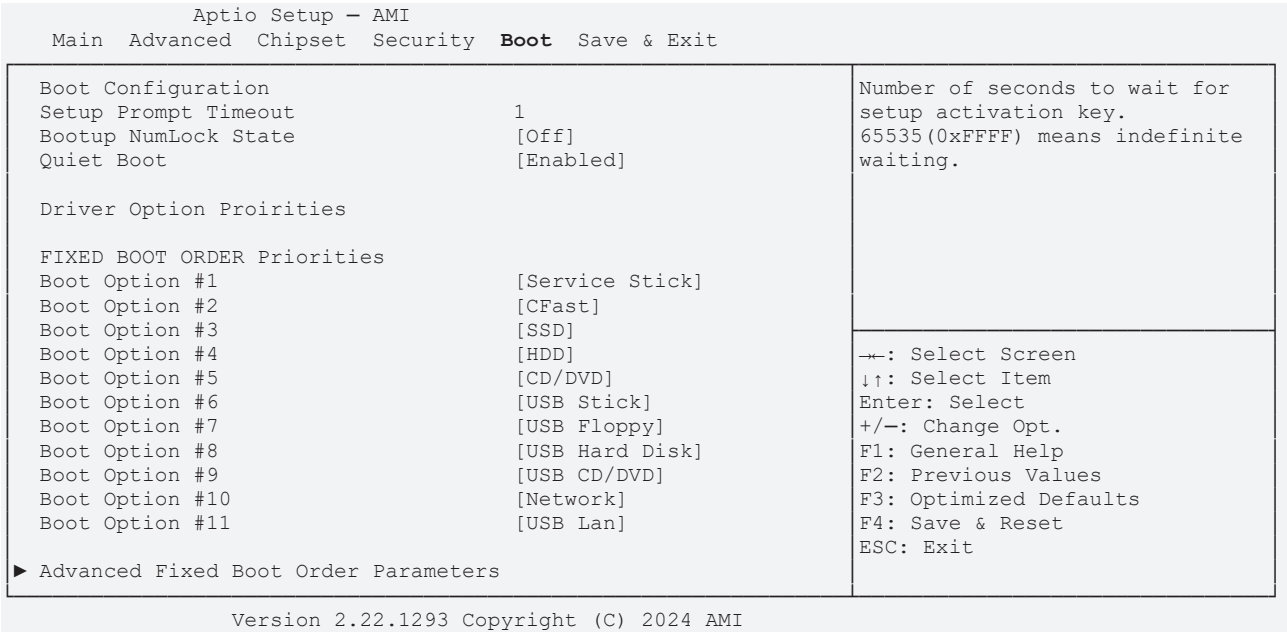
BIOS entry	Options
Vendor Keys	None
Authorized TimeStamps	Authorized TimeStamps, see box

7.5.1.3.10 OsRecovery Signatures



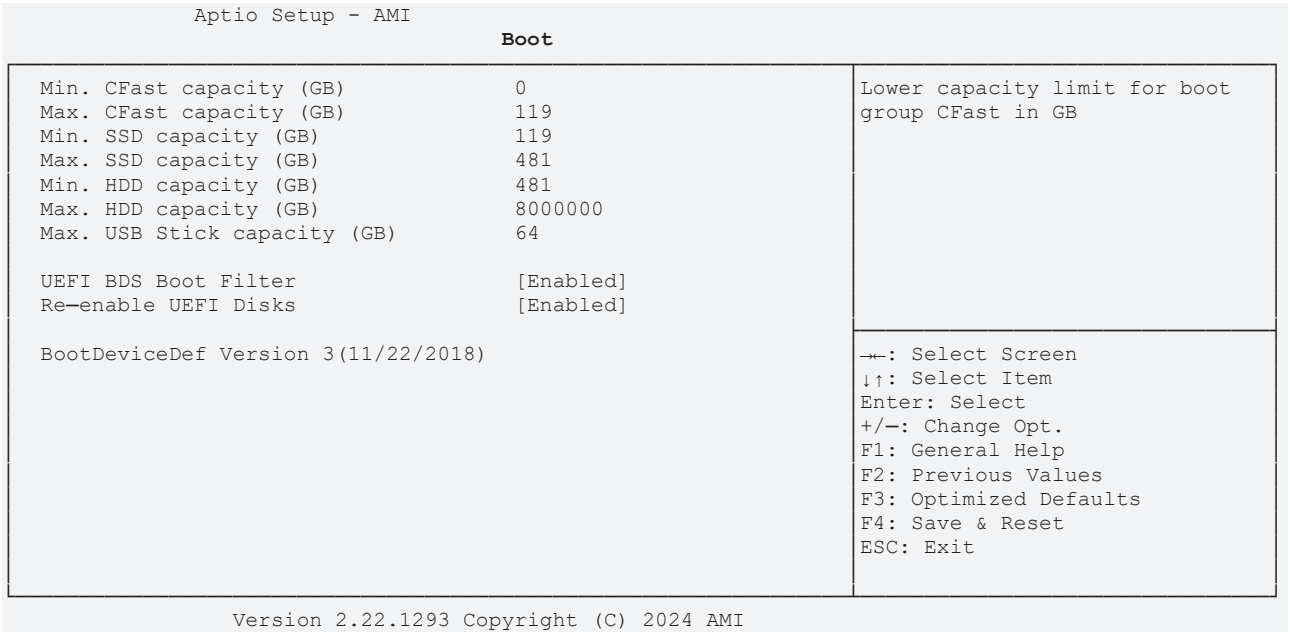
BIOS entry	Options
Vendor Keys	None
OsRecovery Signatures	OsRecovery Signatures, see box

7.6 Boot



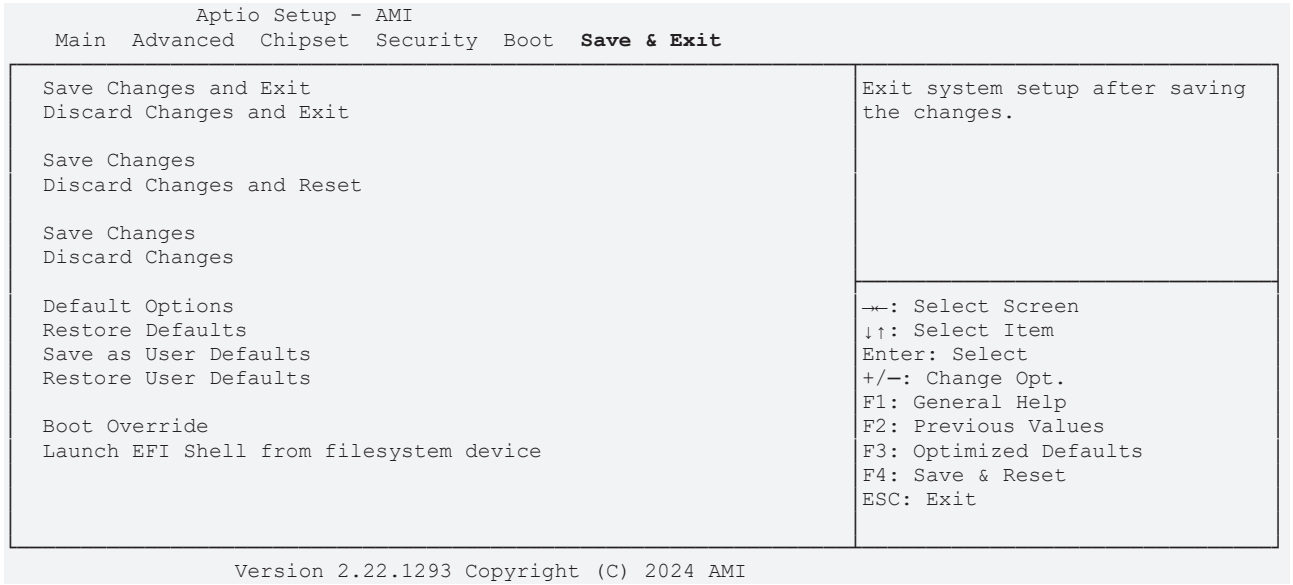
BIOS entry	Options
Boot Configuration	
Setup Prompt Timeout	None
Bootup NumLok State	On / Off
Quiet Boot	Enabled / Disabled
Driver Option Priorities	
Fixed Boot Order Priorities	
Boot Option #1 - 11	Here you can set the order of the boot media to be used.
Advanced Fixed Boot Order Parameters	Submenu see: Advanced Fixed Boot Order Parameters [▶ 110]

7.6.1 Advanced Fixed Boot Order Parameters



BIOS entry	Options
Min. CFast capacity (GB)	None
Max. CFast capacity (GB)	None
Min. SSD capacity (GB)	None
Max. SSD capacity (GB)	None
Min. HDD capacity (GB)	None
Max. HDD capacity (GB)	None
Max. USB Stick capacity (GB)	None
UEFI BDS Boot Filter	Enabled / Disabled
Re-enable UEFI Disks	Enabled / Disabled
BootDeviceDef Version 3(11/22/2018)	

7.7 Save & Exit



BIOS entry	Options
Save Options	
Save Changes and Exit	Press enter key
Discard Changes and Exit	Press enter key
Save Changes	Press enter key
Discard Changes and Reset	Press enter key
Save Changes	Press enter key
Discard Changes	Press enter key
Default Options	
Restore Optimized Defaults	Press enter key
Save as User Defaults	Press enter key
Restore as User Defaults	Press enter key
Boot Override	
Launch EFI Shell from filesystem device	Press enter key

8 Mechanical drawings

8.1 PCB: dimensions

Fig. 25: CB1076 MZ

8.2 PCB: mounting holes

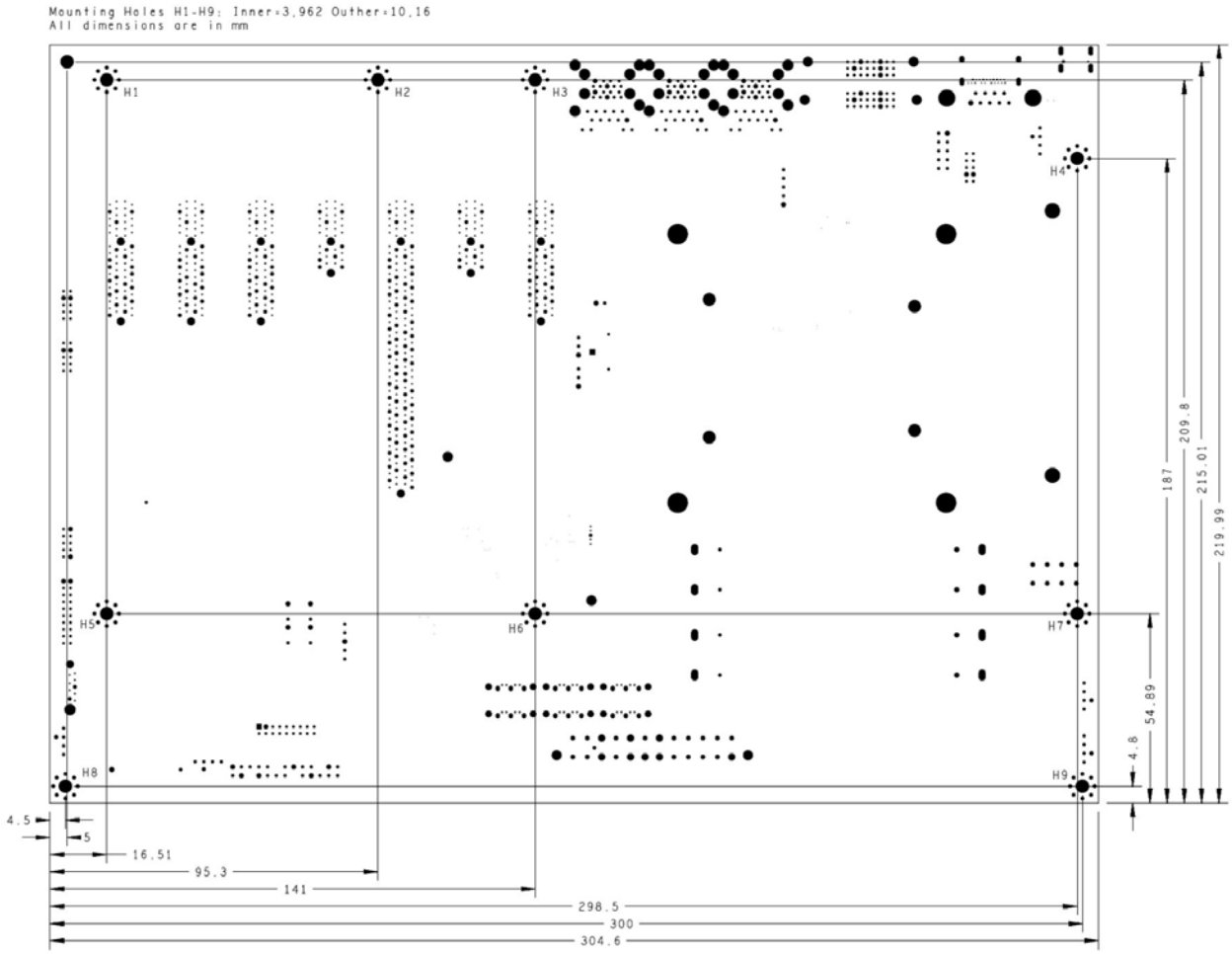


Fig. 26: CB1076 MZ-MH

9 Technical data

9.1 Electrical data

Power supply	
Board	24 VDC power supply (+20 % / - 15 %)
RTC	≥3 A
Power	
Transformer	95 W continuous load 150 W peak load
Current consumption	
RTC	≤ 10 µm

9.2 Environmental conditions

Temperature range	
Operating	0 °C to +60 °C (extended temperature range on request)
Storage	-25 °C ... +85 °C
Shipping	-25 °C ... +85 °C, for packed boards
Temperature changes	
Operating	0.5 °C per minute, 7.5 °C in 30 minutes
Storage	1.0 °C per minute
Shipping	1.0 °C per minute, for packed boards
Relative humidity	
Operating	5 % ... 85 % (non-condensing)
Storage	5 % ... 95 % (non-condensing)
Shipping	5 % ... 100 % (non-condensing), for packed boards
Impact	
Operating	150 m/s², 6 ms
Storage	400 m/s², 6 ms
Shipping	400 m/s², 6 ms, for packed boards
Vibration	
Operating	10 ... 58 Hz, amplitude 0.075 mm
Storage	5 to 9 Hz, 3.5 mm amplitude 9 to 500 Hz, 10 m/s²
Shipping	5 ... 9 Hz, 3.5 mm amplitude 9 ... 500 Hz, 10 m/s², for packed boards

Note on impact and vibration resistance

The specifications for impact and vibration resistance refer only to the motherboard itself without heat sink, memory module, cabling, etc.

9.3 Technical specifications

The board is specified for an ambient temperature range of 0 °C to +60 °C (extended temperature range on request). In addition, care must be taken that the temperature of the processor die does not exceed 100 °C. To ensure this a suitable cooling concept must be implemented that is oriented to the maximum power consumption of the processor/chipset. It must also be ensured that any existing controllers are included in the cooling concept. The power consumption of these function blocks may be of the same order of magnitude as the power consumption of the processor. The board is prepared with suitable holes for the use of modern cooling solutions. We have a series of compatible cooling components in our range. Your distributor will be pleased to assist you in selecting suitable solutions.

NOTICE

Prevent the maximum die temperature being exceeded!

It is the end customer's responsibility to ensure that the die temperature of the processor does not exceed 100 °C! Continuous overheating can destroy the board!

If the temperature exceeds 100 °C, the ambient temperature needs to be reduced. Ensure sufficient air circulation if necessary.

10 Appendix I: Post Codes

During the boot phase, the BIOS generates a series of status messages (so-called "POST Codes"), which can be output with the help of a suitable reading device (POST Code card). The meanings of the POST Codes are explained in the document "Aptio™ 5.x Status Codes" from American Megatrends®, which is available from the website http://www.ami.com. In addition, the following OEM POST Codes are output:

Code	Description
87h	BIOS-API started
88h	PCA9535 started
89h	PWRCTRL firmware started

11 Appendix II: Resources

11.1 Interrupt

The resources used depend on the setup setting. The listed interrupts and their use are given by the AT compatibility. If interrupts are to be available only on the ISA side, they must be reserved by the BIOS setup. Exclusivity on the PCI side is neither given nor possible.

11.2 PCI-Devices

The PCI devices listed here all exist on the board, including those that are detected and configured by the BIOS. Due to the BIOS setup settings it may be the case that various PCI devices or functions of devices are not activated. If devices are disabled, the bus numbers of other devices may change as a result.

Bus	Dev.	Fct.	Controller / Slot
00	00	00	Host Bridge ID 3E30
00	01	00	PCI-to- PCI Bridge ID1901
00	01	01	PCI-to- PCI Bridge ID1905
00	01	02	PCI-to- PCI Bridge ID1909
00	02	00	VGA Controller ID3E98
00	08	00	System Device ID1911
00	12	00	Data Acquisition/Signal Processing Controller ID A379
00	14	00	XHCI USB Controller ID A36D
00	14	02	RAM Controller ID A36F
00	16	00	Communication Device ID A360
00	16	03	Serial Device ID A363
00	17	00	RAID Controller ID 2822
00	1D	00	PCI-to-PCI Bridge ID A330
00	1D	04	PCI-to-PCI Bridge ID A334
00	1F	02	ISA Bridge ID A306
00	1F	03	HD Audio Device ID A348
00	1F	04	SMBus Controller ID A323
00	1F	05	Controller ID A324
00	1F	06	Ethernet Controller ID 15BB
01	00	00	Ethernet Controller (PCIE) ID 1533
02	00	00	Ethernet Controller (PCIE) ID 1533
03	00	00	Ethernet Controller (PCIE) ID 1533

11.3 SMB-Devices

The following table lists the reserved SM-Bus device addresses in 8-bit notation.

NOTICE

These address ranges may not be used by external devices even if the component assigned in the table doesn't exist on the motherboard.

Address	Function
34-35	API access to power supply
36-39	Reserved
5C-5D	NCT7491
60-6F	Reserved for DDR4
70-73	POST-Code Output
88-89	Slave address defined by BIOS
A0-A7	Reserved for DDR4
B0-B3	Power controller (access via BIOS-API)
B8-BB	Power controller (access via BIOS-API)

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