Application note

EtherCAT® slave controller

Section I – Technology
(Online at http://www.beckhoff.com)

Section II – Register description
(Online at http://www.beckhoff.com)

Section III – Hardware description
(Online at http://www.beckhoff.com)

Application note – ESC comparison

Feature and register comparison

Version 2.8
Date: 2025-09-15

BECKHOFF

DOCUMENT ORGANIZATION

The Beckhoff EtherCAT Slave Controller (ESC) documentation covers the following Beckhoff ESCs:

- ET1200
- ET1100, ET1150
- EtherCAT IP Core for FPGAs
- ESC20

The documentation is organized in three sections. Section I and section II are common for all Beckhoff ESCs, Section III is specific for each ESC variant.

The latest documentation is available at the Beckhoff homepage (http://www.beckhoff.com).

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Section I – Technology (all ESCs)

Section I deals with the basic EtherCAT technology. Starting with the EtherCAT protocol itself, the frame processing inside EtherCAT slaves is described. The features and interfaces of the physical layer with its two alternatives Ethernet and EBUS are explained afterwards. Finally, the details of the functional units of an ESC like FMMU, SyncManager, distributed clocks, slave information interface, interrupts, watchdogs, and so on, are described.

Since section I is common for all Beckhoff ESCs, it might describe features which are not available in a specific ESC. Refer to the feature details overview in section III of a specific ESC to find out which features are available.

Section II – Register description (all ESCs)

Section II contains detailed information about all ESC registers. This section is also common for all Beckhoff ESCs, thus registers, register bits, or features are described which might not be available in a specific ESC. Refer to the register overview and to the feature details overview in section III of a specific ESC to find out which registers and features are available.

Section III – Hardware description (specific ESC)

Section III is ESC-specific and contains detailed information about the ESC features, implemented registers, configuration, interfaces, pinout, usage, electrical and mechanical specification, and so on. Especially the process data interfaces (PDI) supported by the ESC are part of this section.

Additional documentation

Application notes and utilities can also be found at the Beckhoff homepage. Pinout configuration tools for EtherCAT ASICs are available. Additional information on EtherCAT IP cores with latest updates regarding design flow compatibility, FPGA device support and known issues are also available.

DOCUMENT HISTORY

Version	Comment
1.0	Initial release
1.1	• EtherCAT mode and slave category added • Enhanced link detection compatibility added • Editorial changes
1.2	• Different versions of ESCs added to comparison • Update to EtherCAT IP core release V2.2.0/V2.02a • ESC DL control register address corrected • ET1100: register 0x0980 is only available if DC sync unit is enabled (0x0140.10=1) • IP cores: physical read/write offset (0x0108:0x0109) is configurable • ESC10 removed • Editorial changes
1.3	• Added EtherCAT IP core for Altera FPGAs V2.2.1 • Editorial changes
1.4	• Update to ET1100-0002 and ET1200-0002 • Editorial changes
1.5	• Update to EtherCAT IP core for Altera FPGAs V2.3.0, update to EtherCAT IP core for Xilinx FPGAs V2.03a • Editorial changes
1.6	• Update to EtherCAT IP core for Altera FPGAs V2.3.1, update to EtherCAT IP core for Xilinx FPGAs V2.03b
1.7	• Removed enhanced link detection EBUS support for ET1100/ET1200 • Update to EtherCAT IP core for Altera FPGAs V2.3.2, update to EtherCAT IP core for Xilinx FPGAs V2.03c
1.8	• Update to EtherCAT IP core for Altera FPGAs V2.4.0, update to EtherCAT IP core for Xilinx FPGAs V2.04a • Added optional LED features • Added FPGA design tool compatibility
1.9	• Updated FPGA design tool compatibility
2.0	• Update to EtherCAT IP core for Altera FPGAs V3.0.2, update to EtherCAT IP core for Xilinx FPGAs V3.00c • Update to ET1100-0003 and ET1200-0003 • Removed FPGA design tool compatibility (moved to data sheet addendum)
2.1	• Update to EtherCAT IP core for Altera FPGAs V2.4.3, update to EtherCAT IP core for Xilinx FPGAs V2.04d
2.2	• Update to EtherCAT IP core for Altera FPGAs V3.0.5, update to EtherCAT IP core for Xilinx FPGAs V3.00f
2.3	• Update to EtherCAT IP core for Altera FPGAs V3.0.6, update to EtherCAT IP core for Xilinx FPGAs V3.00g
2.4	• Editorial changes
2.5	• Update to EtherCAT IP core for Altera FPGAs V3.0.9, update to EtherCAT IP core for Xilinx FPGAs V3.00j
2.6	• Update to EtherCAT IP core for Altera FPGAs V2.4.4 and V3.0.10, update to EtherCAT IP core for Xilinx FPGAs V2.04e and V3.00k
2.7	• Added IP core option names to register table, revised distributed clocks alternatives • Altera is now Intel • Editorial changes
2.8	• Update to EtherCAT IP core FPGAs V4.0.0 • Editorial changes

1 Overview

This application note provides an overview of the features and available registers of the following Beckhoff EtherCAT slave controllers:

- ET1200-0003
- ET1100-0003
- ET1150-0002
- EtherCAT IP core for Altera® FPGAs (up to V4.0.0)
- EtherCAT IP core for AMD® FPGAs (up to V4.0.0)
- EtherCAT IP core for Lattice® FPGAs (up to V4.0.0)
- ESC20 (Build 22)

Refer to the ESC data sheets for further information. The ESC data sheets are available from the Beckhoff homepage (http://www.beckhoff.com).

Table 1: ESC main features

Feature	ET1200	ET1100	ET1150	IP core (latest)	ESC20
Ports	2-3 (each EBUS/MII, max. 1xMII)	2-4 (each EBUS/MII)	1-4 (each MII/RGMII)	1-4 MII or 1-4 RGMII or 1-4 RMII	2 MII
FMMUs	3	8	16	0-16	4
SyncManagers	4	8	16	0-16	4
RAM [Kbyte]	1	8	15	0-60	4
Distributed Clocks	64 bit	64 bit	64 bit	32/64 bit	32 bit
Process data interfaces	1	1	2	2	1
Digital I/O	16 bit	32 bit	32 bit	8-32 bit	32 bit
SPI slave	Yes	Yes	Yes	Yes	Yes
SPI master	-	-	Yes	-	-
µController	-	8/16 bit async/sync	8/16/32 bit async/sync	8/16 bit async	8/16 bit async
On-chip bus	-	-	-	Avalon® AMBA AXI4™ AMBA AXI4 LITE™	-

2 ESC features

Table 2: ESC features

Feature	ET1200 -0003	ET1150	ET1100 -0003	IP core V4.0.0	IP core Altera® V3.0.10	IP core Altera® V3.0.0-3.0.9	IP core Altera® V2.4.4	IP core Altera® V2.4.3	IP core Altera® V2.4.0	IP core Altera V2.3.1/ V2.3.2	IP core Altera V2.3.0	IP core Altera V2.2.1	IP core Altera V2.2.0	IP core Altera V2.0.0	IP core Altera V1.1.1	IP core Altera V1.1.0	IP core Altera V1.0.0	IP core Xilinx® V3.00k	IP core Xilinx® V3.00c-3.00j	IP core Xilinx® V2.04e	IP core Xilinx V2.04d	IP core Xilinx V2.04a	IP core Xilinx V2.03d	IP core Xilinx V2.03b/c	IP core Xilinx V2.03a	IP core Xilinx V2.02a	IP core Xilinx V2.00a	IP core Xilinx V1.01b	ESC20
EtherCAT ports	2-3	1-4	2-4	1-4	1-3	1-3	1-3	1-3	1-3	1-3	1-3	2-3	2-3	2	2	2	2	1-3	1-3	1-3	1-3	1-3	1-3	1-3	2-3	2	2	2
Permanent ports	2	1-4	2-4	1-4	1-3	1-3	1-3	1-3	1-3	1-3	1-3	2-3	2-3	2	2	2	2	1-3	1-3	1-3	1-3	1-3	1-3	1-3	2-3	2	2	2
Optional bridge port 3 (EBUS or MII)	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EBUS ports	1-3	0	0-4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
MII ports	0-1	0-4	0-4	0-4	0-3	0-3	0-3	0-3	0-3	0-3	0-3	0/2/3	0/2/3	0/2	0/2	0/2	0/2	0-3	0-3	0-3	0-3	0-3	0-3	0-3	0/2/3	0/2	0/2	2
RMII ports	-	-	-	0-4	0-2	0-2	0-2	0-2	0-2	0-2	0-2	0/2	0/2	0/2	0/2	0/2	0/2	0-2	0-2	0-2	0-2	0-2	0-2	0-2	0/2	0/2	0/2	-
RGMII ports	-	-	-	0-4	0-3	0-3	-	-	-	-	-	-	-	-	-	-	-	0-3	0-3	-	-	-	-	-	-	-	-	-
Port 0	-	x	-	x	x	x	x	x	x	x	x	-	-	-	-	-	-	x	x	x	x	x	x	x	-	-	-	-
Ports 0, 1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Ports 0, 1, 2	-	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	-	x	x	x	x	x	x	x	x	-	-	-
Ports 0, 1, 3	x	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Ports 0, 1, 2, 3	-	x	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EtherCAT mode	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct	Direct
Slave category	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave	Full slave
Position addressing	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Node addressing	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Logical addressing	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Broadcast addressing	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Physical layer general features																												
FIFO size configurable (0x0100[18:16])	x	x	x	x	x	x	x	x	x	c	c	c	c	c	c	c	c	x	x	x	x	x	c	c	c	c	c	x
FIFO size default from SII EEPROM	-	x	-	x	x	x	x	x	-	-	-	-	-	-	-	-	-	x	x	x	x	-	-	-	-	-	-	-
Auto-forwarder checks CRC and SOF	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Forwarded RX error indication, detection and counter (0x0308:0x030B)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Prevention of circulating frames	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Fallback: port 0 opens if all ports are closed	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
VLAN tag and IP/UDP support	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Enhanced link detection per port configurable	-	x	-	x	x	x	x	x	x	x	x	x	x	-	-	-	-	x	x	x	x	x	x	x	x	-	-	-
EBUS features																												
Low jitter	x		x																									
Enhanced link detection supported	-		-																									
Enhanced link detection compatible	x		x																									
EBUS signal validation	x		x																									
LVDS transceiver internal	x		x																									
LVDS termination internal	-		-																									
LVDS current configuration	RBIAS		RBIAS																									
LVDS sample rate [MHz]	1,000		1,000																									
Remote link down signaling time configurable 0x0100[22]	x		x																									

Feature	ET1200 -0003	ET1150	ET1100 -0003	IP core V4.0.0	IP core Altera® V3.0.10	IP core Altera® V3.0.0-3.0.9	IP core Altera® V2.4.4	IP core Altera® V2.4.3	IP core Altera® V2.4.0	IP core Altera V2.3.1/ V2.3.2	IP core Altera V2.3.0	IP core Altera V2.2.1	IP core Altera V2.2.0	IP core Altera V2.0.0	IP core Altera V1.1.1	IP core Altera V1.1.0	IP core Altera V1.0.0	IP core Xilinx® V3.00k	IP core Xilinx® V3.00c-3.00j	IP core Xilinx® V2.04e	IP core Xilinx V2.04d	IP core Xilinx V2.04a	IP core Xilinx V2.03d	IP core Xilinx V2.03b/c	IP core Xilinx V2.03a	IP core Xilinx V2.02a	IP core Xilinx V2.00a	IP core Xilinx V1.01b	ESC20
General Ethernet features (MII/RMII/RGMII)																													
PHY management interface (0x0510:0x051F)	x	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x
Supported PHY address offsets	0/16	0/1/16/17	0/16	any	any	any	any	any	any	any	any	any	any	any	0/16	0/16	0/16	any	any	any	any	any	any	any	any	any	any	0/16	0
Individual port PHY addresses	-	OTP: x	-	x	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-
Port PHY addresses readable	-	x	-	x	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-
Link polarity configurable	-	x	x	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	-
Enhanced link detection supported	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	-
FX PHY support (native)	-	x	-	x	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-
Fast hot connect support (native)	-	x	-	x	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-
PHY reset out signals	-	FX	-	x	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-
Link detection using PHY signal (LED)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Link detection using RGMII in-band status	-	-	-	x	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-
MI link status and configuration	-	PROM per port	-	c per port	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	-	-	-	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	c all ports	-	-
User MI initialization values	-	OTP: 4	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
MI controllable by PDI (0x0516:0x0517)	-	x	-	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	-
MI read error (0x0510[13])	-	x	-	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	-
MI PHY configuration update status (0x0518[5])	-	x	-	x	x	x	x	x	x	x	x	x	x	-	-	-	-	x	x	x	x	x	x	x	x	x	x	-	-
MI preamble suppression	-	x	-	x	x	x	x	x	x	x	x	-	-	-	-	-	-	x	x	x	x	x	x	x	x	-	-	-	-
Additional MCLK	x	x	x	x	x	x	x	x	x	x	-	-	-	-	-	-	-	x	x	x	x	x	x	x	-	-	-	-	-
Gigabit PHY configuration	-	c	-	x	x	x	x	x	x	-	-	-	-	-	-	-	-	x	x	x	x	x	x	-	-	-	-	-	-
Gigabit PHY register 9 detection	-	full	-	full	relaxed	relaxed	relaxed	relaxed	-	-	-	-	-	-	-	-	-	relaxed	relaxed	relaxed	relaxed	-	-	-	-	-	-	-	-
Clause 45 access	-	x	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Transparent mode	-	c	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
MII features																													
CLK25OUT as PHY clock source	x	x	x	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	-
Bootstrap TX shift settings	x	x	x	c	c	c	c	c	c	c	c	c	c	c	User logic	User logic	User logic	c	c	c	c	c	c	c	c	c	c	-	-
Automatic TX shift setting (with TX_CLK)	-	x	-	x	c	c	c	c	c	c	c	c	c	c	-	-	-	c	c	c	c	c	c	c	c	c	c	-	-
TX shift not necessary (PHY TX_CLK as clock source)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x
FIFO size reduction steps	1	2	1	2	2	2	1	1	1	1	1	1	1	1	1	1	1	2	2	1	1	1	1	1	1	1	1	1	1
MII back-to-back connections	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
PDI general features																													
Internal PDI clock	25 MHz TD	25/50/100/ 200 MHz	25 MHz TD	25/50/ 100 MHz	25 MHz	25 MHz	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz	25 MHz	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD	25 MHz TD
Internal processing data bus width [bits]	8	32	8	8/16/32	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
Extended PDI configuration (0x0152:0x0153)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
CPU_CLK output (10, 20, 25 MHz)	c	c	c	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	-
CPU_CLK2 output and CPU_nRESET_OUT	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SOF, EOF, WD_TRIG and WD_STATE independent of PDI	-	WD_ STATE	-	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	x	-
Available PDIs and PDI features depending on port configuration	x	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PDI selection at run-time (SII EEPROM)	x	c	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x
PDI active immediately (SII EEPROM settings ignored)	-	c	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
PDI function acknowledge by write	-	c	-	c	c	c	-	-	-	-	-	-	-	-	-	-	-	c	c	-	-	-	-	-	-	-	-	-	-
PDI function acknowledge SyncManager/register independently	-	c	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Feature	ET1200 -0003	ET1150	ET1100 -0003	IP core V4.0.0	IP core Altera® V3.0.10	IP core Altera® V3.0.0-3.0.9	IP core Altera® V2.4.4	IP core Altera® V2.4.3	IP core Altera® V2.4.0	IP core Altera V2.3.1/ V2.3.2	IP core Altera V2.3.0	IP core Altera V2.2.1	IP core Altera V2.2.0	IP core Altera V2.0.0	IP core Altera V1.1.1	IP core Altera V1.1.0	IP core Altera V1.0.0	IP core Xilinx® V3.00k	IP core Xilinx® V3.00c-3.00j	IP core Xilinx® V2.04e	IP core Xilinx V2.04d	IP core Xilinx V2.04a	IP core Xilinx V2.03d	IP core Xilinx V2.03b/c	IP core Xilinx V2.03a	IP core Xilinx V2.02a	IP core Xilinx V2.00a	IP core Xilinx V1.01b	ESC20
PDI information register 0x014E:0x014F	-	x	-	x	c	c	-	-	-	-	-	-	-	-	-	-	-	c	c	-	-	-	-	-	-	-	-	-	-	-
Support for two PDIs	-	x	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Digital I/O PDI	**x**	**PDI0, PDI1**	**x**	**PDI0, PDI1**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**
Digital I/O width [bits]	8/16	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	8/16/24/32	32
PDI control register value (0x0140:0x0141)	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	16-20
Control/status signals:	2/0[1,2]	8/0[2]	7/0[2]	7	7	7	7	7	7	7	7	7	7	7	5	5	5	7	7	7	7	7	7	7	7	7	7	7	5	-
LATCH_IN	x[1,2]	x[2]	x[2]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
SOF	x[1,2]	x[2]	x[2]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
OUTVALID	x[1,2]	x[2]	x[2]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
WD_TRIG	x[1,2]	x[2]	x[2]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
OE_CONF	-	x[2]	x[2]	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
OE_EXT	-	x[2]	x[2]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
EEPROM_ Loaded	-	x[2]	x[2]	x	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-	-
WD_STATE	-	-	-	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	x	-	-
EOF	-	-	-	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	x	-	-
OUT_START	-	x[2]	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Granularity of direction configuration [bits]	2	2	2	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
Bidirectional mode	x	x	x	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	- (User logic)	-
Output high-Z if WD expired	x	x	x	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	-
Output 0 if WD expired	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Output with EOF	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Output with DC SyncSignals	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Input with SOF	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Input with DC SyncSignals	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Digital I/O user mode from ECAT	-	x	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Digital input register	-	PDI1	-	PDI1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI slave PDI	**x**	**PDI0, PDI1**	**x**	**PDI0, PDI1**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**
Max. SPI clock [MHz]	6-20 (SPI mode dep.)	50	20	30	30	30	30	30	30	30	30	30	30	30	30	30	6-20 (SPI mode dep.)	30	30	30	30	30	30	30	30	30	30	30	15
SPI modes configurable (0x0150[1:0])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
SPI_IRQ driver configurable (0x0150[3:2])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
SPI_SEL polarity configurable (0x0150[4])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Data out sample mode configurable (0x0150[5])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Busy signaling	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x
Wait state byte(s)	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Number of address extension byte(s)	1	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	any	-
2/4 byte SPI master support	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Extended error detection (read busy violation)	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
IRQ byte 0/1 swap	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI user mode from PDI	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI_IRQ delay	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Status indication	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
EEPROM Loaded signal	x	x	x	x	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-	-
Additional select signals	-	c	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI data width	1	1/2/4/8	1	1/2/4/8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
SPI data bidirectional	-	c	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SPI master PDI	**-**	**PDI0, PDI1**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**

[1] Shared control/status signals: LATCH_IN/SOF and OUT_VALID/WD_TRIGGER
[2] Availability depending on port configuration

Feature	ET1200 -0003	ET1150	ET1100 -0003	IP core V4.0.0	IP core Altera® V3.0.10	IP core Altera® V3.0.0-3.0.9	IP core Altera® V2.4.4	IP core Altera® V2.4.3	IP core Altera® V2.4.0	IP core Altera V2.3.1/ V2.3.2	IP core Altera V2.3.0	IP core Altera V2.2.1	IP core Altera V2.2.0	IP core Altera V2.0.0	IP core Altera V1.1.1	IP core Altera V1.1.0	IP core Altera V1.0.0	IP core Xilinx® V3.00k	IP core Xilinx® V3.00c-3.00j	IP core Xilinx® V2.04e	IP core Xilinx V2.04d	IP core Xilinx V2.04a	IP core Xilinx V2.03d	IP core Xilinx V2.03b/c	IP core Xilinx V2.03a	IP core Xilinx V2.02a	IP core Xilinx V2.00a	IP core Xilinx V1.01b	ESC20
Asynchronous µController PDI	-	PDI0: 8/16 bit	8/16 bit	PDI0: 8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit	8/16 bit
Extended µC configuration bits 0x0150[7:4], 0x0152:0x0153		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
ADR[15:13] available (000_b if not available)		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
EEPROM_Loaded signal		x	x	x	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-	-
RD polarity configurable (0x0150[7])		x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Read BUSY delay (0x0152[0])		x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-
Write after first edge (0x0152[2])		c	-	c	c	c	c	c	c	c	c	-	-	-	-	-	-	x	x	x	x	x	x	x	x	-	-	-	-	-
Default BUSY state		c	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
ET1100 compatible timing		c	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Synchronous µController PDI	-	PDI0: 8/16 bit	8/16 bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
EEPROM_ Loaded signal		x	x																											
BUSY until access starts		c	-																											
ET1100 compatible timing		c	x																											
Multiplexed asynchronous µController PDI	-	PDI0: 8/16/32 bit PDI1: 8 bit	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Extended µC configuration bits 0x0150[7:4], 0x0152:0x0153		x																												
ADR[15:13] available (000_b if not available)		x																												
EEPROM_Loaded signal		x																												
RD polarity configurable (0x0150[7])		x																												
Read BUSY delay (0x0152[0])		c																												
Default BUSY state		c																												
On-chip bus PDI	-	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Avalon®				- ET1810: x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	-	-	-	-	-	-	-	-	-	
OPB				-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x	x	x	x	x	x	x	x	x	
PLB v4.6				-	-	-	-	-	-	-	-	-	-	-	-	-	-	x	x	x	x	x	x	x	x	-	-	-	-	
AXI3				-	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
AXI4				x	-	-	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-	
AXI4-Lite				x	-	-	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-	
Bus clock [MHz] (N=1,2,3,…)				any	any	any	N*25	N*25	N*25	N*25	N*25	N*25	N*25	N*25	N*25	N*25	25	any	any	N*25	N*25	N*25	N*25	N*25	N*25	N*25	N*25	N*25	N*25	
Data bus width [bits]				8/16/32/64	8/16/32/64	8/16/32/64	8	8	8	8	8	8	8	8	8	8	8	8/16/32/64	8/16/32/64	32	32	32	32	32	32	32	32	32		
Prefetch cycles				1	1	1	1/2/4	1/2/4	1/2/4	1/2/4	1/2/4	1/2/4	1/2/4	1/2/4	1/2/4	4	4	1	1	1/2/4 (OPB)	1/2/4 (OPB)	1/2/4 (OPB)	1/2/4 (OPB)	1/2/4 (OPB)	1/2/4 (OPB)	1/2/4	1/2/4	4		
DC SyncSignals available directly and as IRQ				x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	x		
Bus clock multiplier in register 0x0150[4:0]				x	x	x	x	x	x	x	x	x	x	x	x	-	x	x	x	x	x	x	x	x	x	x	x	x		
EEPROM_ Loaded signal				x	x	x	-	-	-	-	-	-	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-		
EtherCAT bridge (port 3, EBUS/MII)	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port open/closed configurable	-																													
General purpose I/O	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	-
GPO bits	0-12	0-46	0-16	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64				0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64		
GPI bits	-	0-46	0-16	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64				0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64	0/8/16/32/64		
GPIO available independent of PDI or port configuration	-	-	-	x	x	x	x	x	x	x	x	x	x	x				x	x	x	x	x	x	x	x	x	x	x		
GPIO available without PDI	-	x	-	x	x	x	x	x	x	x	x	x	x	x				x	x	x	x	x	x	x	x	x	x	x		
Concurrent access to GPO by ECAT and PDI	x	x	x	x	x	x	x	x	x	x	x	x	x	x				x	x	x	x	x	x	x	x	x	x	x		
Bidirectional GPIO bits	-	x	-	x	-	-	-	-	-	-	-	-	-	-				-	-	-	-	-	-	-	-	-	-	-		

Feature	ET1200 -0003	ET1150	ET1100 -0003	IP core V4.0.0	IP core Altera® V3.0.10	IP core Altera® V3.0.0-3.0.9	IP core Altera® V2.4.4	IP core Altera® V2.4.3	IP core Altera® V2.4.0	IP core Altera V2.3.1/ V2.3.2	IP core Altera V2.3.0	IP core Altera V2.2.1	IP core Altera V2.2.0	IP core Altera V2.0.0	IP core Altera V1.1.1	IP core Altera V1.1.0	IP core Altera V1.0.0	IP core Xilinx® V3.00k	IP core Xilinx® V3.00c-3.00j	IP core Xilinx® V2.04e	IP core Xilinx V2.04d	IP core Xilinx V2.04a	IP core Xilinx V2.03d	IP core Xilinx V2.03b/c	IP core Xilinx V2.03a	IP core Xilinx V2.02a	IP core Xilinx V2.00a	IP core Xilinx V1.01b	ESC20
ESC information																														
Basic information (0x0000:0x0006)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Port descriptor (0x0007)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
ESC features supported (0x0008:0x0009)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Extended ESC feature availability in user RAM (0x0F80 ff.)	-	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	-	x	x	x	x	x	x	x	x	x	x	x	x	-
Write protection (0x0020:0x0031)	x	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x
Data link layer features																														
ECAT reset (0x0040)	x	x	x	c	c	c	c	c	c	c	c	c	c	-	-	-	-	c	c	c	c	c	c	c	c	c	-	-	-	
PDI reset (0x0041)	-	x	-	c	c	c	c	c	c	c	c	c	c	-	-	-	-	c	c	c	c	c	c	c	c	c	-	-	-	
ESC DL control (0x0100:0x0103) bytes	4	4	4	4	4	4	4	4	4	2/4	2/4	2/4	2/4	2/4	2/4	2/4	2	4	4	4	4	4	2/4	2/4	2/4	2/4	2/4	2/4	4	
EtherCAT only mode (0x0100[0])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Temporary loop control (0x0100[1])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
FIFO size configurable (0x0100[18:16])	x	x	x	x	x	x	x	x	x	c	c	c	c	c	c	c	c	x	x	x	x	x	c	c	c	c	c	c	c	x
Configured station address (0x0010:0x0011)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Configured station alias (0x0100[24], 0x0012:0x0013)	x	x	x	x	x	x	x	x	x	c	c	c	c	c	c	c	c	x	x	x	x	x	c	c	c	c	c	c	c	x
Physical read/write offset (0x0108:0x0109)	x	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x
Application layer features																														
Extended AL control/status bits (0x0120[15:5], 0x0130[15:5])	x	x	x	x	x	x	x	x	x	-	-	-	-	-	-	-	-	x	x	x	x	x	-	-	-	-	-	-	-	
AL status emulation (0x0140[8])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
AL status code (0x0134:0x0135)	x	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	-	c	c	c	c	c	c	c	c	c	c	c	c	x
Interrupts																														
ECAT event mask (0x0200:0x0201)	x	x	x	x	x	x	x	x	x	c	c	c	c	c	c	c	c	x	x	x	x	x	c	c	c	c	c	c	c	x
AL event mask (0x0204:0x0207)	x	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x
ECAT event request (0x0210:0x0211)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
AL event request (0x0220:0x0223)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
SyncManager activation changed (0x0220[4])	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	x	
SyncManager watchdog expiration (0x0220[6])	-	x	-	x	x	x	x	x	x	x	x	-	-	-	-	-	-	x	x	x	x	x	x	x	x	-	-	-	-	
DC SYNC interrupt	[1:0]	[3:0]	[1:0]	[3:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]	[1:0]
Error counters																														
RX error counter (0x0300:0x0307)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Forwarded RX error counter (0x0308:0x030B)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
ECAT processing unit error counter (0x030C)	-	x	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-
PDI error counter (0x030D)	-	x	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-
PDI error code (0x030E:0x030F)	-	x	-	x	c	c	c	c	c	c	c	-	-	-	-	-	-	c	c	c	c	c	c	c	c	-	-	-	-	
Lost link counter (0x0310:0x0313)	x	x	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x
Extended RX error counters (0x0314:0x0317)	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
RX error code (0x0320:0x0327)	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PDI clearing error counters	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Feature	ET1200 -0003	ET1150	ET1100 -0003	IP core V4.0.0	IP core Altera® V3.0.10	IP core Altera® V3.0.0-3.0.9	IP core Altera® V2.4.4	IP core Altera® V2.4.3	IP core Altera® V2.4.0	IP core Altera V2.3.1/ V2.3.2	IP core Altera V2.3.0	IP core Altera V2.2.1	IP core Altera V2.2.0	IP core Altera V2.0.0	IP core Altera V1.1.1	IP core Altera V1.1.0	IP core Altera V1.0.0	IP core Xilinx® V3.00k	IP core Xilinx® V3.00c-3.00j	IP core Xilinx® V2.04e	IP core Xilinx V2.04d	IP core Xilinx V2.04a	IP core Xilinx V2.03d	IP core Xilinx V2.03b/c	IP core Xilinx V2.03a	IP core Xilinx V2.02a	IP core Xilinx V2.00a	IP core Xilinx V1.01b	ESC20
Watchdog																														
Watchdog divider configurable (0x0400:0x0401)	x	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x
Watchdog process data	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Watchdog PDI	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Watchdog counter process data (0x0442)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-
Watchdog counter PDI (0x0443)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	-	-	-
Watchdog status (0x0448)	-	x	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SII EEPROM interface (0x0500:0x050F)																														
I²C EEPROM sizes supported	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	16 Kbit-4 Mbit	16 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	1 Kbit-4 Mbit	16 Kbit-4 Mbit
I²C EEPROM size reflected in 0x0502[7]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
EEPROM controllable by PDI	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
EEPROM emulation by PDI	-	x	-	c	c	c	c	c	c	c	c	c	c	c	-	-	-	c	c	c	c	c	c	c	c	c	c	-	-	-
EEPROM emulation CRC error 0x0502[11] PDI writable	-	x	-	x	x	-	x	x	x	x	x	x	x	x	-	-	-	x	-	x	x	x	x	x	x	x	x	-	-	-
Read data bytes (0x0502[6])	8	8	8	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
Internal pull-up resistors for EEPROM_CLK and EEPROM_DATA	x	x	x	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	-
ESC configuration area A	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
ESC configuration area B	-	x	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
I2C base address	0	0	0	0-7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
I2C half speed	-	-	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
FMMUs	3	16	8	0-16	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	4
Bit-oriented operation	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
SyncManagers	4	16	8	0-16	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	4
Watchdog trigger generation for 1 byte Mailbox configuration independent of reading access	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	-	-	x	x	x	x	x	x	x	x	x	x	x	-	-
SyncManager event times (+0x8[7:6])	-	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	-	c	c	c	c	c	c	c	c	c	c	c	-	-
Buffer state (+0x5[7:6])	-	x	-	x	x	x	x	x	x	x	x	-	-	-	-	-	-	x	x	x	x	x	x	x	x	-	-	-	-	-
SyncManager sequential mode	-	x	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
SyncManager deactivation delay	-	x	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Distributed clocks	**x**	**x**	**x**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**c**	**x**
Width	64	64	64	32/64	32/64	32/64	32/64	32/64	32/64	32/64	32/64	32/64	32/64	32	32	32	32	32/64	32/64	32/64	32/64	32/64	32/64	32/64	32/64	32/64	32	32	32	
Sync/Latch signals	1-2[3]	0-8 (0-4 Sync-Signals, 0-4 Latch-Signals)	2	0-8 (0-4 Sync-Signals, 0-4 Latch-Signals)	4 (0-2 Sync-Signals, 0-2 Latch-Signals)	4 (0-2 Sync-Signals, 0-2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (0-2 Sync-Signals, 0- 2 Latch-Signals)	4 (0-2 Sync-Signals, 0- 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	4 (2 Sync-Signals, 2 Latch-Signals)	2
SyncManager event times (0x09F0:0x09FF)	-	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	-	c	c	c	c	c	c	c	c	c	c	c	-	-
DC receive times	x	x	x	x	c	c	c	c	c	c	c	c	c	if DC on	if DC on	if DC on	if DC on	c	c	c	c	c	c	c	c	c	if DC on	if DC on	x	
DC time loop control controllable by PDI	-	-	-	-	c	c	c	c	c	c	c	c	c	c	-	-	-	c	c	c	c	c	c	c	c	c	c	-	-	
DC sync/latch activation (0x0140[11:10])	-	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
DC time loop activation (0x0142[8])	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Propagation delay measurement with traffic (BWR/FPWR 0x900 detected at each port)	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	
LatchSignal state in latch status register (0x09AE:0x09AF)	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	
SyncSignal auto-activation (0x0981[3])	-	x	-	x	x	x	x	x	x	x	x	x	x	-	-	-	-	x	x	x	x	x	x	x	x	x	-	-	-	
SyncSignal 32 or 64 bit start time (0x0981[4])	-	x	-	x	x	x	x	x	x	x	x	x	x	-	-	-	-	x	x	x	x	x	x	x	x	x	-	-	-	

[3] SYNC/LATCH[1] available if no MII port is used.

Feature	ET1200 -0003	ET1150	ET1100 -0003	IP core V4.0.0	IP core Altera® V3.0.10	IP core Altera® V3.0.0-3.0.9	IP core Altera® V2.4.4	IP core Altera® V2.4.3	IP core Altera® V2.4.0	IP core Altera V2.3.1/ V2.3.2	IP core Altera V2.3.0	IP core Altera V2.2.1	IP core Altera V2.2.0	IP core Altera V2.0.0	IP core Altera V1.1.1	IP core Altera V1.1.0	IP core Altera V1.0.0	IP core Xilinx® V3.00k	IP core Xilinx® V3.00c-3.00j	IP core Xilinx® V2.04e	IP core Xilinx V2.04d	IP core Xilinx V2.04a	IP core Xilinx V2.03d	IP core Xilinx V2.03b/c	IP core Xilinx V2.03a	IP core Xilinx V2.02a	IP core Xilinx V2.00a	IP core Xilinx V1.01b	ESC20
SyncSignal late activation (0x0981[6:5])	-	x	-	x	x	x	x	x	x	x	x	x	x	-	-	-	-	x	x	x	x	x	x	x	x	x	-	-	-
SyncSignal debug pulse (0x0981[7])	-	x	-	x	x	x	x	x	x	x	x	x	x	-	-	-	-	x	x	x	x	x	x	x	x	x	-	-	-
SyncSignal activation state 0x0984)	-	x	-	x	x	x	x	x	x	x	x	x	x	-	-	-	-	x	x	x	x	x	x	x	x	x	-	-	-
Reset filters after writing filter depth	-	x	-	x	x	x	x	x	x	x	x	x	x	-	-	-	-	x	x	x	x	x	x	x	x	x	-	-	-
Speed counter diff direct control (0x0938:0x0939)	-	x	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
ESC specific registers (0x0E00:0x0EFF)																													
Product and vendor ID	-	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
POR values	x	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
FPGA update	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x
Process RAM and user RAM																													
Process RAM (0x1000 ff.) [Kbyte]	1	15	8	0-60	0-60	0-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	0-60	0-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	4
User RAM (0x0F80:0x0FFF)	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
User RAM ESC feature initialization	-	-	-	c	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
RAM BIST	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Additional EEPROMs	1	1	1	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	1-2	2
SII EEPROM (I²C)	x	c (EEPROM of µC used)	x	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	x	x	x	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	c (EEPROM of µC used)	x	x
FPGA configuration EEPROM	-	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
LED signals																													
RUN LED	x	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x
RUN LED override	-	x	-	c	c	c	c	c	c	c	c	-	-	-	-	-	-	c	c	c	c	c	c	c	c	-	-	-	-
Link/activity(x) LED per port	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
PERR(x) LED per port	x	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Device ERR LED	-	x	-	c	c	c	c	c	c	c	c	-	-	-	-	-	-	c	c	c	c	c	c	c	c	-	-	-	-
STATE_RUN LED	-	x	-	c	c	c	c	c	c	c	c	-	-	-	-	-	-	c	c	c	c	c	c	c	c	-	-	-	-
PDI_ERR LED per PDI	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Optional LED states																													
RUN LED: bootstrap	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
RUN LED: booting	-	x	-	c	c	c	c	c	c	c	c	-	-	-	-	-	-	c	c	c	c	c	c	c	c	-	-	-	-
RUN LED: device identification	-	x	-	c	c	c	c	c	c	c	c	-	-	-	-	-	-	c	c	c	c	c	c	c	c	-	-	-	-
RUN LED: loading SII EEPROM	-	x	-	c	c	c	c	c	c	c	c	-	-	-	-	-	-	c	c	c	c	c	c	c	c	-	-	-	-
RUN LED: POR values signaling	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Error LED: SII EEPROM loading error	-	x	-	c	c	c	c	c	c	c	c	-	-	-	-	-	-	c	c	c	c	c	c	c	c	-	-	-	-
Error LED: invalid hardware configuration	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Error LED: process data watchdog timeout	-	x	-	c	c	c	c	c	c	c	c	-	-	-	-	-	-	c	c	c	c	c	c	c	c	-	-	-	-
Error LED: PDI watchdog timeout	-	x	-	c	c	c	c	c	c	c	c	-	-	-	-	-	-	c	c	c	c	c	c	c	c	-	-	-	-
Error LED: BIST error	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Error LED: error indication 0x0130[4]	-	x	-	c	c	c	-	-	-	-	-	-	-	-	-	-	-	c	c	-	-	-	-	-	-	-	-	-	-
Link/activity: port closed	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Link/activity: local auto-negotiation error	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Link/activity: remote auto-negotiation error	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Link/activity: unknown PHY auto-negotiation error	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
LED test	-	-	-	c	c	c	-	-	-	-	-	-	-	-	-	-	-	c	c	-	-	-	-	-	-	-	-	-	-
Clock supply																													
Crystal	x	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Crystal oscillator	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
TX_CLK from PHY	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
25ppm clock source accuracy	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Internal PLL	x	x	x	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	User logic	x

Feature	ET1200 -0003	ET1150	ET1100 -0003	IP core V4.0.0	IP core Altera® V3.0.10	IP core Altera® V3.0.0-3.0.9	IP core Altera® V2.4.4	IP core Altera® V2.4.3	IP core Altera® V2.4.0	IP core Altera V2.3.1/ V2.3.2	IP core Altera V2.3.0	IP core Altera V2.2.1	IP core Altera V2.2.0	IP core Altera V2.0.0	IP core Altera V1.1.1	IP core Altera V1.1.0	IP core Altera V1.0.0	IP core Xilinx® V3.00k	IP core Xilinx® V3.00c-3.00j	IP core Xilinx® V2.04e	IP core Xilinx V2.04d	IP core Xilinx V2.04a	IP core Xilinx V2.03d	IP core Xilinx V2.03b/c	IP core Xilinx V2.03a	IP core Xilinx V2.02a	IP core Xilinx V2.00a	IP core Xilinx V1.01b	ESC20
Power supply voltages	1-3	1-3	1-2	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	2
I/O voltages				FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	
1.8 V	-	x	-	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	-
2.5 V	-	x	-	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	-
3.3 V	x	x	x	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	x
5 V	(x)	-	(x)	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	-
Separate I/O voltages	-	PDI+COM	-	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	-
Core voltage	2.5V	1.1V	2.5V	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	1.5V
Internal regulators	2x LDO	1x LDO/ DC-DC	1x LDO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Input voltage	3.3V/5V	2.5V/3.3V/ -	3.3V/5V																										
Output core Voltage	x	x	x																										
Output I/O Voltage	3.3V	-	-																										
JTAG	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Package	QFN48	BGA128	BGA128	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	BGA256
Size [mm²]	7x7	10x10	10x10	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	FPGA dep.	17x17
Original release date	11/2006	2025	3/2007	9/2025	1/2015	3/2013	1/2015	7/2013	3/2011	2/2010	12/2009	6/2009	6/2008	8/2007	1/2007	11/2006	7/2006	1/2015	5/2013	1/2015	7/2013	3/2011	6/2010	2/2010	12/2009	6/2008	8/2007	1/2007	7/2005
Configuration and pinout calculator	x	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Register configuration	fixed	fixed	fixed	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	3 sets (s/m/l)	3 sets (s/m/l)	3 sets (s/m/l)	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	individual	3 sets (s/m/l)	fixed
Evaluation version	-	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	-	x	x	x	x	x	x	x	x	-	-	-	-
Vendor ID package	-	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Internal tri-state drivers	x	x	x	-	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	c	x
IP core configuration tool	-	-	-	x ET1810: -	-	-	-	-	-	-	-	-	-	-	-	-	-	x	x	x	x	x	x	x	x	x	x	x	-
XPS IP cores	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x	x	x	x	x	x	x	x	x	x	x	-
Vivado IP cores	-	-	-	ET1815: x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Propel IP cores	-	-	-	ET1825: x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Example designs/ pre-synthesized time-limited evaluation core included in setup	-	-	-	separate/ 0	4/4	6/6	3/3	5/4	5/4	7/3	7/3	7/3	7/3	4/-	4/-	4/-	2/-	3/3	4/3	2/1	4/2	4/2	3/1	3/1	3/1	4/1	3/-	3/-	-

Table 3: ESC feature legend

Symbol	Description
x	available
-	not available
c	configurable
User logic	Functionality can be added by user logic inside the FPGA
POR	Value can be changed by power-on reset values (strapping)
PROM	Value can be changed by SII EEPROM content
OTP	Value can be changed by OTP content
red	Feature changed in this version

3 ESC registers

Table 4: ESC registers

Address	Length (byte)	Description	ET1200	ET1150	ET1100	IP core V4.0.0	IP core V3.0.0-V3.0.10, V3.00c-V3.00k	IP core V2.4.0-V2.4.4/ V2.04a-V2.04e			IP core V2.3.0-V2.3.2/ V2.03a-V2.03d			IP core V2.2.1/V2.2.0/ V2.02a			IP core V2.0.0/V2.00a			IP core V1.1.1/V1.01b			IP core V1.1.0			IP core V1.0.0			ESC20	IP core option
								Register set			Register set			Register set			Register set			Register set			Register set			Register set				
								S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L		
0x0000	1	Type	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0001	1	Revision	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0002:0x0003	2	Build	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0004	1	FMMUs supported	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0005	1	SyncManagers supported	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0006	1	RAM size	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0007	1	Port descriptor	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	
0x0008:0x0009	2	ESC features supported	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0010:0x0011	2	Configured station address	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0012:0x0013	2	Configured station alias	x	x	x	x	x	x	x	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	x	x	
0x0020	1	Write register enable	x	x	x	c	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	x	x	*Write protection*
0x0021	1	Write register protection	x	x	x	c	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	x	x	*Write protection*
0x0030	1	ESC write enable	x	x	x	c	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	x	x	*Write protection*
0x0031	1	ESC write protection	x	x	x	c	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	x	x	*Write protection*
0x0040	1	ESC reset ECAT	x	x	x	c	c	c	c	c	c	c	c	c	c	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Reset slave by ECAT/PDI*
0x0041	1	ESC reset PDI	-	x	-	c	c	c	c	c	c	c	c	c	c	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Reset slave by ECAT/PDI*
0x0100:0x0101	2	ESC DL control	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0102:0x0103	2	Extended ESC DL control	x	x	x	x	x	x	x	x	r/c	r/c	x	r/c	r/c	x	r/c	r/c	x	r	r	x	r	r	x	r	r	x	x	x	
0x0108:0x0109	2	Physical read/write offset	x	x	x	c	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	x	x	*Read/write offset*
0x0110:0x0111	2	ESC DL status	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0120	5 bits [4:0]	AL control	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0120:0x0121	2	AL control	x	x	x	x	x	x	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
0x0130	5 bits [4:0]	AL status	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0130:0x0131	2	AL status	x	x	x	x	x	x	x	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
0x0134:0x0135	2	AL status Code	x	x	x	c	c	c	x	x	c	x	x	c	x	x	c	x	x	-	x	x	-	x	x	-	-	-	x	*AL status code register*
0x0138	1	RUN LED override	-	x	-	c	c	c	c	c	c	c	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Extended RUN/ERR LED*
0x0139	1	ERR LED override	-	x	-	c	c	c	c	c	c	c	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Extended RUN/ERR LED*
0x0140	1	PDI0 control	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0141	1	ESC configuration A0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0142:0x0143	2	ESC configuration A5	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
0x0144:0x0145	2	ESC configuration A6	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
0x014E:0x014F	2	PDI0 information	-	x	-	x	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*PDI information register*
0x0150	1	PDI0 configuration	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0151	1	DC sync/latch configuration	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0152:0x0153	2	Extended PDI0 configuration	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0158:0x0159	2	PDI0 user mode from ECAT	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*PDI user mode*
0x015C:0x015D	2	PDI0 user mode from PDI	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*PDI user mode*
0x0180	1	PDI1 control	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Enable PDI1*
0x0181	1	ESC configuration B0	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Enable PDI1*
0x0182:0x0183	2	ESC configuration B5	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	

Address	Length (byte)	Description	ET1200	ET1150	ET1100	IP core V4.0.0	IP core V3.0.0-V3.0.10, V3.00c-V3.00k	IP core V2.4.0-V2.4.4/ V2.04a-V2.04e Register set			IP core V2.3.0-V2.3.2/ V2.03a-V2.03d Register set			IP core V2.2.1/V2.2.0/ V2.02a Register set			IP core V2.0.0/V2.00a Register set			IP core V1.1.1/V1.01b Register set			IP core V1.1.0 Register set			IP core V1.0.0 Register set			ESC20	IP core option
								S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L		
0x0188:0x0189	2	ESC configuration B4	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
0x018E:0x018F	2	PDI1 information	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Enable PDI1*
0x0190	1	PDI1 configuration	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Enable PDI1*
0x0191	1	Reserved	-	-	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Enable PDI1*
0x0192:0x0193	2	Extended PDI1 configuration	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Enable PDI1*
0x0198:0x0199	2	PDI1 user mode from ECAT	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*PDI user mode*
0x019C:0x019D	2	PDI1 user mode from PDI	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*PDI user mode*
0x0200:0x0201	2	ECAT event mask	x	x	x	x	x	x	x	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	x	
0x0204:0x0207	4	PDI0 AL event mask	x	x	x	r/c	r/c	r/c	x	x	r/c	x	x	r/c	x	x	r/c	x	x	r	x	x	r	x	x	r	x	x	x	*AL event mask register*
0x020A:0x020D	4	PDI1 AL event mask	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*AL event mask register* and *Enable PDI1*
0x0210:0x0211	2	ECAT event request	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0220:0x0223	4	AL event request	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0300:0x0307	4x2	RX error counter[3:0]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0308:0x030B	4x1	Forwarded RX error counter[3:0]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	
0x030C	1	ECAT processing unit error counter	-	x	x	x	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	-	*EPU and PDI error counter*
0x030D	1	PDI0 error counter	-	x	x	x	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	-	*EPU and PDI error counter*
0x030E:0x030F	2	PDI0 error code	-	x	-	x	c	c	c	x	c	c	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*EPU and PDI error counter*
0x0310:0x0313	4x1	Lost link counter[3:0]	x	x	x	x	c	c	x	x	c	x	x	c	x	x	c	x	x	-	x	x	-	x	x	-	x	x	x	*Lost link counter*
0x0314:0x0317	4x1	Extended RX error counter[3:0]	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Extended RX error counter & code*
0x0320:0x0327	4x2	RX error code[3:0]	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Extended RX error counter & code*
0x0340	1	PDI1 error counter	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Enable PDI1*
0x0341	1	PDI1 error code	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Enable PDI1*
0x0400:0x0401	2	Watchdog divider	x	x	x	r/c	r/c	r/c	x	x	r/c	x	x	r/c	x	x	r/c	x	x	r	x	x	r	x	x	r	x	x	x	*Extended watchdog*
0x0410:0x0411	2	Watchdog time PDI0	x	x	x	c	c	c	x	x	c	x	x	c	x	x	c	x	x	-	x	x	-	x	x	-	x	x	x	*Extended watchdog*
0x0412:0x0413	2	Watchdog time PDI1	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Enable PDI1*
0x0420:0x0421	2	Watchdog time process data	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0440:0x0441	2	Watchdog status process data	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0442	1	Watchdog counter process data	x	x	x	c	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	-	*Watchdog counter*
0x0443	1	Watchdog counter PDI0	x	x	x	c	c	c	c	x	c	c	x	c	c	x	c	c	x	-	-	x	-	-	x	-	-	x	-	*Watchdog counter*
0x0444	1	Watchdog counter PDI1	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Watchdog counter* and *Enable PDI1*
0x0448	1	Watchdog status PDI	-	x	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
0x0500:0x050F	16	SII EEPROM interface	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x0510:0x0515	6	PHY management interface	x	x	x	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-	x	x	-	x	x	-	x	x	x	*PHY management interface*
0x0516:0x0517	2	PHY management access state	-	x	-	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-	-	-	-	-	-	-	-	-	-	*PHY management interface*
0x0518:0x051B	4	PHY port status[3:0]	-	x	-	c	c	c	c	c	c	c	c	c	c	c	c	c	c	-	-	-	-	-	-	-	-	-	-	*Link state and PHY configuration through MI*
0x0600:0x06FC	16x13	FMMU[15:0]	3	16	8	0-16	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	4	*Number of FMMU*
0x0800:0x087F	16x8	SyncManager[15:0]	4	16	8	0-16	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	4	*Number of SyncManagers*

Address	Length (byte)	Description	ET1200	ET1150	ET1100	IP core V4.0.0	IP core V3.0.0-V3.0.10, V3.00c-V3.00k	IP core V2.4.0-V2.4.4/ V2.04a-V2.04e Register set			IP core V2.3.0-V2.3.2/ V2.03a-V2.03d Register set			IP core V2.2.1/V2.2.0/ V2.02a Register set			IP core V2.0.0/V2.00a Register set			IP core V1.1.1/V1.01b Register set			IP core V1.1.0 Register set			IP core V1.0.0 Register set			ESC20	IP core option
								S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L		
0x0900:0x090F	4x4	DC – receive times	x	x	x	x	RT	RT	RT	RT	RT	RT	RT	RT	RT	RT	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x0910:0x0917	8	DC – system time	x	DC	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x0918:0x091F	8	DC – receive time EPU	x	DC	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x0920:0x0927	8	DC – system time offset	x	DC	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x0928:0x092B	4	DC – system time delay	x	DC	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x092C:0x092F	4	DC – system time difference	x	DC	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x0930:0x0931	2	DC – speed counter start	x	DC	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x0932:0x0933	2	DC – speed counter diff	x	DC	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x0934	1	DC – system time difference filter depth	x	DC	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x0935	1	DC – speed counter filter depth	x	DC	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x0936	1	DC – receive time latch mode	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	x	
0x0938:0x0939	2	DC – speed counter diff direct control	-	DC	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*DC speed counter direct control*
0x0940:0x0943	4	DC – SYNC2 cycle time	-	S0	-	S2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x0944:0x0947	4	DC – SYNC3 cycle time	-	S0	-	S3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x0950:0x0957	8	DC – next SYNC2 pulse	-	S0	-	S2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x0958:0x095F	8	DC – next SYNC3 pulse	-	S0	-	S3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x0980	1	DC – cyclic unit control	x	SL	S0	SL	SL	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x0981	1	DC – activation	x	S0	S0	S0	S0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x0982:0x0983	2	DC – pulse length of SyncSignals	x	S0	S0	S0	S0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x0984	1	DC – activation status	-	S0	-	S0	S0	DC	DC	DC	DC	DC	DC	DC	DC	DC	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x0986	1	DC – activation SYNC2/3	-	S0	-	S2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x098C	1	DC – SYNC2 status	-	S0	-	S2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x098D	1	DC – SYNC3 status	-	S0	-	S3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x098E	1	DC – SYNC0 status	x	S0	S0	S0	S0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x098F	1	DC – SYNC1 status	x	S0	S0	S1	S1	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x0990:0x0997	8	DC – start time cyclic operation/next SYNC0 pulse	x	S0	S0	S0	S0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x0998:0x099F	8	DC – next SYNC1 pulse	x	S0	S0	S1	S1	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x09A0:0x09A3	4	DC – SYNC0 cycle time	x	S0	S0	S0	S0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x09A4:0x09A7	4	DC – SYNC1 cycle time	x	S0	S0	S1	S1	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x09A8	1	DC – latch0 control	x	L0	L0	L0	L0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x09A9	1	DC – latch1 control	x	L0	L0	L1	L1	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x09AA	1	DC – latch2 control	-	L0	-	L2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x09AB	1	DC – latch3 control	-	L0	-	L3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x09AC	1	DC – latch2 status	-	L0	-	L2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x09AD	1	DC – latch3 status	-	L0	-	L3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x09AE	1	DC – latch0 status	x	L0	L0	L0	L0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x09AF	1	DC – latch1 status	x	L0	L0	L1	L1	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x09B0:0x09B7	8	DC – latch0 positive edge	x	L0	L0	L0	L0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x09B8:0x09BF	8	DC – latch0 negative edge	x	L0	L0	L0	L0	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x09C0:0x09C7	8	DC – latch1 positive edge	x	L0	L0	L1	L1	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x09C8:0x09CF	8	DC – latch1 negative edge	x	L0	L0	L1	L1	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	DC	x	*Refer to legend*
0x09D0:0x09D7	8	DC – latch2 positive edge	-	L0	-	L2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x09D8:0x09DF	8	DC – latch2 negative edge	-	L0	-	L2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*

Address	Length (byte)	Description	ET1200	ET1150	ET1100	IP core V4.0.0	IP core V3.0.0-V3.0.10, V3.00c-V3.00k	IP core V2.4.0-V2.4.4/ V2.04a-V2.04e Register set			IP core V2.3.0-V2.3.2/ V2.03a-V2.03d Register set			IP core V2.2.1/V2.2.0/ V2.02a Register set			IP core V2.0.0/V2.00a Register set			IP core V1.1.1/V1.01b Register set			IP core V1.1.0 Register set			IP core V1.0.0 Register set			ESC20	IP core option
								S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L	S	M	L		
0x09E0:0x09E7	8	DC – latch3 positive edge	-	L0	-	L3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x09E8:0x09EF	8	DC – latch3 negative edge	-	L0	-	L3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Refer to legend*
0x09F0:0x09F3	4	DC – EtherCAT buffer change event time	-	DC	SL	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	-	-	DC	-	-	DC	-	-	DC	-	*Refer to legend*
0x09F8:0x09FB	4	DC – PDI buffer start event time	-	DC	SL	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	-	-	DC	-	-	DC	-	-	DC	-	*Refer to legend*
0x09FC:0x09FF	4	DC – PDI buffer change event time	-	DC	SL	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	ET	-	-	DC	-	-	DC	-	-	DC	-	*Refer to legend*
0x0E00:0x0E07	8	Power-on values [bits]	8	40	16	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
0x0E00:0x0E07	8	Product ID	-	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	
0x0E08:0x0E0F	8	Vendor ID	-	-	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-	
0x0E10:0x0E17	8	ESC health status	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Evaluation version, except ET1810*
0x0F00:0x0F03	4	Digital I/O output data	x	x	x	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	x	*Selected PDI (PDI0/PDI1)=Digital IO*
0x0F08:0x0F0B	4	Digital I/O input data	-	x	-	c	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	*Enable PDI1* and *Selected PDI (PDI1)=Digital IO*
0x0F10:0x0F17	8	General purpose outputs [byte]	2	8	2	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	*Number of GPIOs*
0x0F18:0x0F1F	8	General purpose inputs [byte]	-	8	2	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	0-8	-	*Number of GPIOs*
0x0F80:0x0FFF	128	User RAM	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
0x1000:0x1003	4	Digital I/O input data	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	io	*Selected PDI (PDI0)=Digital IO* and *Process data RAM>0*
0x1000 ff.		Process data RAM [Kbyte]	1	15	8	0-60	0-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	1-60	4	*Process data RAM*

Table 5: ESC register legend

Symbol	Description	ET1200 EEPROM setting	ET1150 EEPROM setting	ET1100 EEPROM setting	Option IP core V4.0.0	Option IP core V3.0.0/V3.00c-V3.0.10/V3.00k	Option IP core V2.2.0/V2.02a-V2.4.4/V2.04e	Option IP core V2.0.0/V2.00a	Option IP core V1.0.0-V1.1.1/V1.01b	ESC20
x	Available									
-	Not available									
r	Read only									
c	Configurable									
RT	DC receive times enabled	x	x	x	x	*Receive times*	*Receive times*	*Distributed clocks*	*Distributed clocks*	x
DC	DC time loop control enabled	x	0x0140[10]=1 or 0x0140[11]=1 or 0x0142[8]=1	0x0140[10]=1 or 0x0140[11]=1	*Distributed clocks*	*Distributed clocks*	*Distributed clocks*	*Distributed clocks*	*Distributed clocks*	x
SL	DC sync unit and/or latch unit enabled	x	0x0140[10]=1 or 0x0140[11]=1	0x0140[10]=1 or 0x0140[11]=1	*DC SyncSignals>0, or DC LatchSignals>0*	*DC SyncSignals>0, or DC LatchSignals>0*	*Distributed clocks*	*Distributed clocks*	*Distributed clocks*	x
S0	DC SyncSignal 0 enabled	x	0x0140[10]=1	0x0140[10]=1	*DC SyncSignals>0*	*DC SyncSignals>0*	*Distributed clocks*	*Distributed clocks*	*Distributed clocks*	x
S1	DC SyncSignal 1 enabled	x	0x0140[10]=1	0x0140[10]=1	*DC SyncSignals>1*	*DC SyncSignals>1*	*Distributed clocks*	*Distributed clocks*	*Distributed clocks*	x
S2	DC SyncSignal 2 enabled		0x0140[10]=1	0x0140[10]=1	*DC SyncSignals>2*					
S3	DC SyncSignal 3 enabled		0x0140[10]=1	0x0140[10]=1	*DC SyncSignals>3*					
L0	DC LatchSignal 0 enabled	x	0x0140[11]=1	0x0140[11]=1	*DC LatchSignals>0*	*DC LatchSignals>0*	*Distributed clocks*	*Distributed clocks*	*Distributed clocks*	x
L1	DC LatchSignal 1 enabled	x	0x0140[11]=1	0x0140[11]=1	*DC LatchSignals>1*	*DC LatchSignals>1*	*Distributed clocks*	*Distributed clocks*	*Distributed clocks*	x
L2	DC LatchSignal 2 enabled		0x0140[11]=1	0x0140[11]=1	*DC LatchSignals>2*					
L3	DC LatchSignal 3 enabled		0x0140[11]=1	0x0140[11]=1	*DC LatchSignals>3*					
ET	DC SyncManager event times are enabled	-	0x0140[10]=1 or 0x0140[11]=1	0x0140[10]=1 or 0x0140[11]=1	*SyncManager event times*	*SyncManager event times*	*SyncManager event times*	*SyncManager event times*	*Distributed clocks*	-
io	Available if digital I/O PDI is selected									
red	Register changed in this version									

4 Appendix

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