

Documentation | EN

ED5112

EtherCAT Terminal, 2-channel encoder interface, incremental, 5 V DC (DIFF RS422, TTL, open collector), 5 MHz, Push-in, 2 x AB/1 x ABC

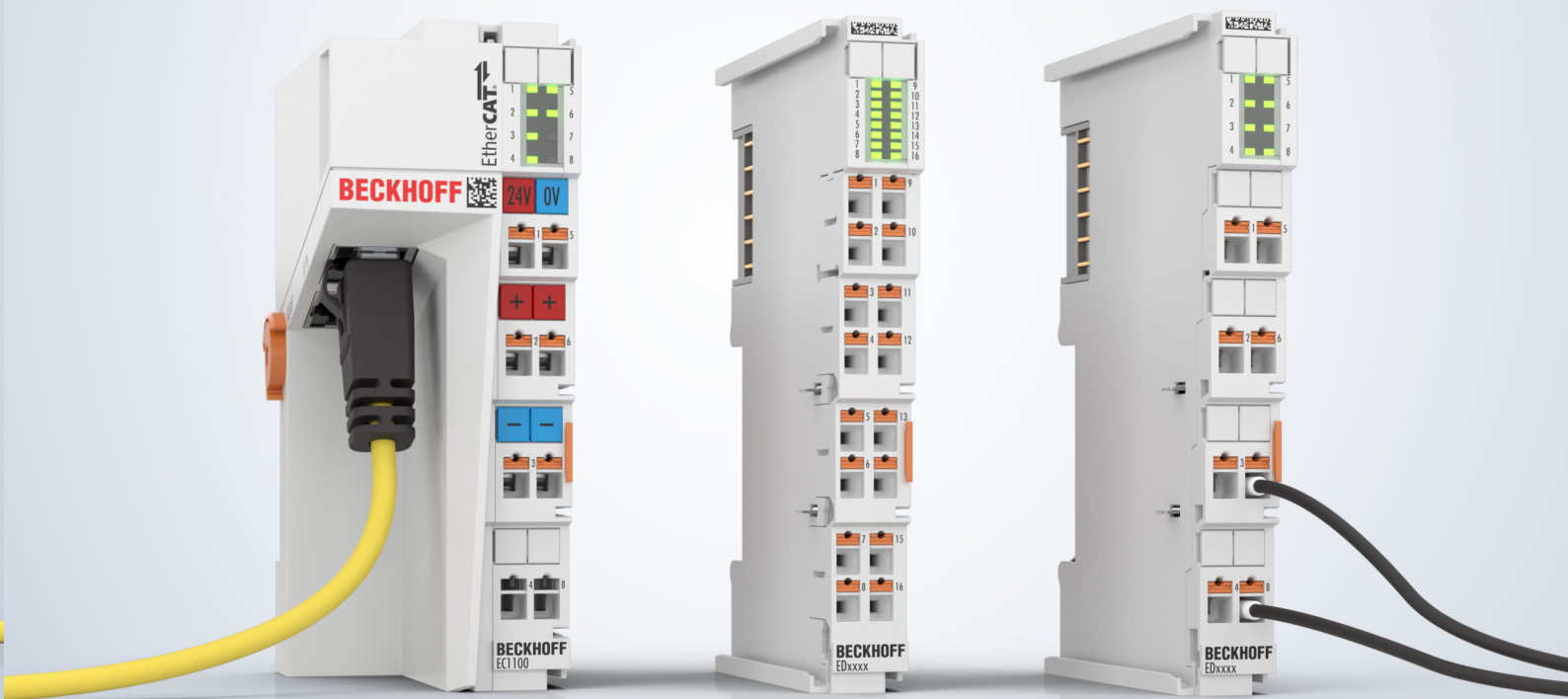


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1 Foreword

1.1 Product overview

This documentation covers the following products:

ED5112 [▶ 9] EtherCAT Terminal, 2-channel encoder interface, incremental, 5 V DC (DIFF RS422, TTL, open collector), 5 MHz, push-in, 2 x AB/1 x ABC

Use the tabular product overview or the product finder to find the right product for your application (<https://www.beckhoff.com/IO>).

1.2 Notes on the documentation

Intended audience

This description is only intended for the use of trained specialists in control and automation engineering who are familiar with the applicable national standards.

It is essential that the documentation and the following notes and explanations are followed when installing and commissioning these components.

The qualified personnel is obliged to always use the currently valid documentation.

The responsible staff must ensure that the application or use of the products described satisfy all the requirements for safety, including all the relevant laws, regulations, guidelines and standards.

Disclaimer

The documentation has been prepared with care. The products described are, however, constantly under development.

We reserve the right to revise and change the documentation at any time and without prior announcement.

No claims for the modification of products that have already been supplied may be made on the basis of the data, diagrams and descriptions in this documentation.

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1.3 Guide through documentation

NOTICE



Further components of documentation

This documentation describes device-specific content. It is part of the modular documentation concept for Beckhoff I/O components. For the use and safe operation of the devices described in this documentation, additional cross-product descriptions are required, which can be found in the following table.

Title	Description
EtherCAT System Documentation (PDF)	• System overview • EtherCAT basics • Cable redundancy • Hot Connect • EtherCAT devices configuration
Infrastructure for EtherCAT/Ethernet (PDF)	Technical recommendations and notes for design, implementation and testing
Software Declarations I/O (PDF)	Open source software declarations for Beckhoff I/O components

The documentations can be viewed at and downloaded from the Beckhoff website (www.beckhoff.com) via:

- the “Documentation and Download” area of the respective product page,
- the [Download finder](#),
- the [Beckhoff Information System](#).

If you have any suggestions or proposals for our documentation, please send us an e-mail stating the documentation title and version number to: documentation@beckhoff.com

1.4 Safety instructions

Safety regulations

Please note the following safety instructions and explanations!

Product-specific safety instructions can be found on following pages or in the areas mounting, wiring, commissioning etc.

Exclusion of liability

All the components are supplied in particular hardware and software configurations appropriate for the application. Modifications to hardware or software configurations other than those described in the documentation are not permitted, and nullify the liability of Beckhoff Automation GmbH & Co. KG.

Personnel qualification

This description is only intended for trained specialists in control, automation and drive engineering who are familiar with the applicable national standards.

Signal words

The signal words used in the documentation are classified below. In order to prevent injury and damage to persons and property, read and follow the safety and warning notices.

Personal injury warnings

DANGER

Hazard with high risk of death or serious injury.

WARNING

Hazard with medium risk of death or serious injury.

CAUTION

There is a low-risk hazard that could result in medium or minor injury.

Warning of damage to property or environment

NOTICE

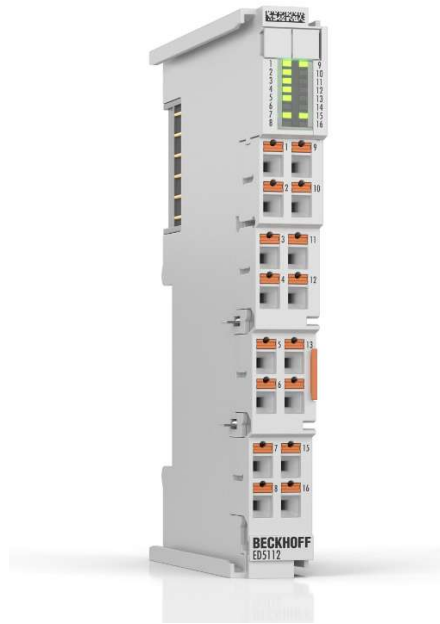
The environment, equipment, or data may be damaged.

Information on handling the product



This information includes, for example:
recommendations for action, assistance or further information on the product.

2 Product description



EtherCAT Terminal, 2-channel encoder interface, incremental, 5 V DC (DIFF RS422, TTL, open collector), 5 MHz, push-in, 2 x AB/1 x ABC

The ED5112 EtherCAT Terminal is an interface for the direct connection of two incremental encoders with A and B tracks or one encoder with A, B, and C tracks. Encoders with differential signals (RS422) or single-ended signals (TTL and open collector) can be connected, and input frequencies up to 5 MHz can be evaluated.

In 2-channel mode, one 24 V DC digital input is available per channel for saving, locking, or setting the counter value.

Both inputs can be used in 1-channel mode. Furthermore, the counter value can also be set directly to a specified value via the process data, or the counter can be locked. The encoders can be supplied with 5 V, 12 V, or 24 V DC directly via the connection points of the terminal.

Special features:

- can be used as a 1 × ABC or 2 × AB incremental encoder interface
- save, lock, set counters
- integrated frequency and period measurement
- can optionally be used as a 5 V up/down counter
- Microincrements
- synchronous reading of the position value via distributed clocks
- timestamp on the last registered incremental edge and the latch value via the 24 V digital inputs

The ED5112 enables the measurement of period, frequency, or speed with a resolution of 10 ns. In 1-channel mode, a duty cycle measurement of the input signal is also implemented.

Due to the optional interpolating microincrements functionality, the ED5112 delivers particularly precise position values even with dynamic axes. It supports the synchronous reading of the encoder value together with other input data in the EtherCAT system via high precision EtherCAT Distributed Clocks (DC). In addition, timestamps are available for the last registered incremental edge, the edge at the latch input, and the zero pulse track C. The use of encoder profiles enables simple and fast linking of the process data into motion control applications.

The ED-series EtherCAT Terminals have push-in connection technology which makes wiring easy and tool-free.

2.1 Technical data

General	ED5112	
	1-channel mode	2-channel mode
Number of channels Total	1	2
Internal communication protocol	EtherCAT	
Minimum cycle time	71.4 µs	125 µs

Position interface	ED5112	
	1-channel mode	2-channel mode
Number of channels	1	2
Function	incremental encoder interface with gate/latch input	
Sensor type	incremental position detection	
Signal range	RS422, TTL, open collector, counter, pulse generator	
Resolution Process data (counter)	32 bit (adjustable)	
Microincrements	yes	no
Resolution Microincrements	8 bit	–
Sensor supply Output voltage	5 V DC, 12 V DC, 24 V DC (adjustable)	
Sensor supply Output current	max. 0.3 A	
Quadrature decoder	yes	
RS422		
Encoder connection	differential inputs: A, $\overline{A}$, B, $\overline{B}$, C, $\overline{C}$	differential inputs: A, $\overline{A}$, B, $\overline{B}$
Input frequency	20 million increments/s with 4-fold evaluation, corresponds to 5 MHz	
Wire break detection	yes	
TTL		
Encoder connection	single-ended connection: A, B, C	single-ended connection: A, B
Input frequency	4 million increments/s with 4-fold evaluation, corresponds to 1 MHz	
Wire break detection	no	
Open collector		
Encoder connection	single-ended connection: A, B, C	single-ended connection: A, B
Input frequency	400 kilo increments/s with 4-fold evaluation, corresponds to 100 kHz	
Wire break detection	no	

Digital input	ED5112	
	1-channel mode	2-channel mode
Standard digital Positive switching		
Number of channels	max. 2	
Function	latch, gate	
Connection technology	1-wire	
Signal range Nominal	24 V DC	
Signal voltage "0"	-3...+5 V DC	
Signal voltage "1"	11...30 V DC	
Input filter	typ. > 1 µs	
Input current	typ. 2.5 mA	

Digital input	ED5112	
	1-channel mode	2-channel mode
Standard digital Ground switching		
Number of channels	1	—
Function	alarm input, status input	—
Connection technology	1-wire	—
Signal range Nominal	5 V DC	—
Signal voltage "0"	2...6 V DC	—
Signal voltage "1"	-6...+0.8 V DC	—
Input current	typ. 5 mA	—
Cable length Sensor cable	max. 30 m	—

XFC	ED5112	
	1-channel mode	2-channel mode
Distributed clocks	yes	
Distributed clocks Accuracy	< 1 µs	
Distributed clocks Scope	64 bit	
Timestamp	yes	
Timestamp Accuracy	typ. < 10 µs	
Timestamp Resolution	1 ns	
Oversampling	no	

Supply and electrical isolation	ED5112	
	1-channel mode	2-channel mode
Electronics Supply voltage	via E-bus, via power contacts	
E-bus Current consumption	typ. 100 mA	
Power contacts Input voltage	24 V DC (-15%/+20%)	
Power contacts Current carrying capacity	max. 10 A	
Power contacts Current consumption	typ. 10 mA + load	
Power contacts Output voltage	corresponds to Power contacts Input voltage	
Electrical isolation Channel/channel	no	
Electrical isolation Channel/bus	functional, 707 V DC (type test)	

Environmental conditions	ED5112	
	1-channel mode	2-channel mode
Operating temperature	0...+55°C	
Storage temperature	-25...+85°C	
Relative humidity	95%, no condensation	
Installation position	variable	

Standards and approvals	ED5112	
	1-channel mode	2-channel mode
Vibration resistance	conforms to EN 60068-2-6	
Shock resistance	conforms to EN 60068-2-27	
EMC immunity	conforms to EN 61000-6-2	
EMC emission	conforms to EN 61000-6-4	
Markings*)	CE	
Approvals*)	—	
*) Real applicable approvals/markings, see name plate on the side (product labeling)		

Housing data	ED-12-16pin
Weight	approx. 60 g
Protection rating	IP20
Material	polycarbonate
Dimensions Width (single)	15 mm
Dimensions Width (stacked)	12 mm
Dimensions Height	100 mm
Dimensions Depth	65 mm
Installation Terminal/back wall	DIN rail, 35 mm (EN 60715)
Installation Terminal/terminal	double slot and key connection
Pluggable wiring level	no
Connection mechanism	push-in
Connection cross-section Solid wire	0.08...1.5 mm ²
Connection cross-section Stranded wire	0.25...1.5 mm ²
Connection cross-section With ferrule	0.14...0.75 mm ²
Connection cross-section AWG Solid wire	AWG28...16
Connection cross-section AWG Stranded wire	AWG22...16
Connection cross-section AWG With ferrule	AWG26...19
Stripping length	8...9 mm
Power contact "+" (left)	yes
Power contact "+" (right)	yes
Power contact "-" (left)	yes
Power contact "-" (right)	yes
Power contact "≡" (left)	no
Power contact "≡" (right)	no
Insertion lock for power contact "≡"	yes

2.2 Overview of functions in single- and two-channel mode

Function		Single-channel mode [► 48] 1 x ABC	Two-channel mode [► 97] 2 x AB
Set counter value via	PLC variable	Yes	Yes
	zero pulse C	Yes	No
	Latch input	Yes	No
	Gate/Latch combination input	No	Yes
Reset counter value via	zero pulse C	Yes	No
	Latch input	Yes	No
	Gate/Latch combination input	No	Yes
Save counter value via	zero pulse C	Yes	No
	Latch input	Yes	No
	Gate/Latch input	Yes	No
	Gate/Latch combination input	No	Yes
Lock counter value via	PLC variable	Yes	Yes
	Gate/Latch input	Yes	No
	Gate/Latch combination input	No	Yes
Detect counting direction		Yes	No
Detect reversion of rotation		Yes	No
Frequency calculation		Yes	Yes
Period duration calculation		Yes	Yes
Duty cycle evaluation		Yes	No
Micro-increments		Yes	No
Timestamp function		Yes	No
Filter function		Yes	Yes
Plausibility check		Yes	Yes

2.3 Technical properties

The ED5112 incremental encoder interface terminal enables connection of incremental encoders to the Bus Coupler or the PLC. In addition to the encoder inputs A, B, and the optional zero pulse C, up to two additional 24 V DC inputs are available ("latch" and "Gate"), which can be used for resetting, setting, locking and storing the counter value. If the incremental encoder has an alarm output, this can be connected to the "Digital input" Input (5 V DC).

- The following inputs are available with the respective technical characteristics:
 - Encoder connection:
Differential signals according to RS422 and single-ended signals from TTL encoders and open collector encoders are supported.
 - "Latch" and "Gate" inputs
 - Input "Digital input"
- The terminal provides a parameterizable encoder supply.
 - Encoder operating voltage

NOTICE

Fast digital inputs – interference from interfering devices

Please note that the input wiring has very little filtering. It has been optimized for fast signal transmission from the input to the evaluation unit. In other words, rapid level changes/pulses in the μ s range and/or high-frequency interference signals from devices (e.g. proportional valves, stepper motor or DC motor output stages) arrive at the evaluation unit almost unfiltered/unattenuated. These interferences can be incorrectly detected as a signal.

- To suppress interference, an additional input filter can be parameterized.
- Furthermore, EMC-compliant cabling and the use of separate power supply units for the terminal and the devices causing interference are recommended.

2.3.1 Supported encoders/signal types

Differential signals according to RS422 are intended as encoder connection. Single-ended signals from TTL encoders and also signals from Open Collector encoders are also options, through internal pull-up resistances.

The following signal types are supported:

Encoder	Signal type	Setting in Index 0x80n1:1D * "Counter mode"	Cut-off frequency	Comments
Encoder with or without zero pulse track C	"RS422 (diff. input)"	0	20 million increments/s with 4-fold evaluation, corresponds to 5 MHz per track	Signal levels according to RS422 are expected
Counter/pulse generator with or without zero pulse track C		1		Detection of wire break and short circuit [► 15]
Encoder with or without zero pulse track C	"TTL (single ended)"	2	4 million increments/s with 4-fold evaluation, corresponds to 1 MHz per track	A voltage level of nominally 2.0 V to 6.0 V with a current of 2.1 mA or higher is expected.
Counter/pulse generator with or without zero pulse track C		3		No wire break detection
Encoder with or without zero pulse track C	"open collector"	4	400,000 increments/s with 4-fold evaluation, corresponds to 100 kHz per track	No wire break detection
Counter/pulse generator with or without zero pulse track C		5		

*) depending on the number of channels (n = 0 for channel 1 and n = 1 for channel 2)

The correct wiring for the respective encoder can be found in chapter "Connection [► 20]".

2.3.1.1 Signal type "RS422 (diff. input)"

Differential signal levels according to RS422 are expected with the following settings in "Counter mode" (0x80n1:1D):

- 0: "Encoder RS422 (diff. input)"
- 1: "Counter RS422 (diff. input)"

A cut-off frequency of up to 20 million increments per second is permissible with 4-fold evaluation (corresponds to 5 MHz).

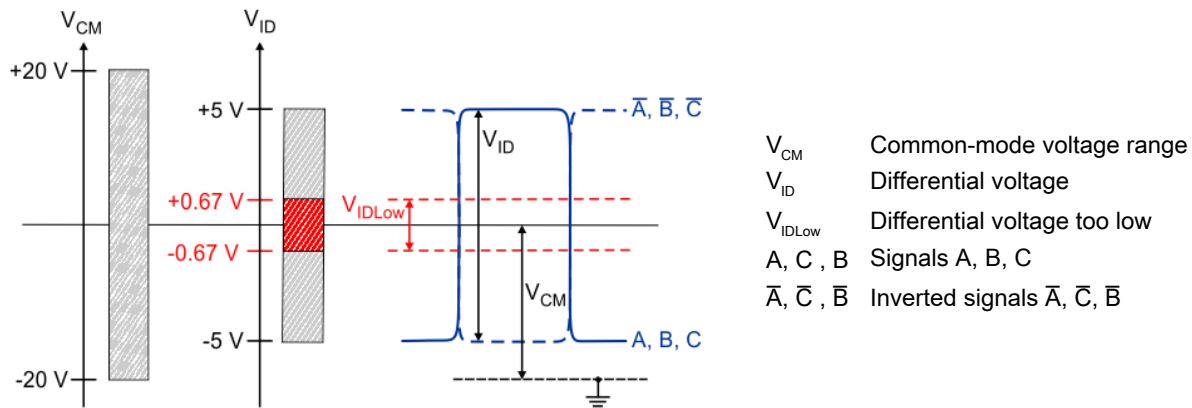


Fig. 1: RS422 signal level

NOTICE

Exceeding of Common-mode range

Exceeding the Common-mode voltage range can lead to destruction of the device.

RS422 - wire break and short circuit detection (open circuit)

In the "RS422 (diff. input)" modes it is possible to detect a wire break or short circuit at the individual encoder inputs.

- In case of wire break, e.g. between input A and input $\bar{A}$,
 - the differential voltage V_{ID} is almost 0 V,
 - which leads to an error with low differential voltage.
- In case of a short circuit, e.g. between input A and input $\bar{A}$, the error behavior is similar to a wire break and also leads to error detection.

Activation and diagnosis of a wire break or short circuit can be found in the chapter "[RS422 - Wire break and short circuit detection \(Open circuit\)](#)". [► 143]



Error bits not permanently set in case of wire break at an encoder input

If a wire break is only present at one encoder input (e.g. only track A), it may happen in individual cases that the differential voltage (V_{ID}) is above the limit range (V_{IDLow}) due to the applied common mode voltage (V_{CM}).

This means that the error is not clearly identified.

The corresponding error bits ("Open circuit" and "Error A") are not permanently present!

NOTICE

Differential and single-ended connection

The RS422 signal transmits a differential voltage, which makes the signal less sensitive to interference compared to a single-ended signal.

- If the encoder signal is to be transmitted over longer distances or at higher frequencies, an encoder with RS422 signals is recommended.
- Shielded and twisted pair cables should be used.

2.3.1.2 Signal type TTL (single-ended) and Open Collector

With the following settings in "Counter mode" (0x80n1:1D), a voltage level of nominally 2.0 V to 6.0 V with a current of 2.1 mA or higher is expected:

- 2: "Encoder TTL (single ended)"
- 3: "Counter TTL (single ended)"
- 4: "Encoder open collector"
- 5: "Counter open collector"

For TTL encoders a cut-off frequency of up to 4 million increments per second is permissible with 4-fold evaluation. This corresponds to 1 MHz.

For open collector encoders, a cut-off frequency of up to 400,000 increments per second is permissible with 4-fold evaluation. This corresponds to 100 kHz.

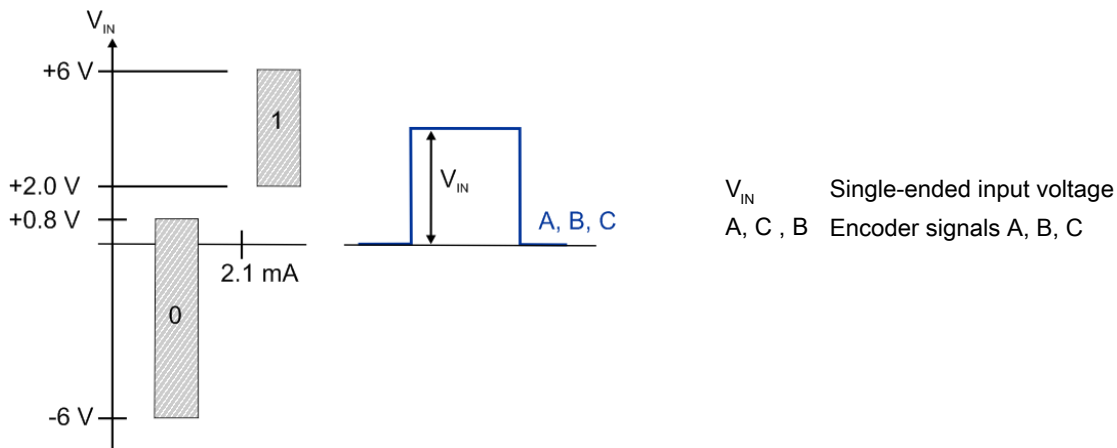


Fig. 2: TTL, open collector signal level (single-ended signal)

NOTICE

Wire break detection (open circuit)

Wire break detection (open circuit) inherently does not work with single-ended cables: TTL and open collector encoders, as well as counters and pulse generators.

NOTICE

Open Collector wiring

When selecting an Open Collector encoder under "Counter mode" (0x80n1:1D), the inputs A, B, C are connected to 5 V via pull-up resistors (1 k Ω).

2.3.2 Latch and gate inputs

The terminal provides two digital 24 V DC inputs. The function of these inputs is described in the respective chapter.

- Latch input [► 93] ("Latch extern")
- Gate input [► 94] ("Latch extern 2")

Both inputs are type 3 inputs according to EN 61131-2, with a minimum pulse duration of $t_{ON} > 1 \mu s$.

Digital input type 3, according to EN 61131-2	Voltage [V]	Input current [mA]
Signal voltage "0 - LOW"	-3 V...+5 V typ.	0 mA...2.6 mA typ.
Signal voltage "1 - HIGH"	11 V...30 V typ.	2.5 mA typ.

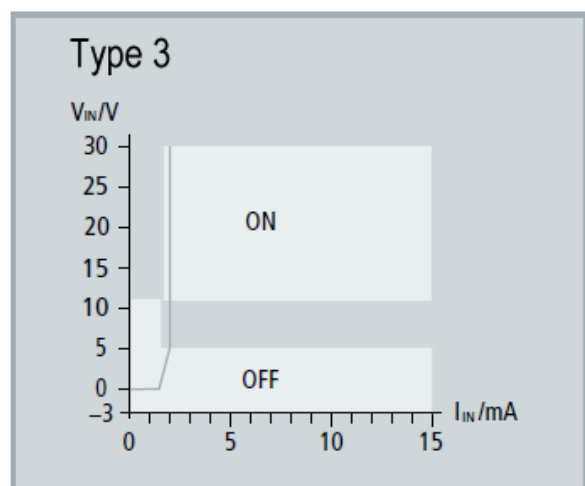


Fig. 3: Characteristic curve input 24 V DC type 3

NOTICE

Be aware of bouncing when using electromechanical switches and push buttons

When using electromechanical switches and push buttons, repeated closing and opening of the switch or push button can occur when the switch or push button is actuated, which is referred to as bouncing.

- If the function 0x80n0:22 "Enable continuous latch extern" or 0x80n0:23 "Enable continuous latch extern 2" is active, the stored value will be overwritten several times due to bouncing. This returns not the first value, but the last value stored in the input process data "Latch value" (index 0x60n0:12) or "Latch value 2" (0x60n0:22).
- If the function is deactivated, only the first opening or closing of the switch or push button is detected and saved as a value in the corresponding parameter. No other actions are taken into account.

2.3.3 Input “Digital input”

The terminal provides the input “Digital input”. The function is described in chapter [Input “Digital input”](#) [► 96].

The input is 5 V compatible.

Input “Digital input”, 5 V-TTL input characteristics	Voltage [V]	Input current [mA]
Signal voltage “0 - LOW”	-6 V...+0.8 V	5 mA typ.
Signal voltage “1 - HIGH”	+2 V...+6 V	0 mA typ.

NOTICE

Wiring of the input “Digital input”

In the terminal the input “Digital input” is internally connected to 5 V via a pull-up resistor (1 k Ω). The encoder output must actively pull the signal against GND. The resistance must be dimensioned so that it is less than 120 Ω .

External power supply is not recommended. If an external supply is used, the maximum permitted voltage is 5 V against GND.

2.3.4 Encoder operating voltage (supply voltage)

The encoder supply is generated internally from the 24 V of the power contacts. The encoder supply can be set in index [0x8001:17 \[► 151\]](#) "Supply voltage". An operating voltage of 5 V DC is preset. Voltage values of 5 V DC, 12 V DC, and 24 V DC can be selected. The setting applies to both channels. Before switching to higher voltages, ensure that both encoders support the voltage range.

The following tolerances apply:

Voltage range	Tolerance
5 V DC	+/-5% (4.75 V...5.25 V)
12 V DC	+/-10% (10.8 V...13.2 V)
24 V DC	-15% to +20% (20.4 V...28.8 V)



Setting the encoder supply via index [0x8001:17 \[► 151\]](#)

The encoder supply is set centrally for both channels via the index [0x8001:17 \[► 151\]](#) (channel 1). The corresponding index [0x8011:17](#) of the second channel has no parameterization function.

NOTICE

Setting the encoder supply voltage

- Before switching to a higher voltage, make sure that the connected encoders support the selected voltage range!
- To write to [0x80n1:17](#) "Supply voltage" you have to set the value [0x72657375](#) (ASCII: "user") in index [0xF008 \[► 182\]](#) "Code word".

2.4 Connection

⚠ WARNING

Risk of injury through electric shock and damage to the device!

Bring the bus terminal system into a safe, de-energized state before beginning to mount, disassemble, or wire the bus terminals!

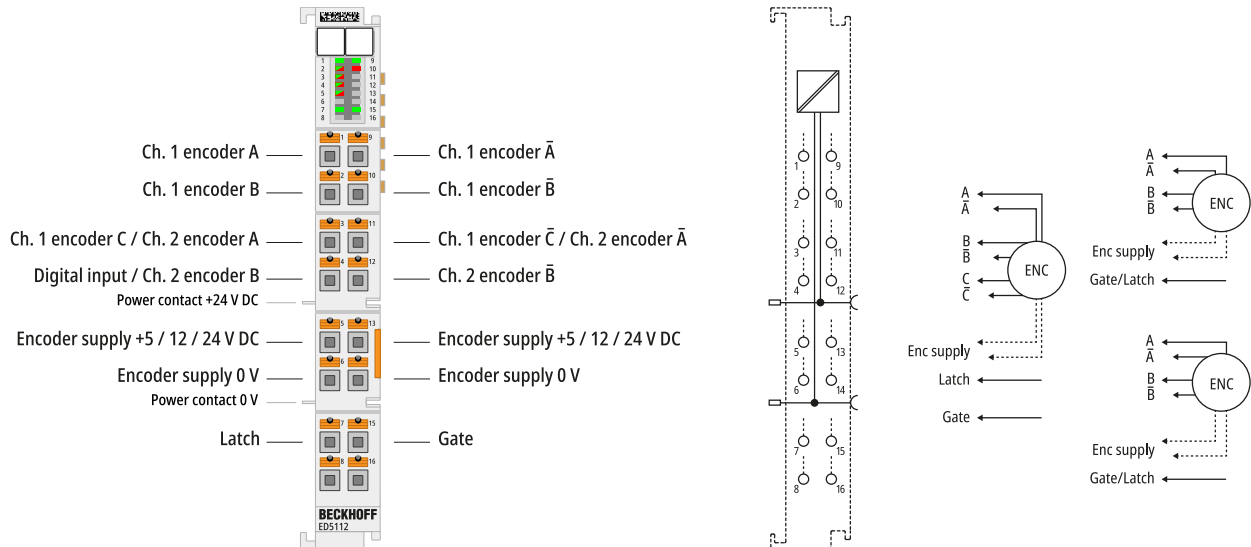


Fig. 4: ED5112

Terminal point		Description	
Abbreviation	No.	1-channel mode 1xABC	2-channel mode 2xAB
Ch1 A	1	Channel 1, encoder input A	Channel 1, encoder input A
Ch1 B	2	Channel 1, encoder input B	Channel 1, encoder input B
Ch1 C/Ch2 A	3	Channel 1, encoder input C	Channel 2, encoder input A
Ch1 DI/Ch2 B	4	Channel 1, digital input The input "Digital input" is internally connected to 5 V via a pull-up resistor. The encoder alarm output must actively pull the signal against GND. External power supply is not recommended. If an external supply is used, the maximum permitted voltage is 5 V against GND	Channel 2, encoder input B
Enc supply+	5	Encoder supply (5 V default, parameterizable 12 V, 24 V)	Encoder supply (5 V default, parameterizable 12 V, 24 V)
Enc supply-	6	0 V encoder supply	0 V encoder supply
Latch	7	Input "Latch extern"	Gate/Latch combination input for encoder 1
n.c.	8	Do not connect the terminal point	Do not connect the terminal point
Ch1 $\bar{A}$	9	Channel 1, encoder input $\bar{A}$	Channel 1, encoder input $\bar{A}$
Ch1 $\bar{B}$	10	Channel 1, encoder input $\bar{B}$	Channel 1, encoder input $\bar{B}$
Ch1 $\bar{C}$ / Ch2 $\bar{A}$	11	Channel 1, encoder input $\bar{C}$	Channel 2, encoder input $\bar{A}$
Ch2 $\bar{B}$	12		Channel 2, encoder input $\bar{B}$
Enc supply+	13	Encoder supply (5 V default, parameterizable 12 V, 24 V)	Encoder supply (5 V default, parameterizable 12 V, 24 V)
Enc supply-	14	0 V encoder supply	0 V encoder supply
Gate	15	The Gate input can also be used as Latch extern 2 input	Gate/Latch combination input for encoder 2
n.c.	16	Do not connect the terminal point	Do not connect the terminal point



Setting the encoder supply via index 0x8001:17 [► 151]

The encoder supply is set centrally for both channels via the index 0x8001:17 [► 151] (channel 1). The corresponding index 0x8011:17 of the second channel has no parameterization function.

NOTICE**Setting the encoder supply voltage**

- Before switching to a higher voltage, make sure that the connected encoders support the selected voltage range!
- To write to 0x80n1:17 "Supply voltage" you have to set the value 0x72657375 (ASCII: "user") in index [0xF008](#) [[▶ 182](#)] "Code word".

2.4.1 Single-channel mode (1 x A, B, C)

2.4.1.1 RS422 mode

NOTICE

Differential and single-ended connection

The RS422 signal transmits a differential voltage, which makes the signal less sensitive to interference compared to a single-ended signal.

- If the encoder signal is to be transmitted over longer distances or at higher frequencies, an encoder with RS422 signals is recommended.
- Shielded and twisted pair cables should be used.

Connection of RS422 encoders with or without zero pulse

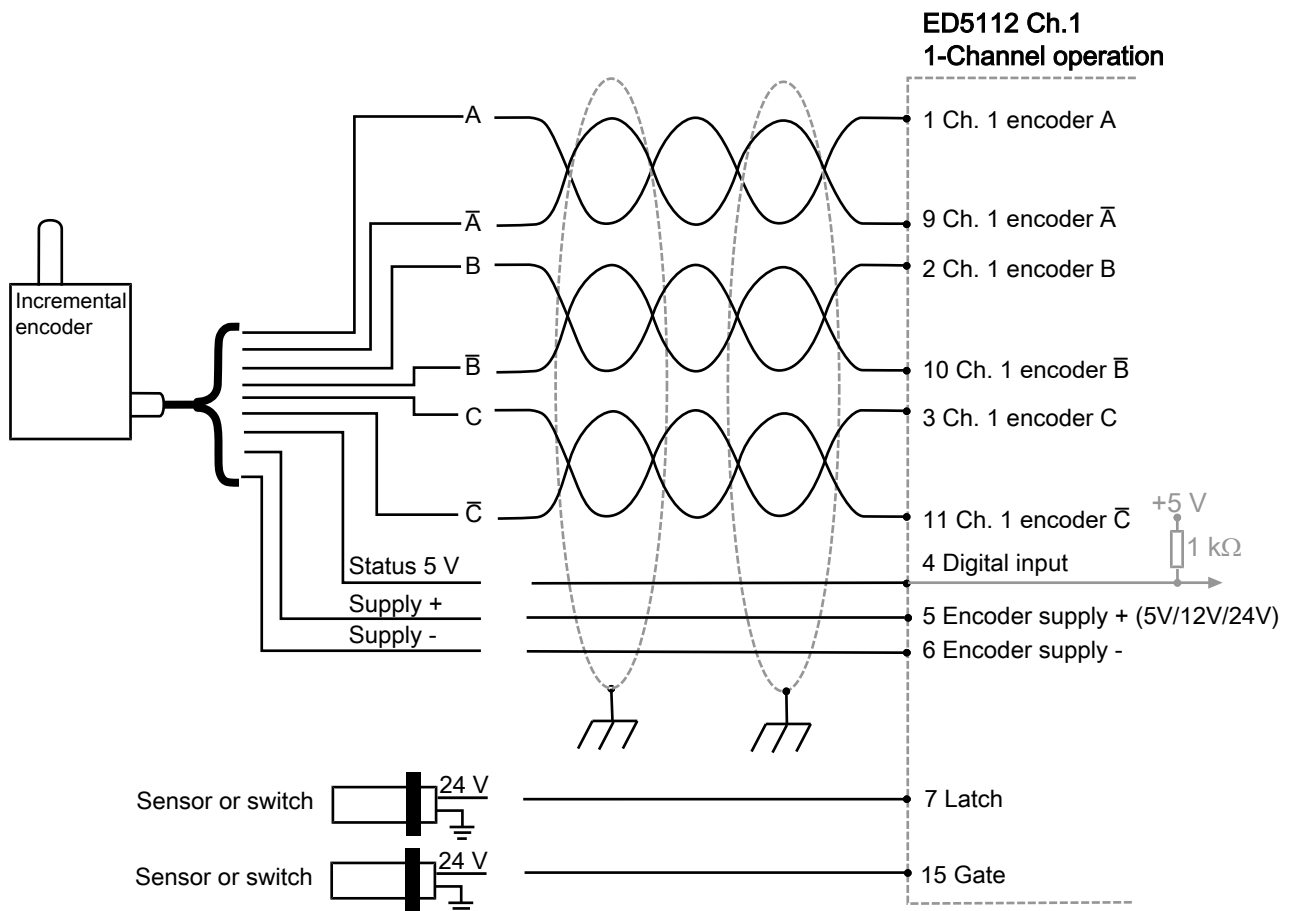


Fig. 5: Connection of RS422 encoders with zero pulse in 1-channel mode



Connection instructions

- When using an encoder without zero pulse C, the terminal points for the C track are not connected.

Connection of RS422 counters/pulse generators with or without zero pulse

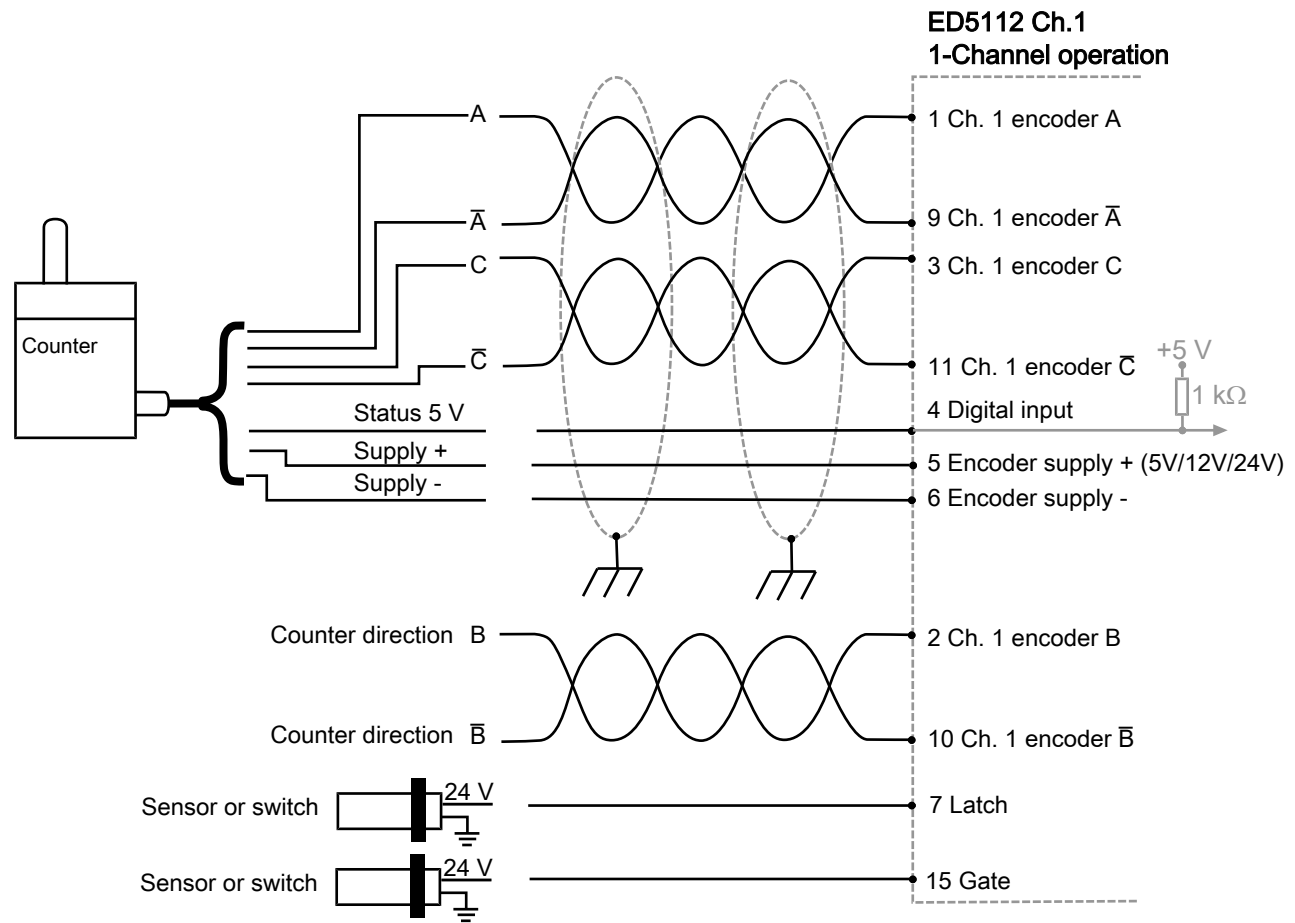


Fig. 6: Connection of RS422 counters/pulse generators with zero pulse in 1-channel mode



Connection instructions

- If a counter/pulse generator is connected, the B track determines the counting direction. In RS422 mode a differential signal is expected on the $\bar{B}$ track.
- When using a counter / pulse generator without zero pulse C, the terminal points for the C track are not connected.

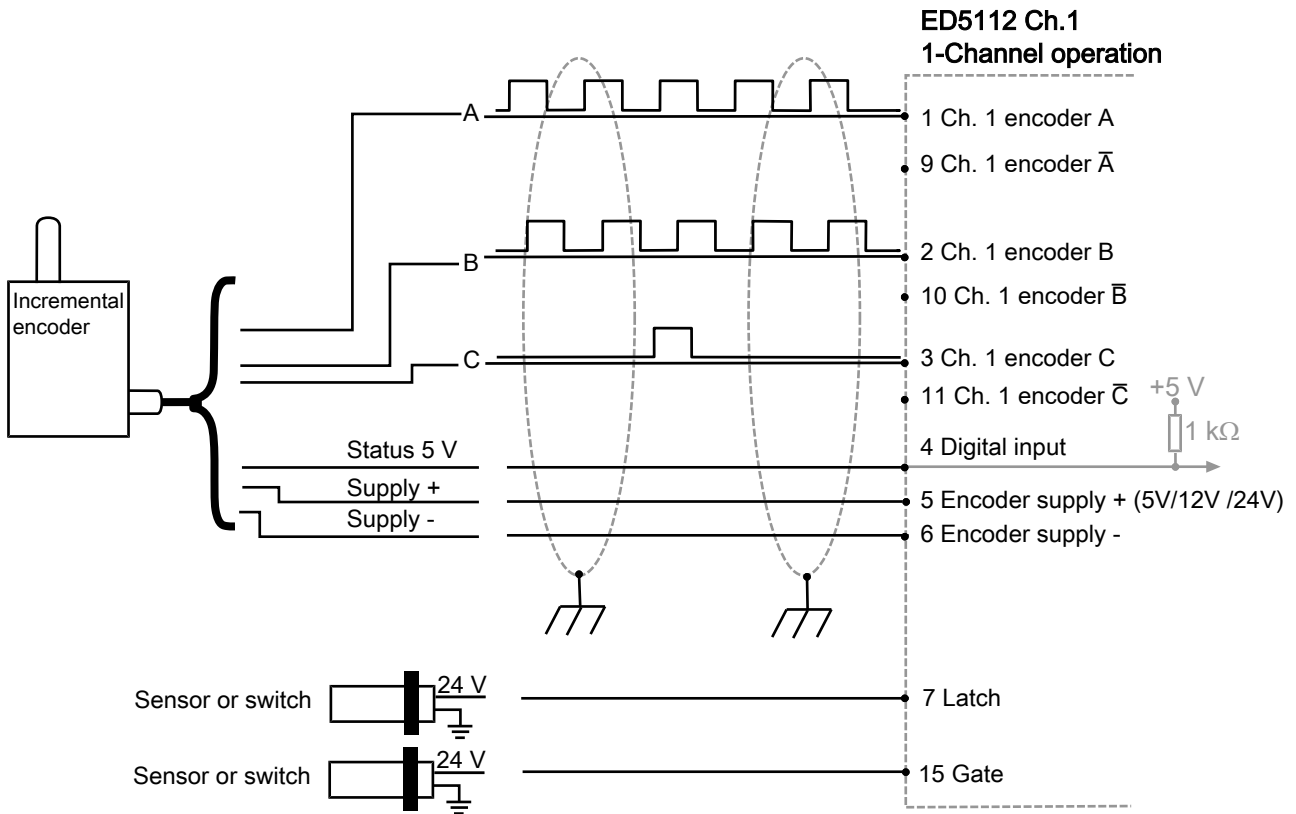
2.4.1.2 TTL mode**Connection of TTL encoders with or without zero pulse**

Fig. 7: Connection of TTL encoders with zero pulse in 1-channel mode

**Connection instructions**

- In TTL mode the inverse inputs are not connected.
- When using an encoder without zero pulse C, the terminal points for the C track are not connected.

Connection of TTL counters/pulse generators with or without zero pulse

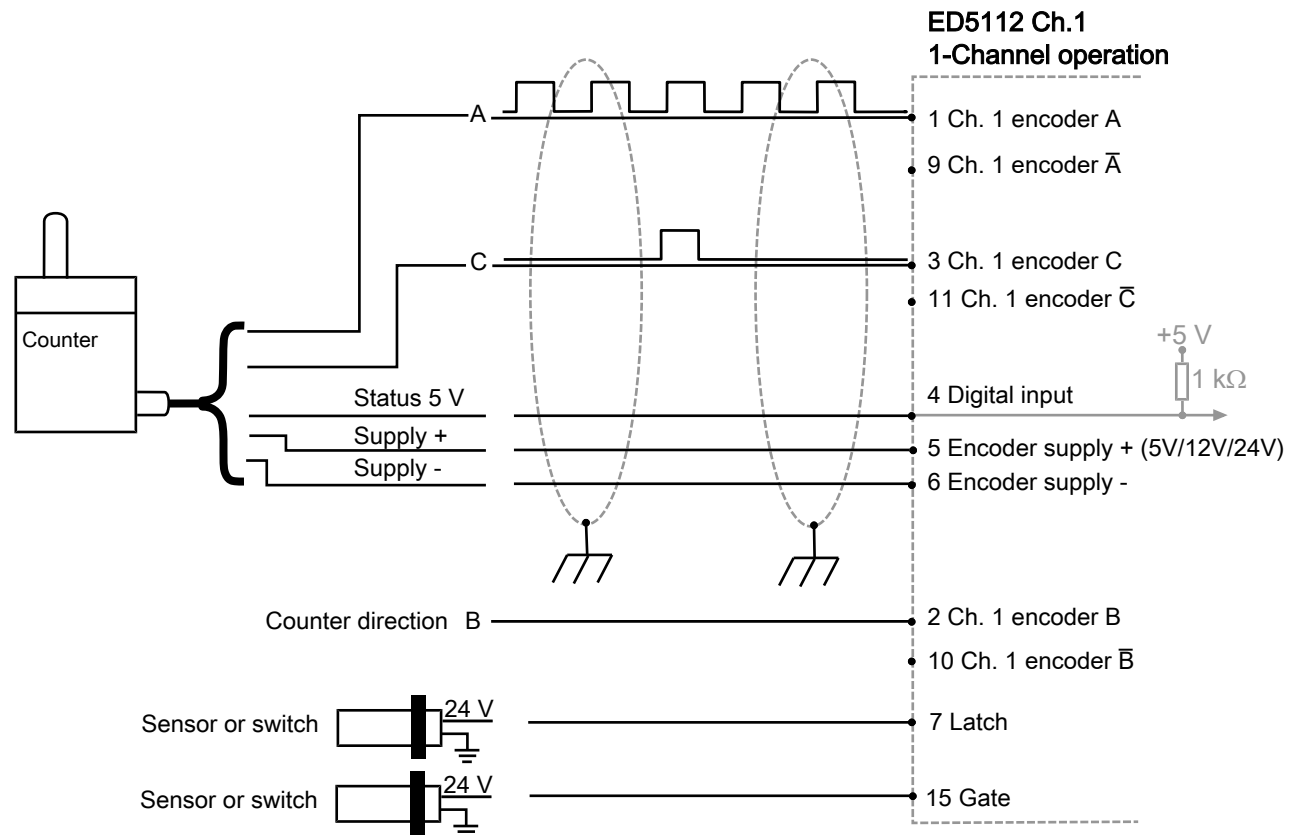


Fig. 8: Connection of TTL counters/pulse generators with zero pulse in 1-channel mode



Connection instructions

- In TTL mode the inverse inputs are not connected.
- If a counter/pulse generator is connected, the B track determines the counting direction. Input $\bar{B}$ is not connected.
- When using a counter/pulse generator without zero pulse C, the terminal points for the C track are not connected.

2.4.1.3 Open Collector mode

Connection of open collector encoders with or without zero pulse

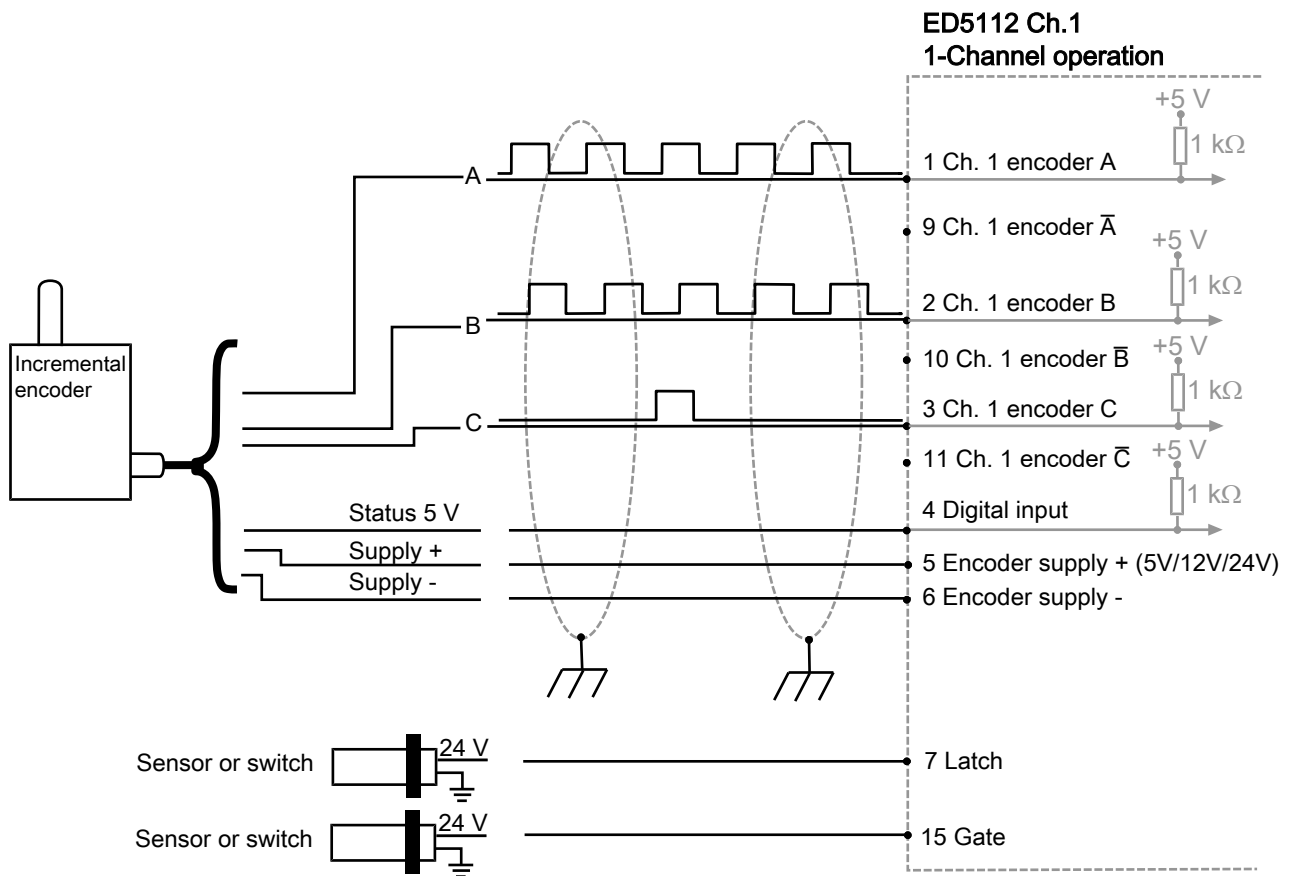


Fig. 9: Connection of open collector encoders with zero pulse in 1-channel mode



Connection instructions

- In open collector mode the inverse inputs are not connected.
- When using an encoder without zero pulse C, the terminal points for the C track are not connected.

Connection of open collector counters/pulse generators with or without zero pulse

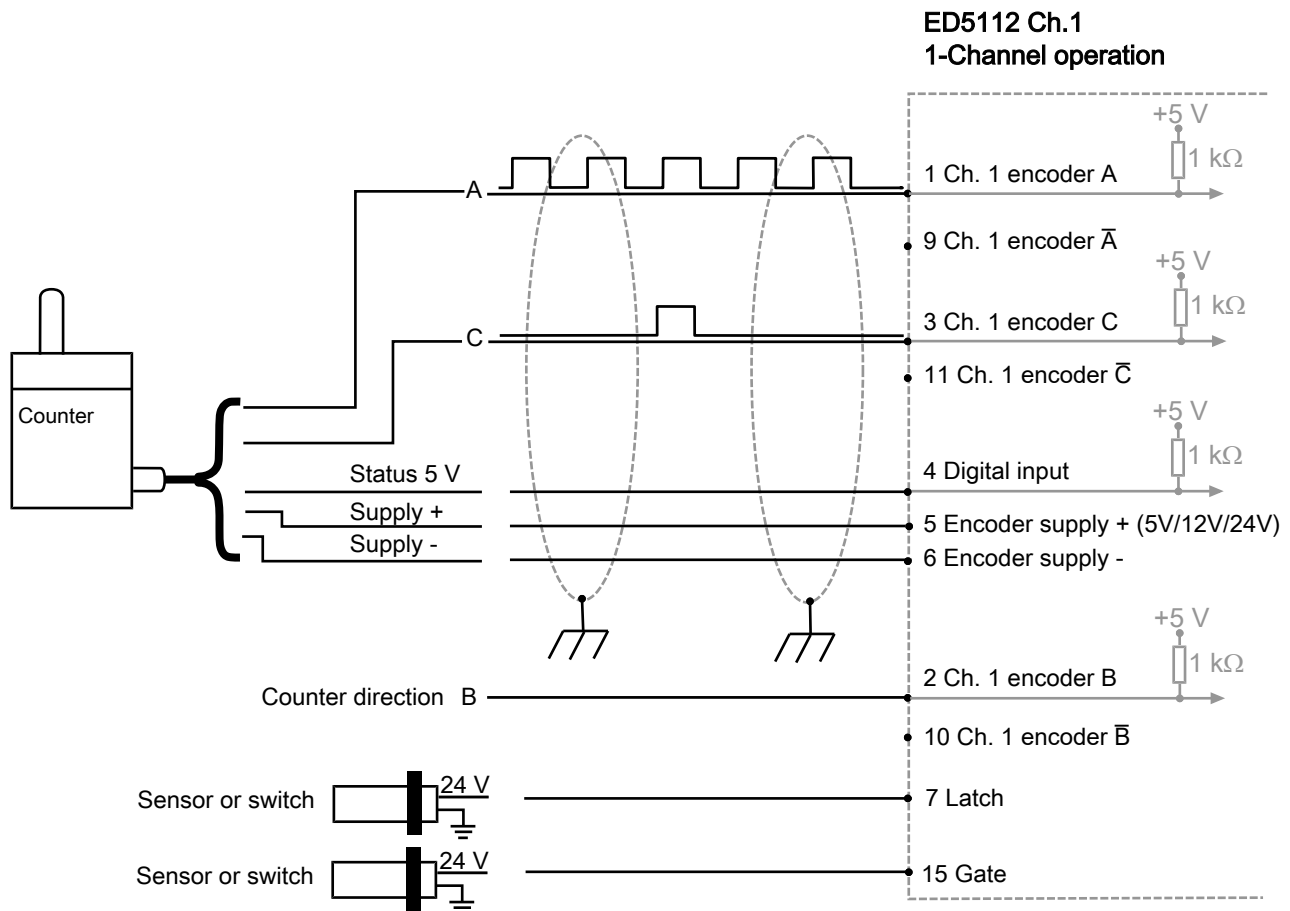


Fig. 10: Connection of open collector counters/pulse generators with zero pulse in 1-channel mode



Connection instructions

- In open collector mode the inverse inputs are not connected.
- If a counter/pulse generator is connected, the B track determines the counting direction. Input $\bar{B}$ is not connected.
- When using a counter/pulse generator without zero pulse C, the terminal points for the C track are not connected.

2.4.2 Two-channel mode (2 x A, B)

2.4.2.1 RS422 mode

NOTICE

Differential and single-ended connection

The RS422 signal transmits a differential voltage, which makes the signal less sensitive to interference compared to a single-ended signal.

- If the encoder signal is to be transmitted over longer distances or at higher frequencies, an encoder with RS422 signals is recommended.
- Shielded and twisted pair cables should be used.

Connection of RS422 encoders without zero pulse in 2-channel mode

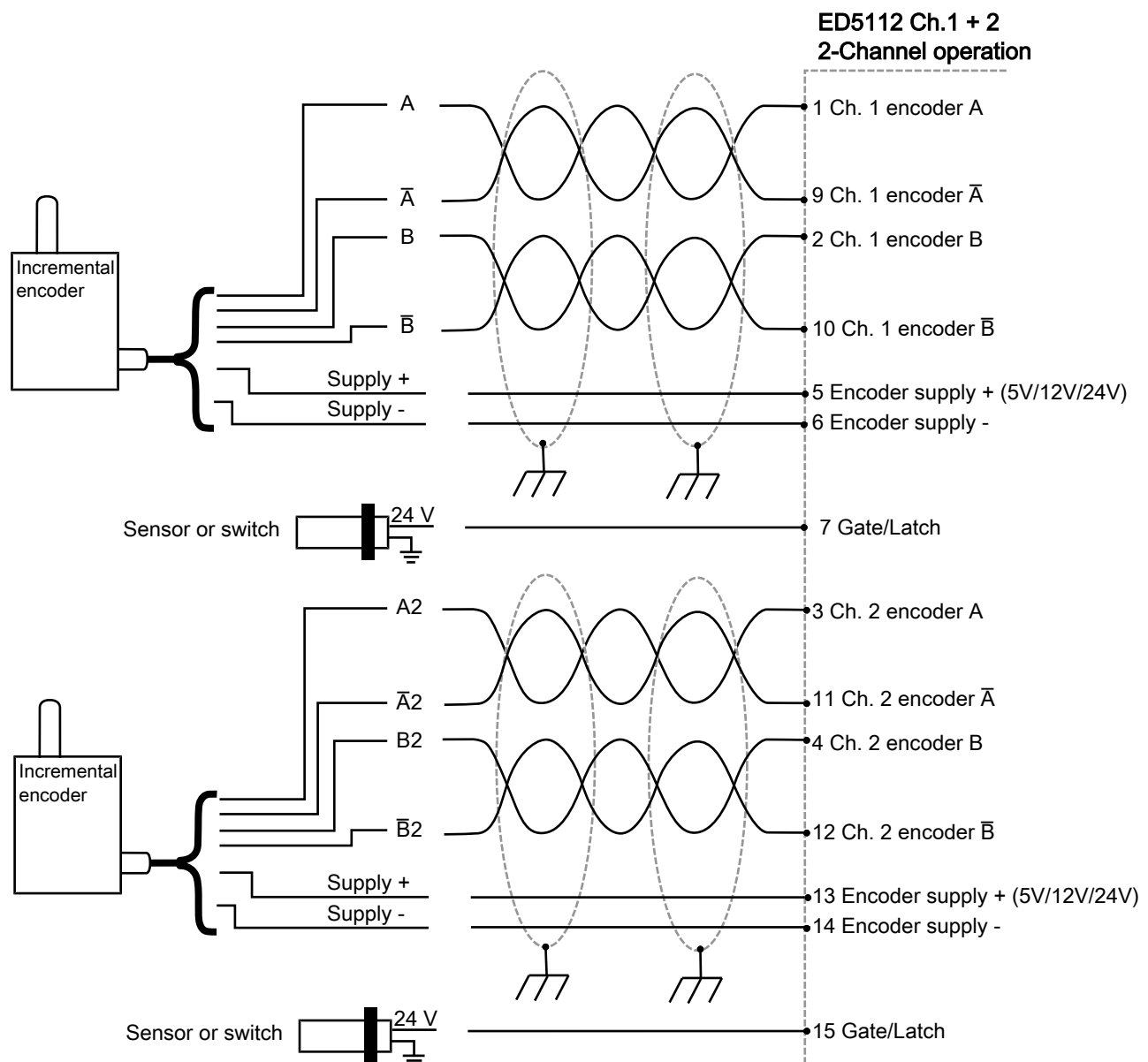


Fig. 11: Connection of RS422 encoders without zero pulse in 2-channel mode



Connection instructions

- In 2-channel mode only encoders without zero pulse C can be used. The terminal points for the C track are assigned the signals of the second A track.

Connection of RS422 counters/pulse generators without zero pulse in 2-channel mode

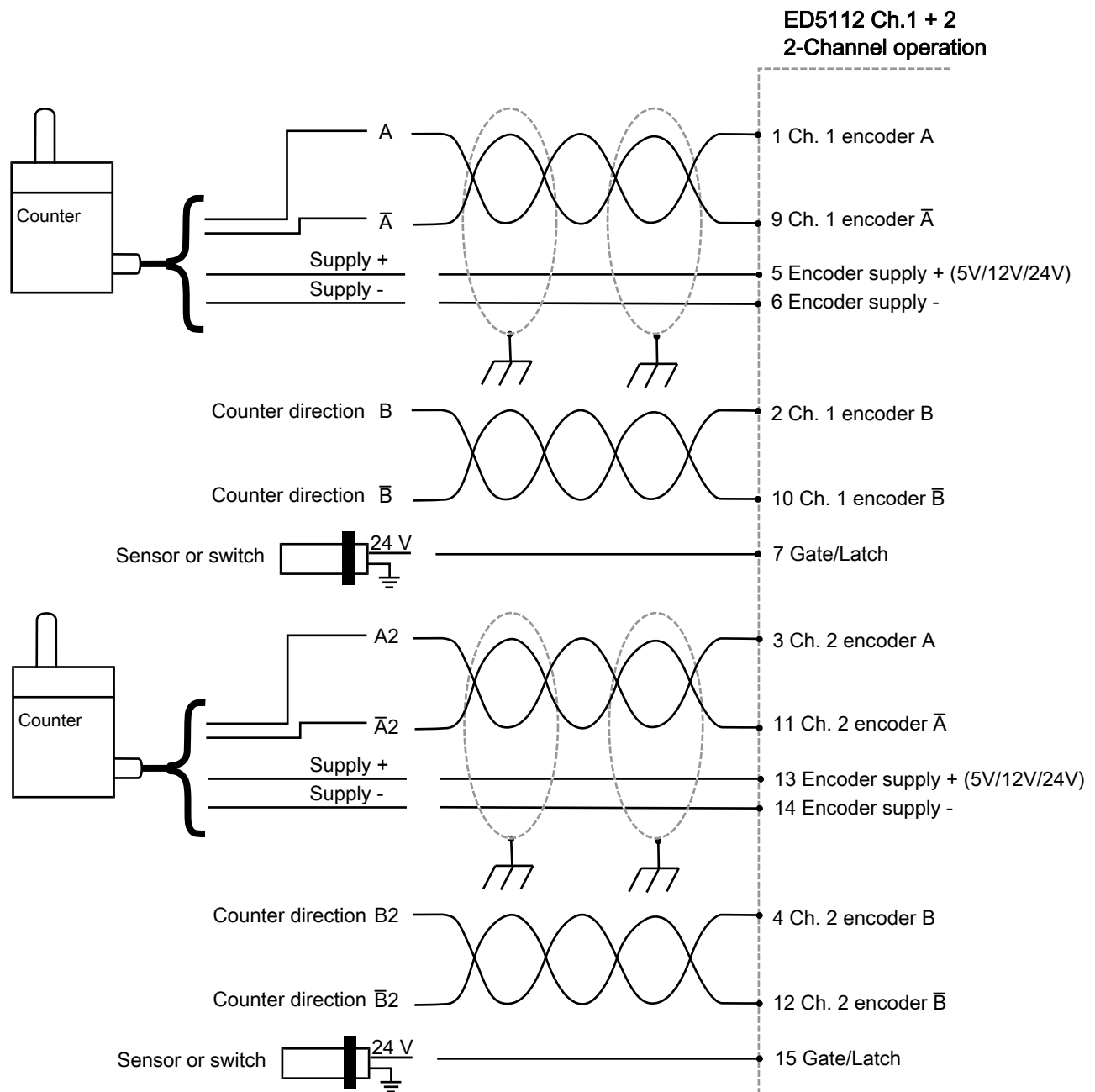


Fig. 12: Connection of RS422 counters/pulse generators without zero pulse in 2-channel mode



Connection instructions

- If a counter/pulse generator is connected, the B track determines the counting direction. In RS422 mode a differential signal is expected on the $\bar{B}$ track.
- Only counters/pulse generators without zero pulse are suitable for use in 2-channel mode. The terminal points of the C track are assigned the signals of the second A track.

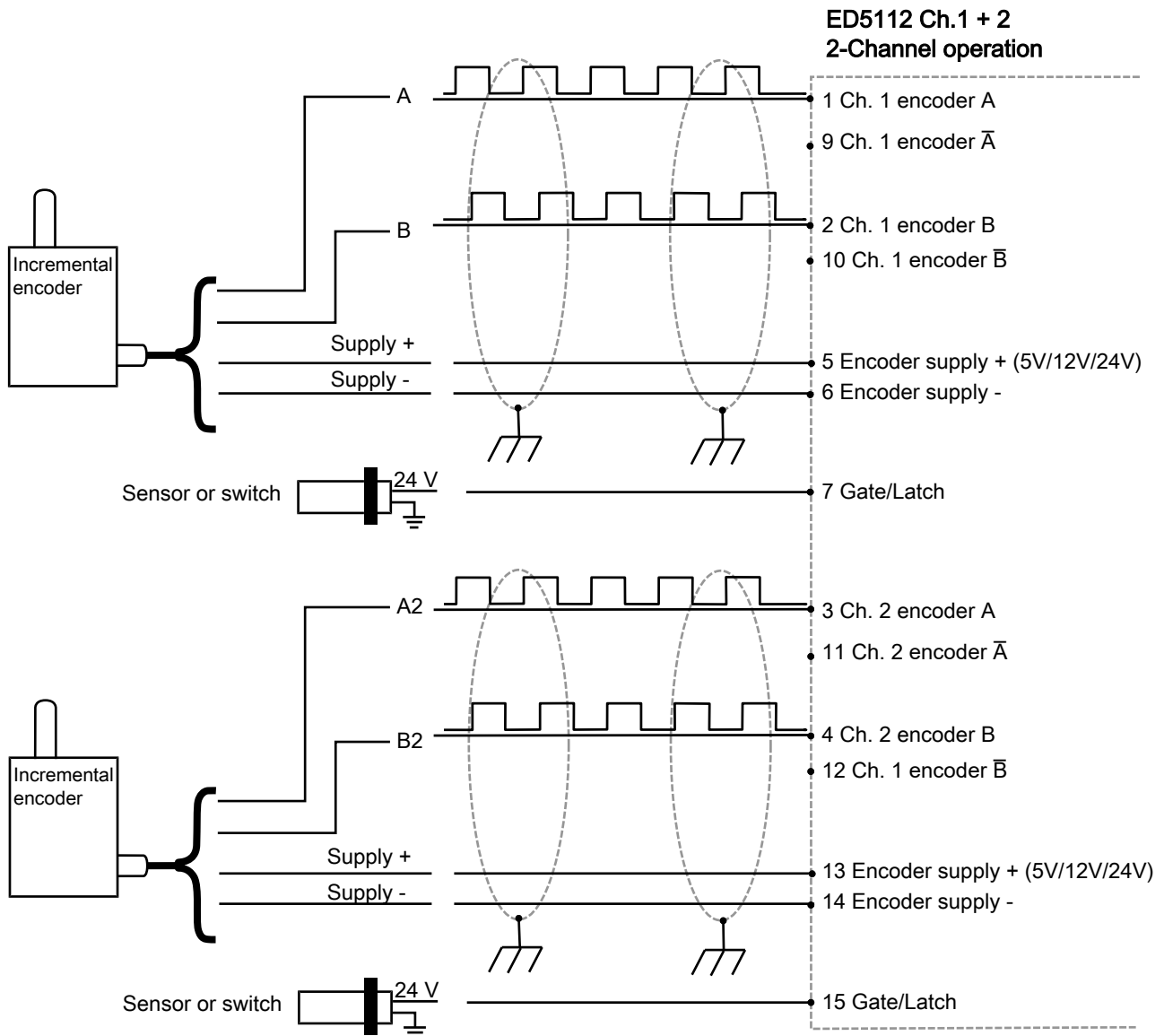
2.4.2.2 TTL mode**Connection of TTL encoders without zero pulse in 2-channel mode**

Fig. 13: Connection of TTL encoders without zero pulse in 2-channel mode

**Connection instructions**

- In TTL mode the inverse inputs are not connected.
- Only encoders without zero pulse are suitable for use in 2-channel mode. The terminal points for the C track are assigned the signals of the second A track.

Connection of TTL counters/pulse generators without zero pulse in 2-channel mode

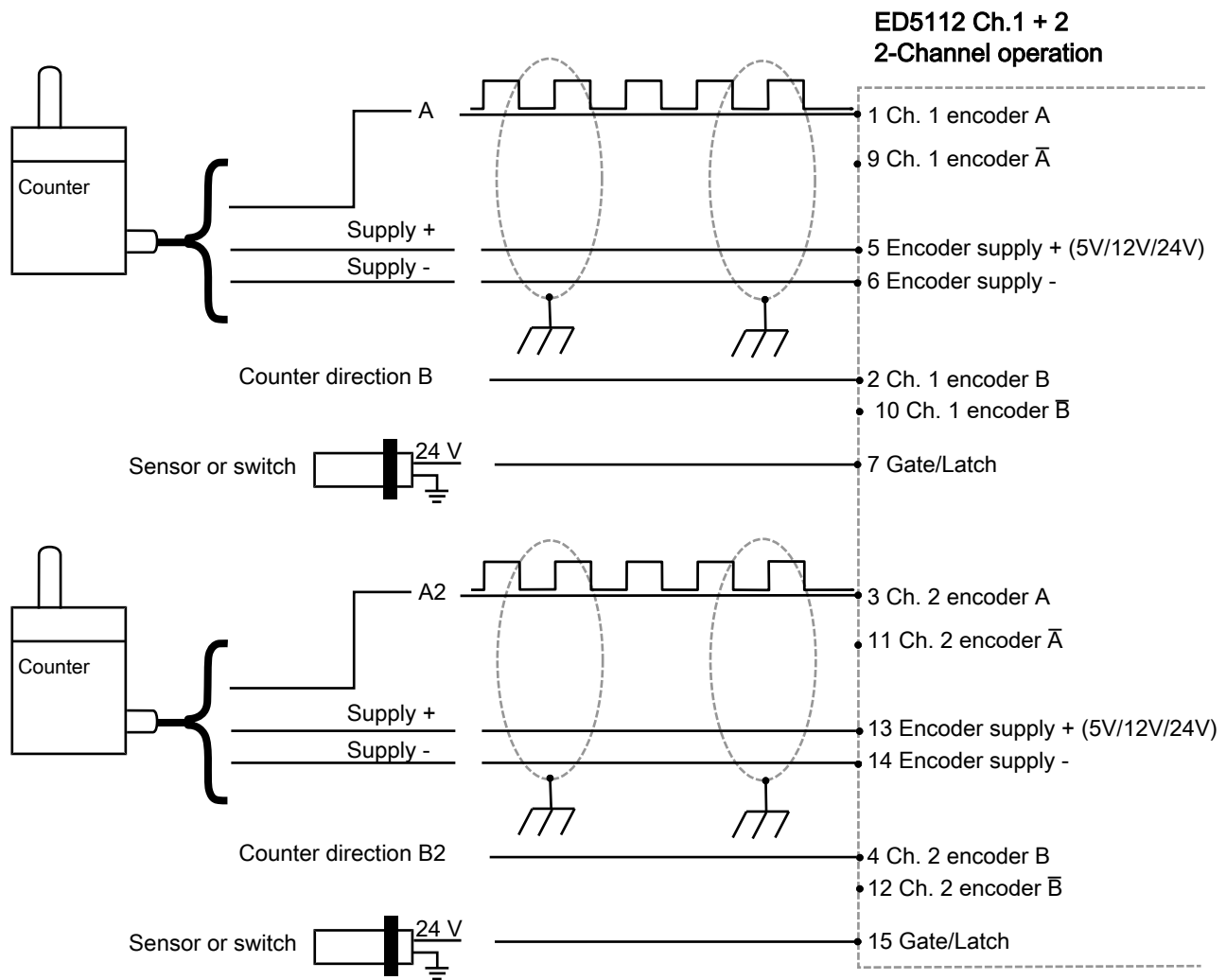


Fig. 14: Connection of TTL counters/pulse generators without zero pulse in 2-channel mode



Connection instructions

- In TTL mode the inverse inputs are not connected.
- If a counter/pulse generator is connected, the B track determines the counting direction. Input $\bar{B}$ is not connected.
- Only counters/pulse generators without zero pulse are suitable for use in 2-channel mode. The terminal points for the C track are assigned the signals of the second A track.

2.4.2.3 Open Collector mode

Connection of open collector encoders without zero pulse in 2-channel mode

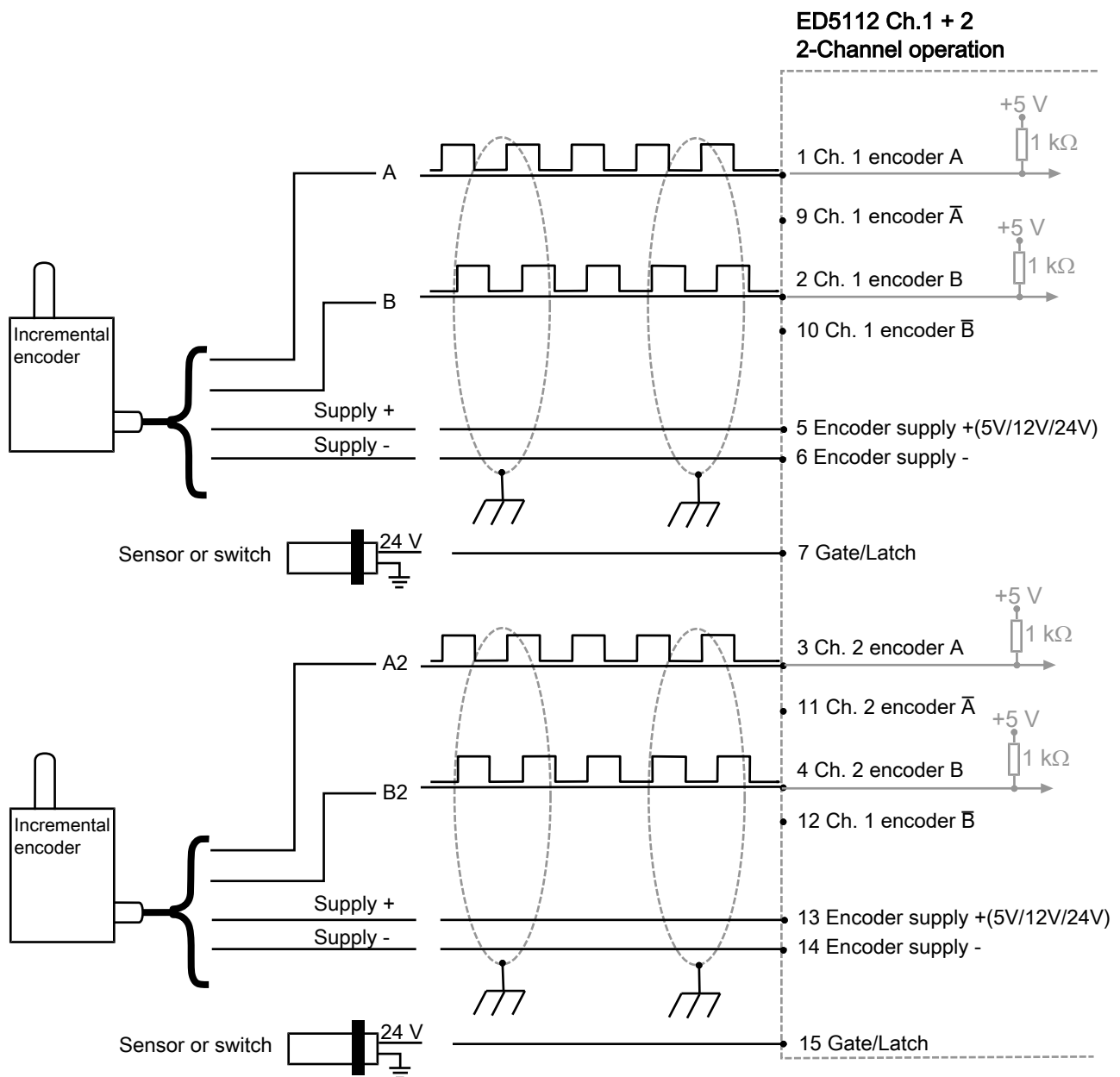


Fig. 15: Connection of open collector encoders without zero pulse in 2-channel mode



Connection instructions

- In open collector mode the inverse inputs are not connected.
- Only encoders without zero pulse are suitable for use in 2-channel mode. The terminal points for the C track are assigned the signals of the second A track.

Connection of open collector counters/pulse generators without zero pulse in 2-channel mode

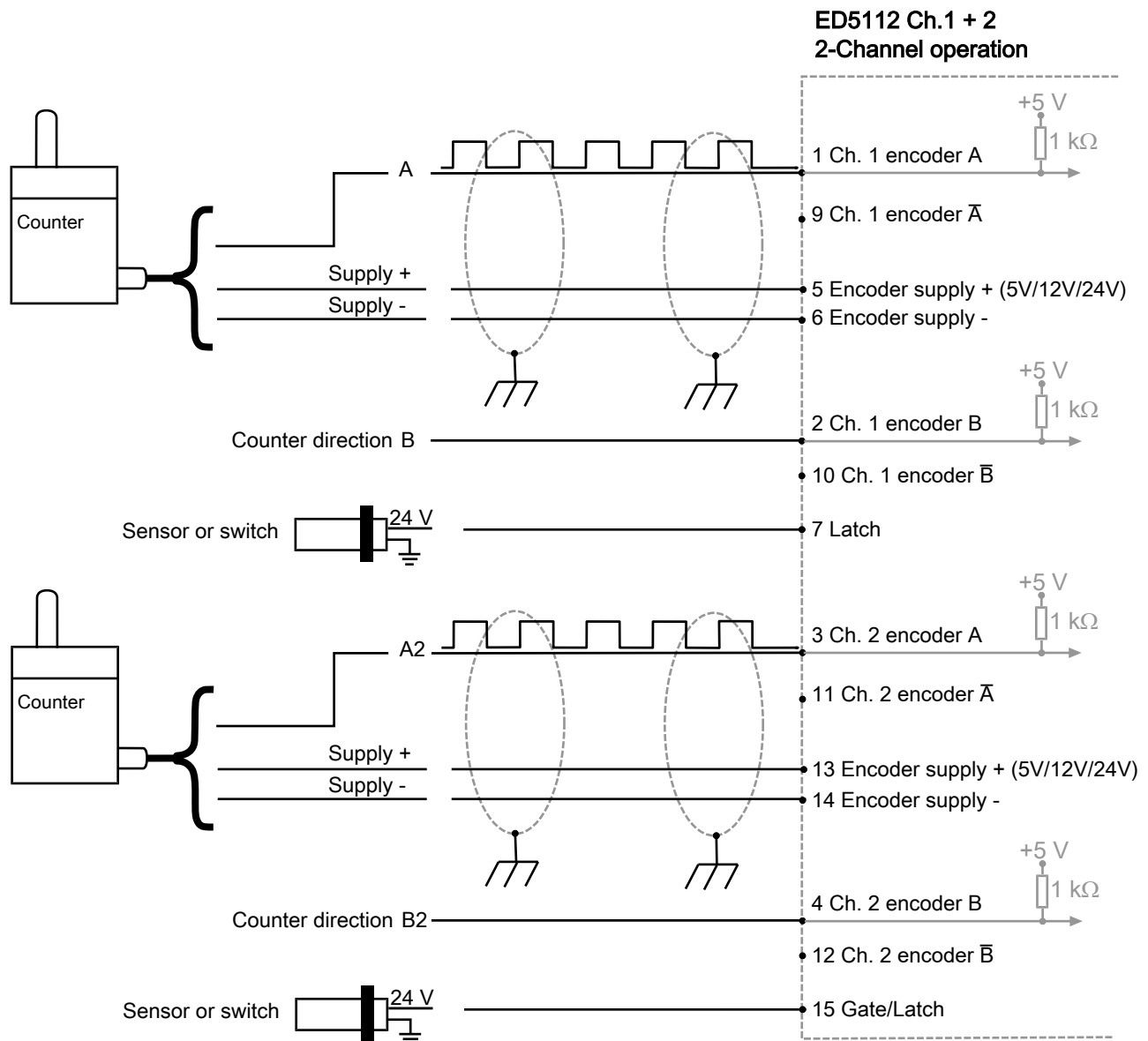


Fig. 16: Connection of open collector counters/pulse generators without zero pulse in 2-channel mode



Connection instructions

- In open collector mode the inverse inputs are not connected.
- If a counter/pulse generator is connected, the B track determines the counting direction. Input $\bar{B}$ is not connected.
- Only counters/pulse generators without zero pulse are suitable for use in 2-channel mode. The terminal points for the C track are assigned the signals of the second A track.

2.5 LEDs

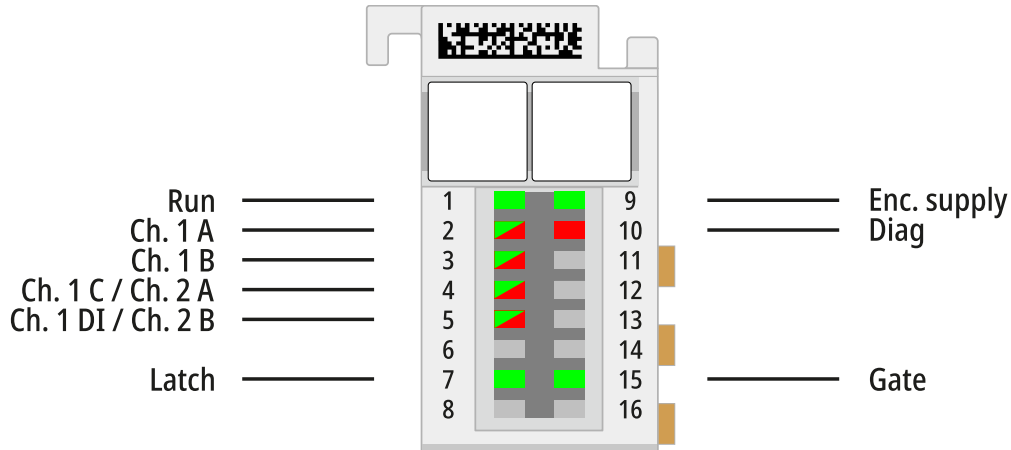


Fig. 17: ED5112 – LEDs

Name	No.	Color	Meaning
Run	1	green	This LED indicates the terminal's operating state: - off: State of the EtherCAT State Machine: INIT = initialization of the terminal - flashing: State of the EtherCAT State Machine: PREOP = function for mailbox communication and different default settings are applied - single flash: State of the EtherCAT State Machine: SAFEOP = verification of the <u>Sync Manager</u> channels and the distributed clocks. Outputs remain in safe state - on: State of the EtherCAT State Machine: OP = normal operating state; mailbox and process data communication is possible - flickering: State of the EtherCAT State Machine: BOOTSTRAP = Function for <u>Firmware updates</u> of the terminal
Ch. 1 A	2	green, red	green: Indicates TRUE level. red: Indicates wire break at the respective input. Diagnosis is only possible if the following three conditions are met. - The corresponding input is differentially wired. Corresponds to: "Counter mode" 0x8001:1D = 0 ("Encoder RS422 (diff. input)") - or "Counter mode" 0x8001:1D = 1 ("Counter RS422 (diff. input)") "Error detection" for the respective input is enabled: "Error detection A" 0x8000:0B = TRUE "Error detection B" 0x8000:0C = TRUE "Error detection C" 0x8000:0D = TRUE - The differential voltage $V_{ID\ Low}$ is typically less than 0.67 V (subject to change).
Ch. 1 B	3		
Ch. 1 C / Ch. 2 A	4		
Ch. 2 B	5		
Ch. 1 DI	5	green, red	Alarm input from encoder. Input is internally connected to 5 V via a pull-up resistor. The encoder output must actively pull the signal against GND. - green: Output active at the encoder, a fault message is present at the encoder - red: Output not active at the encoder; no fault message is present
Latch	7	green	Lights up if a signal (+24 V) is connected to the latch input
Enc. supply	9	green	Operating voltage display for incremental encoder power supply
Diag	10	red	Initialization process active or state of the EtherCAT State Machine: BOOT
Gate	15	green	Lights up if a signal (+24 V) is connected to the gate input

2.6 Incremental encoder basics

Incremental encoders divide a 360° rotation of the encoder axis into individual steps (increments) and mark a full revolution by means of a special mark (zero pulse). An RS422 encoder transmits the signal symmetrically as a differential line pair. TTL and Open Collector encoders use single signal lines (single-ended).

The module evaluates the 90° phase-shifted square wave signals of an incremental encoder on tracks A and B. The zero pulse is captured on track C. With a differential connection, the inverted signals ($\bar{A}$, $\bar{B}$, $\bar{C}$) are also recorded.

These signals are converted by means of the quadrature decoder and the 32-bit counter into a position value with optional quadruple, double or single evaluation. The digital inputs enable latch, reset and set functionalities and thus exact and speed-independent referencing and storage of the counter value.

Encoder type		Incremental signals
RS422 encoder	with zero pulse	A, $\bar{A}$, B, $\bar{B}$, C, $\bar{C}$
RS422 encoder	without zero pulse	A, $\bar{A}$, B, $\bar{B}$
RS422 counter or pulse generator	with zero pulse	A, $\bar{A}$, C, $\bar{C}$; counting direction specification via track B ($\bar{B}$)
RS422 counter or pulse generator	without zero pulse	A, $\bar{A}$; counting direction specification via track B ($\bar{B}$)
TTL, Open Collector encoder	with zero pulse	A, B, C
TTL, Open Collector encoder	without zero pulse	A, B
TTL, Open Collector counter or pulse generator	with zero pulse	A, C; counting direction specification via B
TTL, Open Collector counter or pulse generator	without zero pulse	A, counting direction specification via B

The phase position between the signals at track A and track B determines the counting direction.

Forward (cw): signal at track A is 90° leading with respect to track B

Backward (ccw): signal at track A is 90° lagging compared to track B.

With 1-fold evaluation the rising edges on track A are counted.

With 2-fold evaluation, the rising and falling edges on track A are counted.

With 4-fold evaluation, the rising and falling edges on track A and track B are counted.

Cyclical output

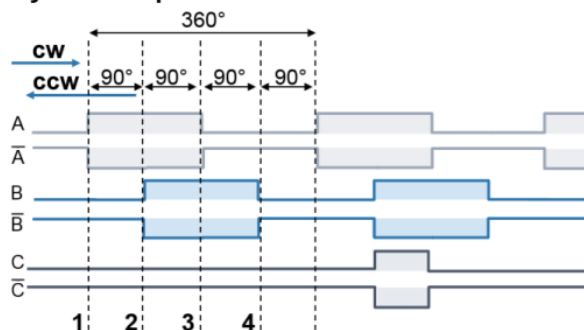


Fig. 18: Incremental signals

Absolute value encoders provide an absolute position value directly after switch-on, which is unambiguous over the entire travel path. With incremental encoders, a homing must be carried out after switching on in order to be able to determine a unique position.

Homing can be carried out, for example, with the aid of referencing cams or via the zero pulse of the encoder.

NOTICE

Differential and single-ended connection

The RS422 signal transmits a differential voltage, which makes the signal less sensitive to interference compared to a single-ended signal.

- If the encoder signal is to be transmitted over longer distances or at higher frequencies, an encoder with RS422 signals is recommended.
- Shielded and twisted pair cables should be used.

3 Mounting and wiring

3.1 Notes on ESD protection

NOTICE

Devices can be destroyed by electrostatic charging!

The devices contain electrostatically sensitive components which can be damaged by improper handling.

- When handling the components, take care to avoid electrostatic discharge; also, prevent direct contact with the spring-loaded contacts (see illustration).
- Contact with highly insulating materials (synthetic fibers, plastic films, etc.) should be avoided when simultaneously handling components.
- When handling the components, ensure proper earthing of the environment (workplace, packaging, and persons).
- Each bus station must be terminated with the [EL9011](#) or [EL9012](#) end cap on its right side to guarantee the protection rating and ESD protection.

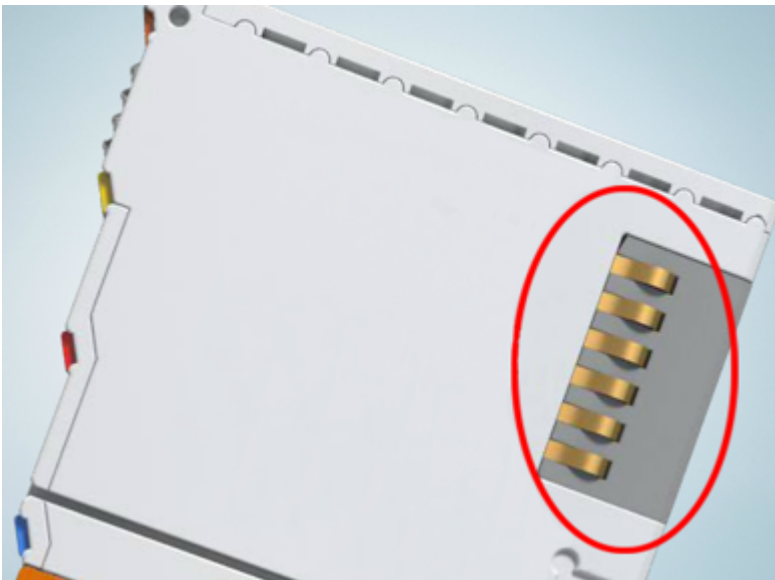


Fig. 19: Spring contacts of Beckhoff I/O components

3.2 Mounting rail installation

⚠ WARNING

Risk of injury through electric shock and damage to the device!

Bring the bus terminal system into a safe, de-energized state before beginning to mount, disassemble, or wire the bus terminals!

The bus terminal system is designed for installation in a control cabinet or junction box.

Installation

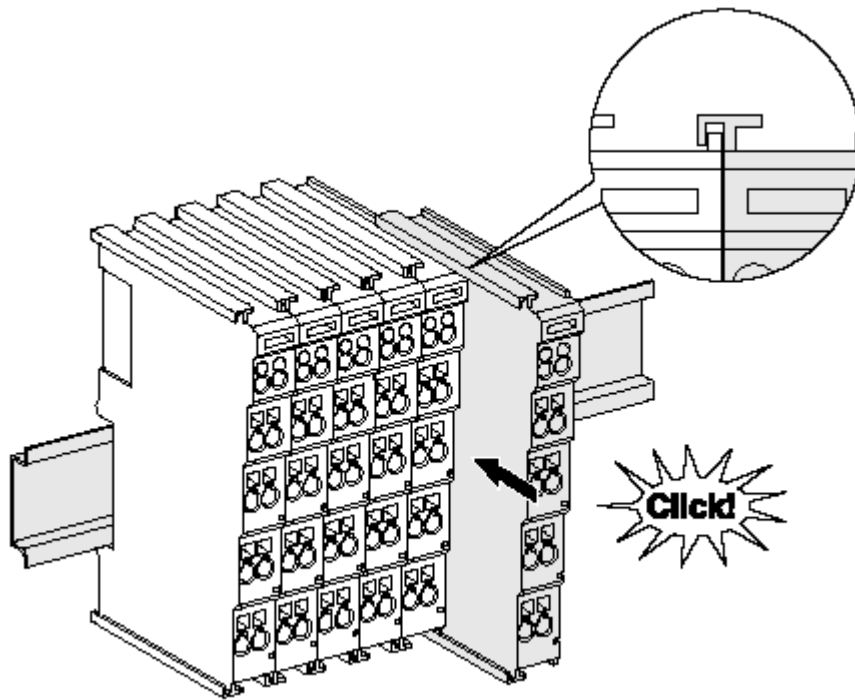


Fig. 20: Installation on the mounting rail

The bus couplers and bus terminals are attached to commercially available 35 mm mounting rails (DIN rail according to EN 60715) by applying slight pressure:

1. First attach the fieldbus coupler to the mounting rail.
2. The bus terminals are now attached on the right-hand side of the fieldbus coupler. To do this, connect the components with the slot and key and push the terminals against the mounting rail until the latch audibly engages on the mounting rail.

If you snap the terminals onto the mounting rail first and then push them next to each other without the slot and key engaging, no functional connection will be established! When correctly assembled, no significant gap should be visible between the housing units.

● Fastening the mounting rails

i The locking mechanism of the terminals and couplers protrudes into the profile of the mounting rail. When installing the components, make sure that the locking mechanism doesn't come into conflict with the fixing bolts of the mounting rail. When fastening mounting rails with a height of 7.5 mm under the terminals and couplers, use flat fastening components such as countersunk head screws or blind rivets.

NOTICE

Earth the mounting rail!

Make sure the mounting rail is properly earthed.

Connections within a bus terminal block

The electric connections between the bus coupler and the bus terminals are made automatically by joining the components:

- The six spring-loaded contacts of the E-bus/K-bus deal with the data transfer and the supply of the bus terminal electronics.
- The power contacts deal with the supply for the field electronics and thus represent a supply rail within the bus terminal block. The power contacts are supplied via terminal points on the bus coupler (up to 24 V) or via power supply terminals for higher voltages.

i Power contacts

When configuring a bus terminal block, note the contact assignments of the individual bus terminals, as some types

- do not loop through the power contacts or do not loop them through completely (e. g. analog bus terminals or digital 4-channel bus terminals),
- the power contacts are disconnected, thus marking the start of a new supply rail (power supply terminals).

Power contact $\perp$

The power contact marked $\perp$ (ground connection in accordance with IEC 60417-5017) can be used as a ground. For safety reasons this contact mates first when plugging together, and can ground short-circuit currents of up to 125 A.

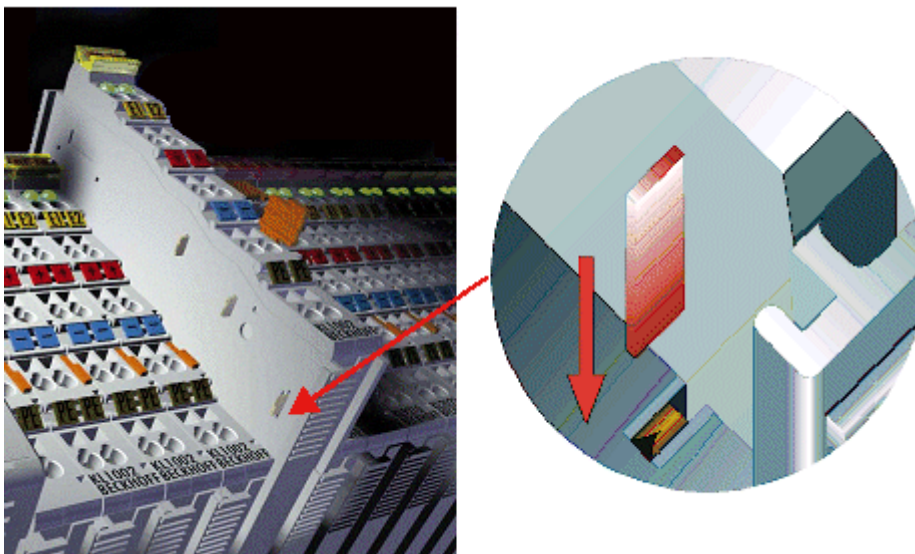


Fig. 21: Power contact on the left

⚠ WARNING

Risk of injury from electric shock!

The power contact marked $\perp$ may not be used for other potentials!

NOTICE

Risk of damage to the device

Note that, for electromagnetic compatibility, the earth contacts are capacitatively coupled to the mounting rail. This may lead to incorrect results during insulation testing or to damage to the terminal (e.g. disruptive discharge to the earth line during insulation testing of a consumer with a rated voltage of 230 V). For insulation testing, disconnect the earth supply line at the bus coupler or the power supply terminal! In order to decouple further supply points for testing, these power supply terminals can be released and pulled at least 10 mm from the group of terminals.

Disassembly

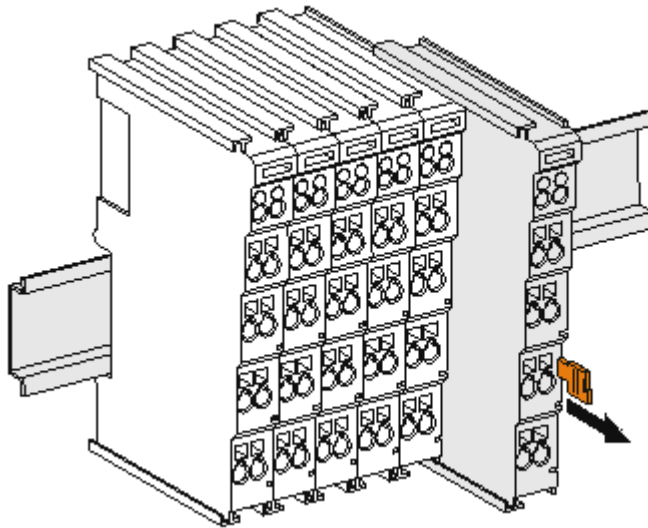


Fig. 22: Removal from mounting rail

Each terminal is secured by a lock on the mounting rail, which must be released for disassembly:

1. Pull down the terminal at its orange-colored straps from the mounting rail by approx. 1 cm. The rail locking of this terminal is automatically released, and you can now pull the terminal out of the bus terminal block with little effort.
2. To do this, grasp the unlocked terminal simultaneously at the top and bottom of the housing surfaces with your thumb and index finger and pull it out of the bus terminal block.

3.3 Positioning of passive terminals



Note on the placement of passive terminals in the bus terminal block

EtherCAT Terminals that do not take part in active data exchange within the bus terminal block are referred to as passive terminals. These terminals can be recognized because they do not consume power from the E-bus. To ensure optimal data exchange, no more than two passive terminals may be connected directly to each other!

Examples of the placement of passive terminals (highlighted in light color)

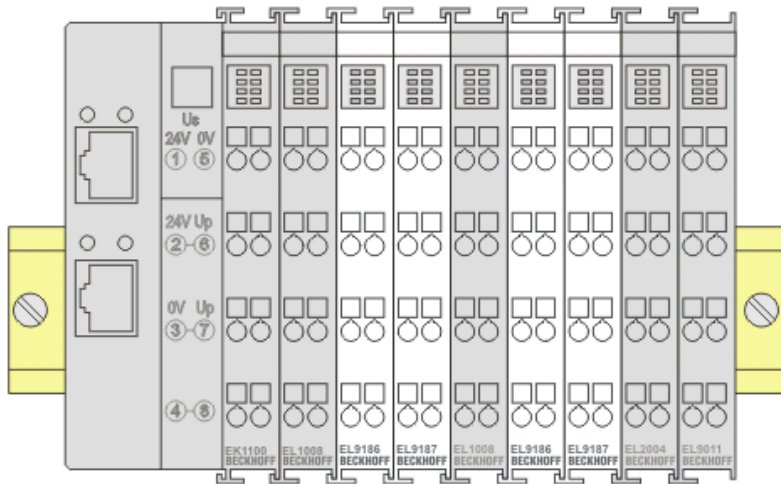


Fig. 23: Proper positioning

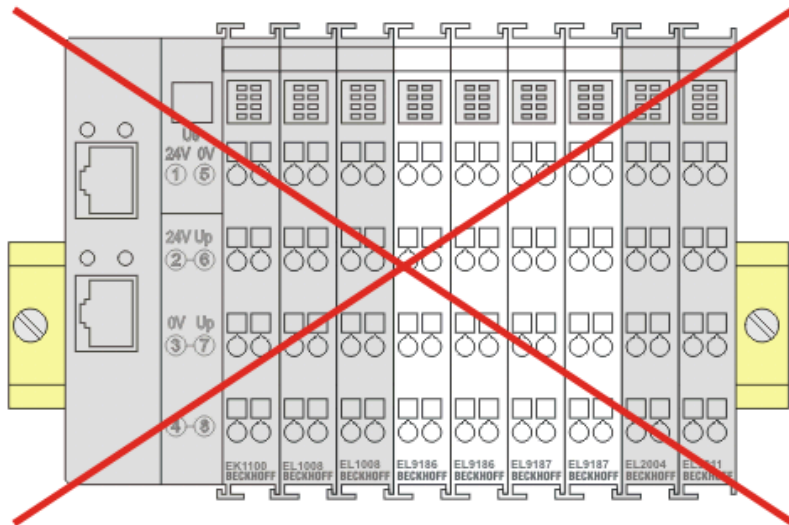


Fig. 24: Incorrect positioning

3.4 Installation positions

NOTICE

Constraints regarding installation position and operating temperature range

- Please refer to the technical data of the device to ascertain whether any restrictions regarding the installation position and/or the operating temperature range have been specified.
- When installing devices with increased heat dissipation, ensure that there is sufficient space above and below the devices during operation to guarantee adequate ventilation!

The installation positions and their names for mounting devices on mounting rails are specified below. The illustration of the devices in the following figures is an example.

The following applies to all installation positions: the reference direction “down” (see arrow) is the direction of the earth's gravitational force.

Horizontal installation (standard installation)

The mounting rail is mounted horizontally on a vertical mounting plate.
The connection level of the devices points to the front.

The devices are ventilated from below, which enables optimum cooling of the electronics through convection. This is therefore also the recommended installation position.

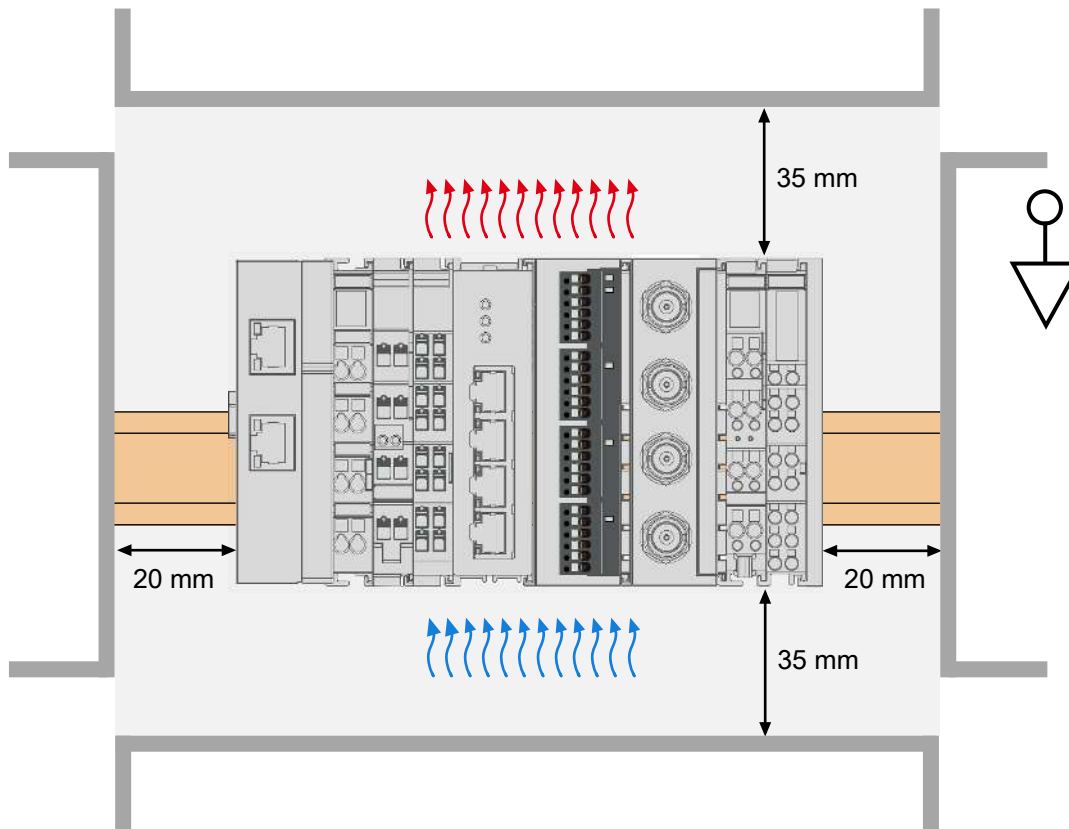


Fig. 25: Recommended minimum distances for standard installation position

NOTICE

Compliance with the minimum distances

Compliance with the minimum distances shown in the figure “Recommended minimum distances for standard installation position” is strongly recommended in all installation positions.

Vertical installation

The mounting rail is mounted vertically on a vertical mounting plate.
The connection level of the devices faces the front.
The devices can be arranged as follows:

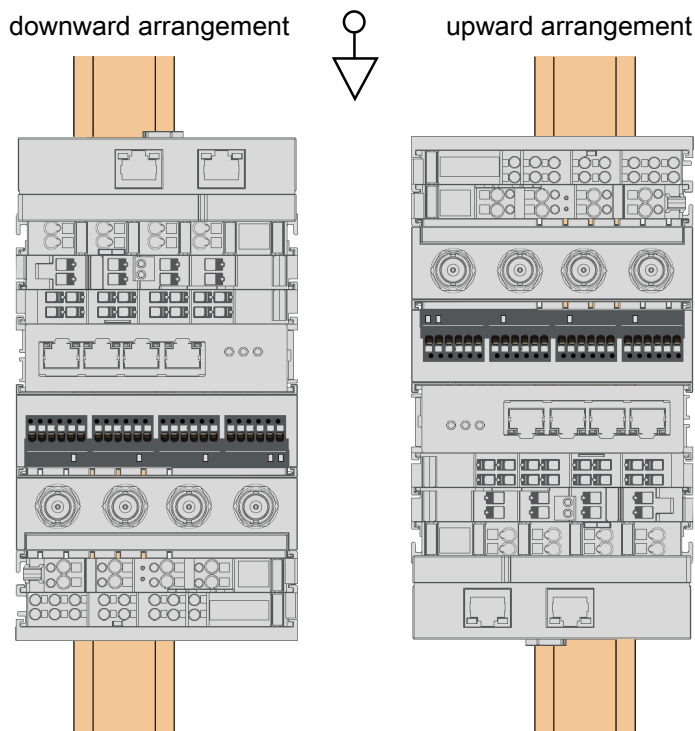


Fig. 26: Installation position: Vertical, downward arrangement (left)/upward arrangement (right)

Flat installation

The mounting rail is mounted on a horizontal mounting plate.
The connection level of the devices points upwards.

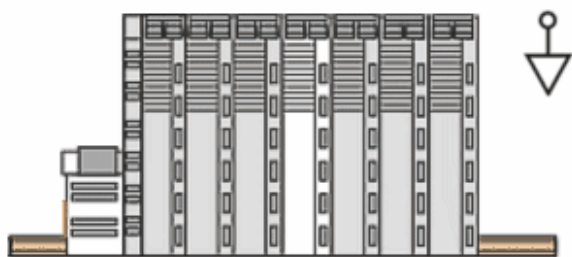


Fig. 27: Flat installation

NOTICE

Danger of sliding off the mounting rail

Particularly in the “vertical” installation position, but also in other installation positions under corresponding mechanical load, the terminal segment may move on the mounting rail. These can lead to undesirable malfunctions.

- If this risk exists, secure the terminal segment with appropriate locking devices, e.g. by clamping it to the mounting rail.

NOTICE

Compliance with the minimum distances

Compliance with the minimum distances shown in the figure “Recommended minimum distances for standard installation position” is strongly recommended in all installation positions.

Installation positions with ZB8610 fan cartridge

If the cooling should or must be increased for the intended application, the ZB8610 fan cartridge can be mounted on the underside of the device. In the horizontal installation position, the devices are ventilated from bottom to top by the fan cartridge. This optimum cooling is further enhanced by convection ventilation (see following figure).

The fan cartridge can be used in any installation position.

Further information on operation with and without a fan can be found in the technical data for the device (e.g. derating, information on installation positions, etc.).

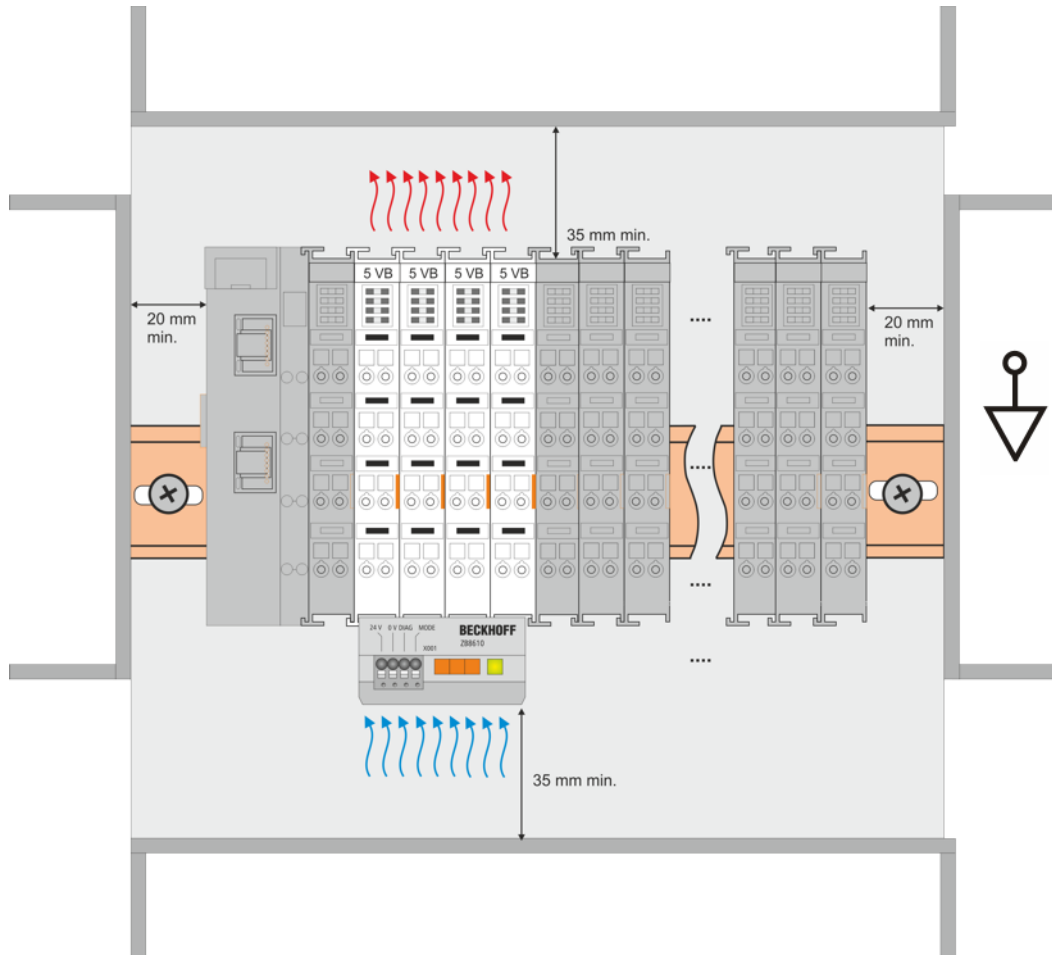


Fig. 28: Recommended minimum distances for operation with fan, using horizontal installation position as an example

NOTICE

Compliance with the minimum distances

Compliance with the minimum distances as shown in the figure “Recommended minimum distances for operation with fan” is strongly recommended.

3.5 Push-in connection technology (EC/ED/EFxxxx)

⚠ WARNING

Risk of injury through electric shock and damage to the device!

Bring the bus terminal system into a safe, de-energized state before beginning to mount, disassemble, or wire the bus terminals!

In the case of EC/ED/EFxxxx-series Terminals with push-in connection technology, solid conductors fitted with wire end ferrules can be plugged in directly without tools (see “Wiring [► 45]” section).

● Ultrasonically compacted wires

i Ultrasonically compacted (ultrasonically welded) wires can also be connected.

- Please note the information on the connection cross-section in the table “housing data” in the chapter “Technical data” of the relevant device!



Fig. 29: Tool-free push-in connection; housing types ED-12-8pin, ED-12-16pin, and EF-12-8pin

The following connection options are available for optimum adaptation to the application:

- The EC/EDxxxx-series Terminals contain electronics and the connection level in one housing unit.
- The EFxxxx-series Terminals have a pluggable connection level. For servicing, the pluggable connection level allows the entire wiring to be removed from the top of the housing as a single plug. This reduces the installation time and eliminates the risk of wires being mixed up. The plug is only slightly protruding (for dimensions, see “Technical data” -> “Housing data” of the corresponding product).
Installation and wiring are carried out as for the EDxxxx-series Terminals.
Proceed as follows when replacing:
 - Press the unlocking hub and pull the lower part out of the terminal block.
 - Push in the replacement component and plug the connector with the upright wiring back in.

● Strain relief of the cable

i A tab for strain relief of the cable simplifies assembly in many applications and prevents entangling of the individual connection wires when the connector is pulled.

Overview of housing designs

EC/EDxxxx housing designs, contain the electronics and connection level in one housing	EFxxxx housing designs with pluggable wiring level	Description
EC-40-8pin	-	8 connection points on 40 mm
ED-12-8pin	EF-12-8pin	8 connection points on 12 mm
ED-24-2x8pin	EF-24-2x8pin	16 connection points on 24 mm
ED-12-16pin	-	16 connection points on 12 mm
ED-24-2x16pin	-	32 connection points on 24 mm

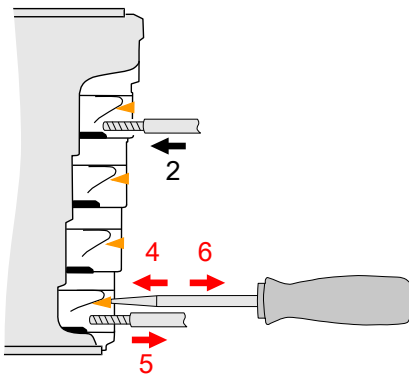
3.5.1 EC/ED/EFxxxx wiring with push-in connection technology

⚠ WARNING

Risk of injury through electric shock and damage to the device!

Bring the bus terminal system into a safe, de-energized state before beginning to mount, disassemble, or wire the bus terminals!

1.) Tool-free connection for solid conductors and conductors with ferrules



2.) Connection by push-button actuation for stranded wire conductors and **loosening the conductor (with tools)**

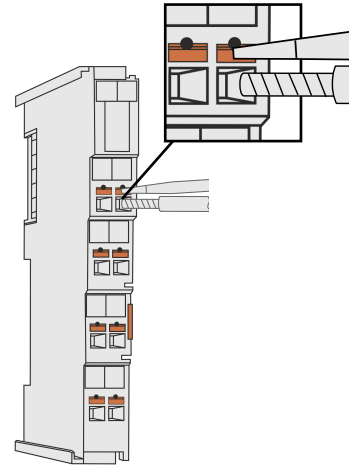
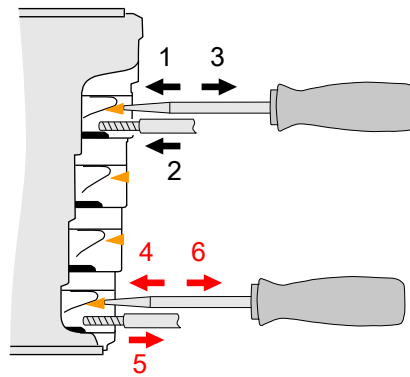


Fig. 30: Connecting and disconnecting the conductors

1. Connecting solid conductors and conductors with ferrules (Fig. top left, step 2)

These can be connected using a direct plug-in technique, without tools.

- Insert the conductor into the terminal point after stripping the insulation (2)

2. Connect stranded cables (Fig. top right, steps 1–3)

These must be connected via the push-button.

- Use a screwdriver to press the push-button to open the contact point (1).
- Then insert the conductor (2).
- Release the push-button by pulling back the screwdriver to close the terminal point (3).

Disconnect cables (Fig. above steps 4–6)

The release is performed using the push-button for all conductor types.

- Use a screwdriver to press the push-button to unlock the contact (4).
- Then pull out the conductor (5).
- Release the push-button by pulling back the screwdriver to close the terminal point (6).

NOTICE



Observe the permissible connection cross-sections and stripping lengths

The permissible conductor cross-section and stripping length depend on the type of housing, please refer to the housing data in the "Technical data" chapter for the device in question.

3.5.2 Shielding



Shielding

Encoders, analog sensors, and actuators should always be connected with shielded, pair-wise twisted cables.

3.6 Note on power supply

WARNING

Power supply from SELV / PELV power supply unit!

SELV / PELV circuits (safety extra-low voltage / protective extra-low voltage) according to IEC 61010-2-201 must be used to supply this device.

Notes:

- SELV / PELV circuits may give rise to further requirements from standards such as IEC 60204-1 et al, for example with regard to cable spacing and insulation.
- A SELV supply provides safe electrical isolation and limitation of the voltage without a connection to the protective conductor, a PELV supply also requires a safe connection to the protective conductor.

3.7 Disposal



Products marked with a crossed-out wheeled bin shall not be discarded with the normal waste stream. The device is considered as waste electrical and electronic equipment. The national regulations for the disposal of waste electrical and electronic equipment must be observed.

4 Commissioning

NOTICE



Further information

For information on commissioning with TwinCAT and EtherCAT basics, please refer to the “[EtherCAT system manual](#)”.

⚠ CAUTION

Watchdog settings

Changes to the watchdog settings can lead to unwanted system behavior or damage to devices.

- Observe the information in the chapter “Notes on watchdog settings” in the EtherCAT system documentation before making any changes to the watchdog settings!

4.1 1-channel mode

4.1.1 Overview of functions

The ED5112 terminals offer a wide range of functions. The following table provides an overview of the functions provided in 1-channel mode. A detailed description can be found in the individual chapters.

To use the extended functions, the corresponding functions must be selected via the “Predefined PDO Assignment”. The assignment is described in chapter “[Process data](#) [► 57]”.

Basic functions	Description
Selection of encoder type [► 61]	Encoders or counters/pulse generators with signal levels according to RS422, TTL or Open Collector can be selected.
Encoder operating voltage [► 62]	The encoder supply can be set separately for each channel to either 5 V DC, 12 V DC or 24 V DC.
Evaluation of the counter value [► 62]	The input signal can be subject to 4-fold, 2-fold or 1-fold evaluation.
Counter limits [► 62]	The value range within which counting takes place can be defined.
Counter overflow / counter underflow [► 142]	If the count limit is exceeded or underrun, this is indicated in separate process data.
Counting direction [► 65]	The counting direction can be adapted to the application.
Reversion of rotation [► 70]	The counting direction and a reversion of rotation can be detected and output via the process data. This function can also be used for standstill monitoring [► 71].
Reset counter value [► 67]	Allows a recurring reset of the counter value via zero pulse C or an edge (positive/negative) at the “Latch extern” input.
Set counter value [► 68]	The counter value can be set at runtime to a predefined counter value via a PLC variable, zero pulse C or an edge (positive/negative) at the “Latch extern” input.
Save counter value [► 72]	The current counter value can be saved, independent of the cycle time, in separate process data via an edge (positive/negative) at the “Latch extern” and Gate/Latch input or the zero pulse C. You can parameterize whether the function is executed at each external edge or only once after each activation. By using both latch inputs a workpiece measurement [► 75] can also be realized.
Lock counter value [► 76]	The counter value can be locked via an edge (positive/negative) at the Gate input or a PLC variable.

Extended functionalities	Description
Frequency measurement [► 77]	The average frequency of the input signal within a given timeframe can be output directly.
Period value measurement [► 79]	The period value of the last period within the PLC cycle can be output directly.
Velocity, speed calculation [► 80]	The average velocity or speed of the input signal within a specified timeframe can be output directly.
Duty cycle measurement [► 82]	The ratio of pulse duration t_{ON} to period value T in the last PLC cycle can be output directly.
Timestamp [► 85]	A timestamp based on the distributed clocks system (DC) can be output for the last counting pulse, the zero pulse and the "Latch extern" and "Latch extern 2" inputs.
Microincrements [► 83]	Allows additional increments (256 steps) to be interpolated between the counted encoder increments, thus increasing the resolution of the counter value.
Adjustable interference pulse filters [► 87]	To suppress interference, a filter can be set for each of the input signals.
Diagnostic data [► 132]	Error messages are communicated to the EtherCAT Master/TwinCAT via "DiagMessages".

Process data	Description
Operation modes [► 57]	The scope of the process data can be selected via "Predefined PDO Assignment".
Synchronicity mode [► 59]	In addition to the frame-triggered operation mode (SM mode), a mode based on synchronization via the distributed clocks is available.

Description of the inputs	Description
Zero pulse C [► 91]	With incremental encoders, a full revolution is marked by a special marker, the zero pulse C. This can be used for resetting, setting and storing the counter value.
Latch extern [► 93]	A Latch input is provided for 24 V DC signals with a min. pulse duration t_{ON} of $> 1 \mu s$. This can be used for resetting, setting and storing the counter value.
Gate [► 94]	An external gate input is provided for 24 V DC signals with a minimum pulse duration of $t_{ON} > 1 \mu s$. This can be used for locking, resetting, setting and storing the counter value.
Digital input [► 96]	If the encoder has an alarm output, this can be evaluated.

4.1.2 Process data for single-channel mode

4.1.2.1 Sync Manager (SM)

For a detailed description of how to configure the process data, see the “[EtherCAT device configuration](#)” chapter in the EtherCAT System Manual.

● Process data can be read via CoE but cannot be set.

I In the following descriptions, the corresponding CoE index is always included as a reference in addition to the name of the process data.

- Please note that while the input and output process data (0x6xxx/0x7xxx) can be read via the CoE directory, they cannot be set via the CoE directory!

The scope of process data offered can be modified via the “Process Data” tab (see Fig. *Process Data tab SM3, ED5112 (default)* below).

Sync Manager:

SM	Size	Type	Flags
0	256	MbxOut	
1	256	MbxIn	
2	6	Outputs	
3	16	Inputs	

PDO List:

Index	Size	Name	Flags	SM	SU
0x1A00	16.0	ENC Status Channel 1	F	3	0
0x1A01	10.0	ENC Status Compact Channel 1	F		0
0x1A02	12.0	ENC Status Channel 1	F		0
0x1A03	8.0	ENC Status Compact Channel 1	F		0
0x1A04	8.0	ENC Status Counter Channel 1	F		0
0x1A05	6.0	ENC Status Compact Counter Channel 1	F		0
0x1A06	10.0	ENC Status Legacy Channel 1	F		0
0x1A07	6.0	ENC Status Compact Legacy Channel 1	F		0
0x1A08	4.0	ENC Frequency Channel 1	F		0
0x1A09	2.0	ENC Frequency Compact Channel 1	F		0
0x1A0A	4.0	ENC Period Channel 1	F		0
0x1A0B	2.0	ENC Period Compact Channel 1	F		0
0x1A0C	6.0	ENC Duty Cycle Channel 1	F		0
0x1A0D	32.0	ENC Timestamp Channel 1	F		0
0x1A0E	16.0	ENC Timestamp Compact Channel 1	F		0
0x1A11	12.0	ENC Status Channel 2	F		0

PDO Assignment (0x1C13):

- ☒ 0x1A00
- ☐ 0x1A01 (excluded by 0x1A00)
- ☐ 0x1A02 (excluded by 0x1A00)
- ☐ 0x1A03 (excluded by 0x1A00)
- ☐ 0x1A04 (excluded by 0x1A00)
- ☐ 0x1A05 (excluded by 0x1A00)
- ☐ 0x1A06 (excluded by 0x1A00)
- ☐ 0x1A07 (excluded by 0x1A00)
- ☐ 0x1A08
- ☐ 0x1A09
- ☐ 0x1A0A
- ☐ 0x1A0B
- ☐ 0x1A0C
- ☐ 0x1A0D
- ☐ 0x1A0E
- ☐ 0x1A11 (excluded by 0x1A00)
- ☐ 0x1A12 (excluded by 0x1A00)
- ☐ 0x1A13 (excluded by 0x1A00)
- ☐ 0x1A14 (excluded by 0x1A00)
- ☐ 0x1A17 (excluded by 0x1A00)
- ☐ 0x1A18 (excluded by 0x1A00)
- ☐ 0x1A19 (excluded by 0x1A00)
- ☐ 0x1A1A (excluded by 0x1A00)

PDO Content (0x1A00):

Index	Size	Offs	Name	Type	Default (hex)
0x6000:01	0.1	0.0	Status__Latch C valid	BIT	
0x6000:02	0.1	0.1	Status__Latch exten valid	BIT	
0x6000:03	0.1	0.2	Status__Set counter done	BIT	
0x6000:04	0.1	0.3	Status__Counter underflow	BIT	
0x6000:05	0.1	0.4	Status__Counter overflow	BIT	
0x6000:06	0.1	0.5	Status__Status of input status	BIT	
0x6000:07	0.1	0.6	Status__Open circuit	BIT	
0x6000:08	0.1	0.7	Status__Extrapolation stall	BIT	
0x6000:09	0.1	1.0	Status__Status of input A	BIT	
0x6000:0A	0.1	1.1	Status__Status of input B	BIT	
0x6000:0B	0.1	1.2	Status__Status of input C	BIT	
0x6000:0C	0.1	1.3	Status__Status of input gate	BIT	
0x6002:0D	0.1	1.4	Status__Diag	BIT	
0x6002:0E	0.1	1.5	Status__TxPDO State	BIT	
0x6002:0F	0.2	1.6	Status__Input cycle counter	BIT2	
0x6002:11	0.1	2.0	Status__Software gate valid	BIT	
0x6002:12	0.1	2.1	Status__Latch exten 2 valid	BIT	
0x6002:13	0.1	2.2	Status__Direction inversion detec...	BIT	

Download

- ☒ PDO Assignment
- ☐ PDO Configuration

Predefined PDO Assignment: "1.Ch Standard, 1xABC"

Load PDO info from device

Sync Unit Assignment...

Fig. 31: ED5112 - Process data tab SM3 (default)

4.1.2.2 PDO assignment for single-channel mode

A wide range of functions and, consequently, a wide range of process data is available.

4.1.2.2.1 SM3 - Inputs (0x1A00 .. 0x1A0E)

0x1A00 - ENC Status Channel 1 (16.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x6000:01 [153] - Status_Latch C valid (0.1)	0x1A01 [171] - ENC Status Compact Channel 1 (10.0)
0x6000:02 [153] - Status_Latch extern valid (0.1)	0x1A02 [172] - ENC Status Channel 1 (12.0)
0x6000:03 [153] - Status_Set counter done (0.1)	0x1A03 [173] - ENC Status Compact Channel 1 (8.0)
0x6000:04 [153] - Status_Counter underflow (0.1)	0x1A04 [173] - ENC Status Counter Channel 1 (8.0)
0x6000:05 [153] - Status_Counter overflow (0.1)	0x1A05 [174] - ENC Status Compact Counter Channel 1 (6.0)
0x6000:06 [153] - Status_Status of input status (0.1)	0x1A06 [174] - ENC Status Legacy Channel 1 (10.0)
0x6000:07 [153] - Status_Open circuit (0.1)	0x1A07 [175] - ENC Status Compact Legacy Channel 1 (6.0)
0x6000:08 [153] - Status_Extrapolation stall (0.1)	
0x6000:09 [153] - Status_Status of input A (0.1)	0x1A11 [177] - ENC Status Channel 2 (12.0)
0x6000:0A [153] - Status_Status of input B (0.1)	0x1A12 [178] - ENC Status Compact Channel 2 (8.0)
0x6000:0B [153] - Status_Status of input C (0.1)	0x1A13 [178] - ENC Status Counter Channel 2 (8.0)
0x6000:0C [153] - Status_Status of input gate (0.1)	0x1A14 [179] - ENC Status Compact Counter Channel 2 (6.0)
0x6002:0D [154] - Status_Diag (0.1)	0x1A17 [179] - ENC Frequency Channel 2 (4.0)
0x6002:0E [154] - Status_TxPDO State (0.1)	0x1A18 [179] - ENC Frequency Compact Channel 2 (2.0)
0x6002:0F [154] - Status_Input cycle counter (0.2)	0x1A19 [179] - ENC Period Channel 2 (4.0)
0x6002:11 [154] - Status_Software gate valid (0.1)	0x1A1A [179] - ENC Period Compact Channel 2 (2.0)
0x6002:12 [154] - Status_Latch extern 2 valid (0.1)	
0x6002:13 [154] - Status_Direction inversion detected (0.1)	
0x6002:14 [154] - Status_Status of extern Latch (0.1)	
0x6002:15 [154] - Status_Counter value out of range (0.1)	
0x6000:11 [153] - Counter value (4.0)	
0x6000:12 [153] - Latch value (4.0)	
0x6000:22 [153] - Latch value 2 (4.0)	

0x1A01 - ENC Status Compact Channel 1 (10.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x6000:01 [153] - Status_Latch C valid (0.1)	0x1A00 [170] - ENC Status Channel 1 (16.0)
0x6000:02 [153] - Status_Latch extern valid (0.1)	0x1A02 [172] - ENC Status Channel 1 (12.0)
0x6000:03 [153] - Status_Set counter done (0.1)	0x1A03 [173] - ENC Status Compact Channel 1 (8.0)
0x6000:04 [153] - Status_Counter underflow (0.1)	0x1A04 [173] - ENC Status Counter Channel 1 (8.0)
0x6000:05 [153] - Status_Counter overflow (0.1)	0x1A05 [174] - ENC Status Compact Counter Channel 1 (6.0)
0x6000:06 [153] - Status_Status of input status (0.1)	0x1A06 [174] - ENC Status Legacy Channel 1 (10.0)
0x6000:07 [153] - Status_Open circuit (0.1)	0x1A07 [175] - ENC Status Compact Legacy Channel 1 (6.0)
0x6000:08 [153] - Status_Extrapolation stall (0.1)	
0x6000:09 [153] - Status_Status of input A (0.1)	
0x6000:0A [153] - Status_Status of input B (0.1)	
0x6000:0B [153] - Status_Status of input C (0.1)	
0x6000:0C [153] - Status_Status of input gate (0.1)	
0x6002:0D [154] - Status_Diag (0.1)	
0x6002:0E [154] - Status_TxPDO State (0.1)	
0x6002:0F [154] - Status_Input cycle counter (0.2)	
0x6002:11 [154] - Status_Software gate valid (0.1)	
0x6002:12 [154] - Status_Latch extern 2 valid (0.1)	
0x6002:13 [154] - Status_Direction inversion detected (0.1)	
0x6002:14 [154] - Status_Status of extern Latch (0.1)	
0x6002:15 [154] - Status_Counter value out of range (0.1)	
0x6000:11 [153] - Counter value (2.0)	
0x6000:12 [153] - Latch value (2.0)	
0x6000:22 [153] - Latch value 2 (2.0)	

0x1A04 - ENC Status Counter Channel 1 (8.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x6000:03 [153] - Status_Set counter done (0.1)	0x1A00 [170] - ENC Status Channel 1 (16.0)
0x6002:0D [154] - Status_Diag (0.1)	0x1A01 [171] - ENC Status Compact Channel 1 (10.0)
0x6002:0E [154] - Status_TxPDO State (0.1)	0x1A02 [172] - ENC Status Channel 1 (12.0)
0x6002:0F [154] - Status_Input cycle counter (0.2)	0x1A03 [173] - ENC Status Compact Channel 1 (8.0)
0x6002:11 [154] - Status_Software gate valid (0.1)	0x1A05 [174] - ENC Status Compact Counter Channel 1 (6.0)
0x6000:11 [153] - Counter value (4.0)	0x1A06 [174] - ENC Status Legacy Channel 1 (10.0)
	0x1A07 [175] - ENC Status Compact Legacy Channel 1 (6.0)

0x1A05 - ENC Status Compact Counter Channel 1 (6.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x6000:03 [153] - Status_Set counter done (0.1)	0x1A00 [170] - ENC Status Channel 1 (16.0)
0x6002:0D [154] - Status_Diag (0.1)	0x1A01 [171] - ENC Status Compact Channel 1 (10.0)
0x6002:0E [154] - Status_TxPDO State (0.1)	0x1A02 [172] - ENC Status Channel 1 (12.0)
0x6002:0F [154] - Status_Input cycle counter (0.2)	0x1A03 [173] - ENC Status Compact Channel 1 (8.0)
0x6002:11 [154] - Status_Software gate valid (0.1)	0x1A04 [173] - ENC Status Counter Channel 1 (8.0)
0x6000:11 [153] - Counter value (2.0)	0x1A06 [174] - ENC Status Legacy Channel 1 (10.0)
	0x1A07 [175] - ENC Status Compact Legacy Channel 1 (6.0)

0x1A06 - ENC Status Legacy Channel 1 (10.0) [single-channel mode, Legacy EL5101]	
Contents Index - name size (byte.bit)	Excluded PDOs Index name size (byte.bit)
0x6000:01 [153] - Status_Latch C valid (0.1)	0x1A00 [170] - ENC Status Channel 1 (16.0)
0x6000:02 [153] - Status_Latch extern valid (0.1)	0x1A01 [171] - ENC Status Compact Channel 1 (10.0)
0x6000:03 [153] - Status_Set counter done (0.1)	0x1A02 [172] - ENC Status Channel 1 (12.0)
0x6000:04 [153] - Status_Counter underflow (0.1)	0x1A03 [173] - ENC Status Compact Channel 1 (8.0)
0x6000:05 [153] - Status_Counter overflow (0.1)	0x1A04 [173] - ENC Status Counter Channel 1 (8.0)
0x6000:06 [153] - Status_Status of input status (0.1)	0x1A05 [174] - ENC Status Compact Counter Channel 1 (6.0)
0x6000:07 [153] - Status_Open circuit (0.1)	0x1A07 [175] - ENC Status Compact Legacy Channel 1 (6.0)
0x6000:08 [153] - Status_Extrapolation stall (0.1)	
0x6000:09 [153] - Status_Status of input A (0.1)	
0x6000:0A [153] - Status_Status of input B (0.1)	
0x6000:0B [153] - Status_Status of input C (0.1)	
0x6000:0C [153] - Status_Status of input gate (0.1)	
0x6000:0D [153] - Status_Status of extern latch (0.1)	
0x6000:0E [153] - Status_Sync error (0.1)	
0x6000:0F [153] - Status_TxPDO State (0.1)	
0x6000:10 [153] - Status_TxPDO Toggle (0.1)	
0x6000:11 [153] - Counter value (4.0)	
0x6000:12 [153] - Latch value (4.0)	

0x1A07 - ENC Status Compact Legacy Channel 1 (6.0) [single-channel mode, Legacy EL5101]			
Contents		Excluded PDOs	
Index	name size (byte.bit)	Index	name size (byte.bit)
0x6000:01	153] - Status_Latch C valid (0.1)	0x1A00	170] - ENC Status Channel 1 (16.0)
0x6000:02	153] - Status_Latch extern valid (0.1)	0x1A01	171] - ENC Status Compact Channel 1 (10.0)
0x6000:03	153] - Status_Set counter done (0.1)	0x1A02	172] - ENC Status Channel 1 (12.0)
0x6000:04	153] - Status_Counter underflow (0.1)	0x1A03	173] - ENC Status Compact Channel 1 (8.0)
0x6000:05	153] - Status_Counter overflow (0.1)	0x1A04	173] - ENC Status Counter Channel 1 (8.0)
0x6000:06	153] - Status_Status of input status (0.1)	0x1A05	174] - ENC Status Compact Counter Channel 1 (6.0)
0x6000:07	153] - Status_Open circuit (0.1)	0x1A06	174] - ENC Status Legacy Channel 1 (10.0)
0x6000:08	153] - Status_Extrapolation stall (0.1)		
0x6000:09	153] - Status_Status of input A (0.1)		
0x6000:0A	153] - Status_Status of input B (0.1)		
0x6000:0B	153] - Status_Status of input C (0.1)		
0x6000:0C	153] - Status_Status of input gate (0.1)		
0x6000:0D	153] - Status_Status of extern latch (0.1)		
0x6000:0E	153] - Status_Sync error (0.1)		
0x6000:0F	153] - Status_TxPDO State (0.1)		
0x6000:10	153] - Status_TxPDO Toggle (0.1)		
0x6000:11	153] - Counter value (2.0)		
0x6000:12	153] - Latch value (2.0)		

0x1A08 - ENC Frequency Channel 1 (4.0)			
Contents		Excluded PDOs	
Index	name size (byte.bit)	Index	name size (byte.bit)
0x6000:13	153] - Frequency value (4.0)	0x1A09	175] - ENC Frequency Compact Channel 1 (2.0)

0x1A09 - ENC Frequency Compact Channel 1 (2.0)			
Contents		Excluded PDOs	
Index	name size (byte.bit)	Index	name size (byte.bit)
0x6000:13	153] - Frequency value (2.0)	0x1A08	175] - ENC Frequency Channel 1 (4.0)

0x1A0A - ENC Period Channel 1 (4.0)			
Contents		Excluded PDOs	
Index	name size (byte.bit)	Index	name size (byte.bit)
0x6000:14	153] - Period value (4.0)	0x1A0B	176] - ENC Period Compact Channel 1 (2.0)

0x1A0B - ENC Period Compact Channel 1 (2.0)			
Contents		Excluded PDOs	
Index	name size (byte.bit)	Index	name size (byte.bit)
0x6000:14	153] - Period value (2.0)	0x1A0A	175] - ENC Period Channel 1 (4.0)

0x1A0C - ENC Duty Cycle Channel 1 (6.0)			
Contents		Excluded PDOs	
Index	name size (byte.bit)	Index	name size (byte.bit)
0x6000:23	153] - Duty cycle (2.0)	-	
0x6000:24	153] - Duty cycle min (2.0)		
0x6000:25	153] - Duty cycle max (2.0)		

0x1A0D - ENC Timestamp Channel 1 (32.0)			
Contents		Excluded PDOs	
Index	name size (byte.bit)	Index	name size (byte.bit)
0x6000:16	153] - Timestamp (8.0)	0x1A0E	176] - ENC Timestamp Compact Channel 1 (16)
0x6000:1F	153] - Timestamp C (8.0)		
0x6000:20	153] - Timestamp latch (8.0)		
0x6000:21	153] - Timestamp latch 2 (8.0)		

0x1A0E - ENC Timestamp Compact Channel 1 (16.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x6000:16 [P 153] - Timestamp (4.0) 0x6000:1F [P 153] - Timestamp C (4.0) 0x6000:20 [P 153] - Timestamp latch (4.0) 0x6000:21 [P 153] - Timestamp latch 2 (4.0)	0x1A0D [P 176] - ENC Timestamp Channel 1 (32.0)

4.1.2.2.2 SM2 - Outputs (0x1600 .. 0x1607)

0x1600 - ENC Control Channel 1 (6.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7000:01 [P 155] - Control_Enable latch C (0.1) 0x7000:02 [P 155] - Control_Enable latch extern on positive edge (0.1) 0x7000:03 [P 155] - Control_Set counter (0.1) 0x7000:04 [P 155] - Control_Enable latch extern on negative edge (0.1) 0x7000:08 [P 155] - Control_Set counter on latch C (0.1) 0x7000:09 [P 155] - Control_Set software gate (0.1) 0x7000:0A [P 155] - Control_Set counter on latch extern on positive edge (0.1) 0x7000:0B [P 155] - Control_Set counter on latch extern on negative edge (0.1) 0x7000:0C [P 155] - Control_Enable latch extern 2 on positive edge (0.1) 0x7000:0D [P 155] - Control_Enable latch extern 2 on negative edge (0.1) 0x7000:11 [P 155] - Set counter value (4.0)	0x1601 [P 161] - ENC Control Compact Channel 1 (4.0) 0x1602 [P 162] - ENC Control Channel 1 (6.0) 0x1603 [P 162] - ENC Control Compact Channel 1 (4.0) 0x1604 [P 162] - ENC Control Counter Channel 1 (6.0) 0x1605 [P 163] - ENC Control Compact Counter Channel 1 (4.0) 0x1606 [P 163] - ENC Control Legacy Channel 1 (6.0) 0x1607 [P 163] - ENC Control Compact Legacy Channel 1 (4.0)

0x1601 - ENC Control Compact Channel 1 (4.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7000:01 [P 155] - Control_Enable latch C (0.1) 0x7000:02 [P 155] - Control_Enable latch extern on positive edge (0.1) 0x7000:03 [P 155] - Control_Set counter (0.1) 0x7000:04 [P 155] - Control_Enable latch extern on negative edge (0.1) 0x7000:08 [P 155] - Control_Set counter on latch C (0.1) 0x7000:09 [P 155] - Control_Set software gate (0.1) 0x7000:0A [P 155] - Control_Set counter on latch extern on positive edge (0.1) 0x7000:0B [P 155] - Control_Set counter on latch extern on negative edge (0.1) 0x7000:0C [P 155] - Control_Enable latch extern 2 on positive edge (0.1) 0x7000:0D [P 155] - Control_Enable latch extern 2 on negative edge (0.1) 0x7000:11 [P 155] - Set counter value (2.0)	0x1600 [P 161] - ENC Control Channel 1 (6.0) 0x1602 [P 162] - ENC Control Channel 1 (6.0) 0x1603 [P 162] - ENC Control Compact Channel 1 (4.0) 0x1604 [P 162] - ENC Control Counter Channel 1 (6.0) 0x1605 [P 163] - ENC Control Compact Counter Channel 1 (4.0) 0x1606 [P 163] - ENC Control Legacy Channel 1 (6.0) 0x1607 [P 163] - ENC Control Compact Legacy Channel 1 (4.0)

0x1602 - ENC Control Channel 1 (6.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7000:02 [P 155] - Control_Enable latch extern on positive edge (0.1) 0x7000:03 [P 155] - Control_Set counter (0.1) 0x7000:04 [P 155] - Control_Enable latch extern on negative edge (0.1) 0x7000:09 [P 155] - Control_Set software gate (0.1) 0x7000:0A [P 155] - Control_Set counter on latch extern on positive edge (0.1) 0x7000:0B [P 155] - Control_Set counter on latch extern on negative edge (0.1) 0x7000:11 [P 155] - Set counter value (4.0)	0x1600 [P 161] - ENC Control Channel 1 (6.0) 0x1601 [P 161] - ENC Control Compact Channel 1 (4.0) 0x1603 [P 162] - ENC Control Compact Channel 1 (4.0) 0x1604 [P 162] - ENC Control Counter Channel 1 (6.0) 0x1605 [P 163] - ENC Control Compact Counter Channel 1 (4.0) 0x1606 [P 163] - ENC Control Legacy Channel 1 (6.0) 0x1607 [P 163] - ENC Control Compact Legacy Channel 1 (4.0)

0x1603 - ENC Control Compact Channel 1 (4.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7000:02 [P 155] - Control_Enable latch extern on positive edge (0.1)	0x1600 [P 161] - ENC Control Channel 1 (6.0)
0x7000:03 [P 155] - Control_Set counter (0.1)	0x1601 [P 161] - ENC Control Compact Channel 1 (4.0)
0x7000:04 [P 155] - Control_Enable latch extern on negative edge (0.1)	0x1602 [P 162] - ENC Control Channel 1 (6.0)
0x7000:09 [P 155] - Control_Set software gate (0.1)	0x1604 [P 162] - ENC Control Counter Channel 1 (6.0)
0x7000:0A [P 155] - Control_Set counter on latch extern on positive edge (0.1)	0x1605 [P 163] - ENC Control Compact Counter Channel 1 (4.0)
0x7000:0B [P 155] - Control_Set counter on latch extern on negative edge (0.1)	0x1606 [P 163] - ENC Control Legacy Channel 1 (6.0)
0x7000:11 [P 155] - Set counter value (2.0)	0x1607 [P 163] - ENC Control Compact Legacy Channel 1 (4.0)

0x1604 - ENC Control Counter Channel 1 (6.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7000:03 [P 155] - Control_Set counter (0.1)	0x1600 [P 161] - ENC Control Channel 1 (6.0)
0x7000:09 [P 155] - Control_Set software gate (0.1)	0x1601 [P 161] - ENC Control Compact Channel 1 (4.0)
0x7000:11 [P 155] - Set counter value (4.0)	0x1602 [P 162] - ENC Control Channel 1 (6.0)
	0x1603 [P 162] - ENC Control Compact Channel 1 (4.0)
	0x1605 [P 163] - ENC Control Compact Counter Channel 1 (4.0)
	0x1606 [P 163] - ENC Control Legacy Channel 1 (6.0)
	0x1607 [P 163] - ENC Control Compact Legacy Channel 1 (4.0)

0x1605 - ENC Control Compact Counter Channel 1 (4.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7000:03 [P 155] - Control_Set counter (0.1)	0x1600 [P 161] - ENC Control Channel 1 (6.0)
0x7000:09 [P 155] - Control_Set software gate (0.1)	0x1601 [P 161] - ENC Control Compact Channel 1 (4.0)
0x7000:11 [P 155] - Set counter value (2.0)	0x1602 [P 162] - ENC Control Channel 1 (6.0)
	0x1603 [P 162] - ENC Control Compact Channel 1 (4.0)
	0x1604 [P 162] - ENC Control Counter Channel 1 (6.0)
	0x1606 [P 163] - ENC Control Legacy Channel 1 (6.0)
	0x1607 [P 163] - ENC Control Compact Legacy Channel 1 (4.0)

0x1606 - ENC Control Legacy Channel 1 (6.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7000:01 [P 155] - Control_Enable latch C (0.1)	0x1600 [P 161] - ENC Control Channel 1 (6.0)
0x7000:02 [P 155] - Control_Enable latch extern on positive edge (0.1)	0x1601 [P 161] - ENC Control Compact Channel 1 (4.0)
0x7000:03 [P 155] - Control_Set counter (0.1)	0x1602 [P 162] - ENC Control Channel 1 (6.0)
0x7000:04 [P 155] - Control_Enable latch extern on negative edge (0.1)	0x1603 [P 162] - ENC Control Compact Channel 1 (4.0)
0x7000:11 [P 155] - Set counter value (4.0)	0x1604 [P 162] - ENC Control Counter Channel 1 (6.0)
	0x1605 [P 163] - ENC Control Compact Counter Channel 1 (4.0)
	0x1607 [P 163] - ENC Control Compact Legacy Channel 1 (4.0)

0x1607 - ENC Control Compact Legacy Channel 1 (4.0)	
Contents	Excluded PDOs
Index - name size (byte.bit)	Index - name size (byte.bit)
0x7000:01 [▶ 155] - Control_Enable latch C (0.1)	0x1600 [▶ 161] - ENC Control Channel 1 (6.0)
0x7000:02 [▶ 155] - Control_Enable latch extern on positive edge (0.1)	0x1601 [▶ 161] - ENC Control Compact Channel 1 (4.0)
0x7000:03 [▶ 155] - Control_Set counter (0.1)	0x1602 [▶ 162] - ENC Control Channel 1 (6.0)
0x7000:04 [▶ 155] - Control_Enable latch extern on negative edge (0.1)	0x1603 [▶ 162] - ENC Control Compact Channel 1 (4.0)
0x7000:11 [▶ 155] - Set counter value (2.0)	0x1604 [▶ 162] - ENC Control Counter Channel 1 (6.0)
	0x1605 [▶ 163] - ENC Control Compact Counter Channel 1 (4.0)
	0x1606 [▶ 163] - ENC Control Legacy Channel 1 (6.0)

4.1.2.3 Predefined PDO Assignment for single-channel mode

The “Predefined PDO Assignment” enables a simplified selection of the process data. The desired function is selected on the lower part of the Process data tab. As a result, all necessary PDOs are automatically enabled and the unnecessary PDOs are disabled.

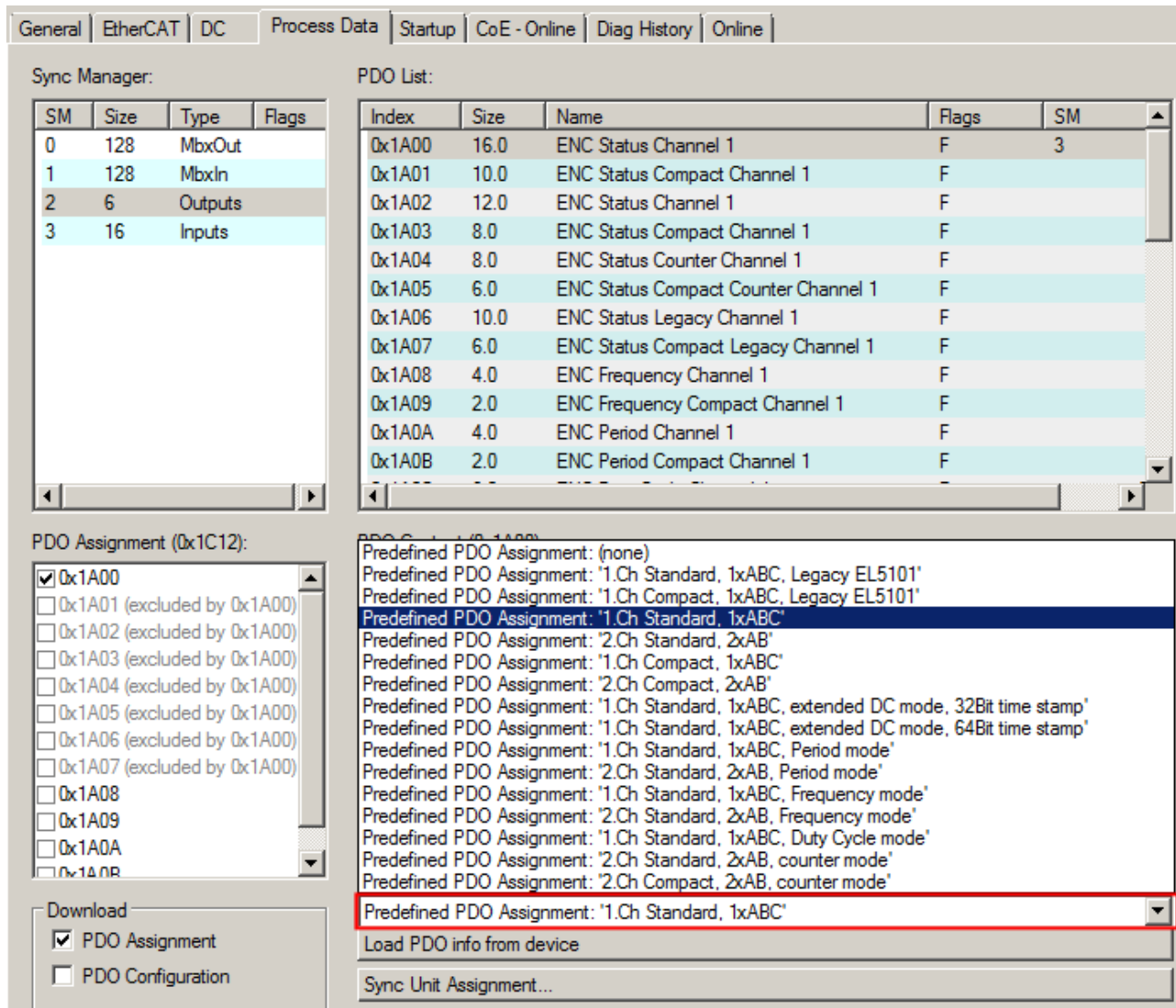


Fig. 32: Process data, Predefined PDO (default: 1.Ch Standard, 1xABC)

15 Predefined PDO assignments are available for 1-channel and 2-channel mode [► 105] in the modes “Standard”, “Compact”, “Counter” and “Legacy” (1-channel mode only).

● Note on using the timestamp function

I In order to be able to use the timestamp function, the terminal must be operated in “DC-Synchron” or “DC-Synchron (input based)” mode.

In 1-channel mode the following predefined PDOs are available:

Predefined PDO Assignments for Legacy mode (single-channel mode)

Predefined PDO Assignment	PDO Assignment
1.Ch Standard, 1xABC, Legacy EL5101	SM3: 0x1A06 [► 52] - ENC Status Legacy Channel 1 (10.0) SM2: 0x1606 [► 55] - ENC Control Legacy Channel 1 (6.0)
1.Ch Compact, 1x ABC, Legacy EL5101	SM3: 0x1A07 [► 53] - ENC Status Compact Legacy Channel 1 (6.0) SM2: 0x1607 [► 56] - ENC Control Compact Legacy Channel 1 (4.0)

Predefined PDO Assignments for Compact mode (single-channel mode)

Predefined PDO Assignment	PDO Assignment
1.Ch Compact, 1xABC	SM3: 0x1A01 [► 51] - ENC Status Compact Channel 1 (10.0) SM2: 0x1601 [► 54] - ENC Control Compact Channel 1 (4.0)

Predefined PDO Assignments for Standard mode (single-channel mode)

Predefined PDO Assignment	PDO Assignment
1.Ch Standard, 1xABC	SM3: 0x1A00 [► 170] - ENC Status Channel 1 (16.0) SM2: 0x1600 [► 161] - ENC Control Channel 1 (6.0)
1.Ch Standard, 1xABC, extended DC mode, 32Bit time stamp	SM3: 0x1A00 [► 170] - ENC Status Channel 1 (16.0) 0x1A08 [► 175] - ENC Frequency Channel 1 (4.0) 0x1A0A [► 175] - ENC Period Channel 1 (4.0) 0x1A0C [► 176] - ENC Duty Cycle Channel 1 (6.0) 0x1A0E [► 176] - ENC Timestamp Compact Channel 1 (16.0) SM2: 0x1600 [► 161] - ENC Control Channel 1 (6.0)
1.Ch Standard, 1xABC, extended DC mode, 64Bit time stamp	SM3: 0x1A00 [► 170] - ENC Status Channel 1 (16.0) 0x1A08 [► 175] - ENC Frequency Channel 1 (4.0) 0x1A0A [► 175] - ENC Period Channel 1 (4.0) 0x1A0C [► 176] - ENC Duty Cycle Channel 1 (6.0) 0x1A0D [► 176] - ENC Compact Channel 1 (32.0) SM2: 0x1600 [► 161] - ENC Control Channel 1 (6.0)
1.Ch Standard, 1xABC, Period mode	SM3: 0x1A00 [► 170] - ENC Status Channel 1 (16.0) 0x1A0A [► 175] - ENC Period Channel 1 (4.0) SM2: 0x1600 [► 161] - ENC Control Channel 1 (6.0)
1.Ch Standard, 1xABC, Frequency mode	SM3: 0x1A00 [► 170] - ENC Status Channel 1 (16.0) 0x1A08 [► 175] - ENC Frequency Channel 1 (4.0) SM2: 0x1600 [► 161] - ENC Control Channel 1 (6.0)
1.Ch Standard, Duty cycle mode,	SM3: 0x1A00 [► 170] - ENC Status Channel 1 (16.0) 0x1A08 [► 175] - ENC Frequency Channel 1 (4.0) SM2: 0x1600 [► 161] - ENC Control Channel 1 (6.0)

4.1.2.4 Synchronicity mode

The terminal can be operated in three different operation modes. Depending on the operation mode, the process data are synchronized by the terminal at different times and made available to the EtherCAT frame.

The following operation modes are available for selection in the “DC” tab:

Operation mode	Description
FreeRun/SM Synchron	Cyclic, frame-triggered exchange of process data. An Ethernet frame triggers the process data provision for the next retrieving frame.
DC-Synchron	Cyclically constant determination of the counter value by the integrated distributed clocks unit. The configuration corresponds to an output module. The local SYNC event is triggered shortly after the passage of the EtherCAT frame. This means that the output data just delivered is output immediately.
DC-Synchron (input based)	Cyclically constant determination of the counter value by the integrated distributed clocks unit. The configuration corresponds to an input module. The local SYNC event is triggered before the EtherCAT frame. This makes current input data available for onward transport.

NOTICE



Further information

For more information, see the chapter “[I/O Synchronization via Distributed Clocks](#)” in the EtherCAT system manual.

4.1.2.5 EtherCAT cycle time

The EtherCAT cycle time depends on the selection of the process data to be transferred. The following table provides an overview of the recommended cycle time, depending on the “Predefined PDO Assignment”. The specifications refer to a multiple of the “Base Time” to be set via the TwinCAT Master. If a faster cycle time is used, the process data “Input cycle counter” (0x6002:0F) must be used to monitor when new process data are delivered.

ED5112 - Predefined PDO assignment in 1-channel mode	EtherCAT cycle time	
	Min.	Max.
1. Ch. Standard, 1xABC Legacy EL5101	typ. 76.9 µs	typ. 125 µs
1. Ch. Compact, 1xABC Legacy EL5101	typ. 71.4 µs	typ. 125 µs
1. Ch. Standard, 1xABC	typ. 76.9 µs	typ. 125 µs
1. Ch. Compact, 1xABC	typ. 76.9 µs	typ. 125 µs
1. Ch. Standard, 1xABC, extended DC mode, 32Bit time stamp	typ. 125 µs	typ. 150 µs
1. Ch. Standard, 1xABC, extended DC mode, 64Bit time stamp	typ. 125 µs	typ. 150 µs
1. Ch. Standard, 1xABC, Period mode	typ. 83.3 µs	typ. 125 µs
1. Ch. Standard, 1xABC, Frequency mode	typ. 76.9 µs	typ. 125 µs
1. Ch. Standard, 1xABC, Duty Cycle mode	typ. 100 µs	typ. 125 µs

4.1.2.6 “Legacy EL5101” mode

The process image of the terminal is based on the MDP511 profile. This profile has been extended for improved functionality in terms of status bits. The terminal provides various status information in the respective “Predefined PDO Assignments”. A process image compatible with the EL5101 is provided via “Legacy EL5101” mode. The process image of the terminal outside “Legacy EL5101” mode differs by the following status bits in the PDO assignment:

EL5101		ED5112			
“Standard / Line Motion” mode		“Legacy EL5101” mode (Ch.1 n = 0, Ch.2 n = 1)		“n.Ch. Standard / Compact / counter” mode (Ch.1 n = 0, Ch.2 n = 1)	
0x6010:0D	Status_Status of extern latch	0x60n0:0D	Status_Status of extern latch	0x60n2:0D	Status_Diag
0x6010:0E	Status_Sync error	0x60n0:0E	Status_Sync error	0x60n2:0E	Status_TxPDO State
0x6010:0F	Status_Status TxPDO State	0x60n0:0F	Status_Status TxPDO State	0x60n2:0F	Status_Status Input cycle counter
0x6010:10	Status_Status TxPDO Toggle	0x60n0:10	Status_Status TxPDO Toggle	0x60n2:10	-
-	-	-	-	0x60n2:14	Status_Status of extern latch

“Legacy EL5101” mode enables the use of existing function blocks based on the modified status bits.

i ED5112 in conjunction with older TwinCAT versions

From TwinCAT version 3.1 Build 4024 and higher, all predefined PDOs of the ED5112 can be automatically linked to the NC. For older TwinCAT versions the “Legacy EL5101” mode must be used. Note the associated functionality restrictions.

i Functional compatibility with EL5101

ED5112 is not functionally compatible with the EL5101. Internal calculation methods and timings may differ. Compatibility with existing projects must be checked on a case-by-case basis.

Limitations of “Legacy EL5101” mode

The following table provides an overview of the functions available in “Legacy EL5101” mode:

Function		“Legacy” mode
Set counter value via	PLC variable	Yes
	zero pulse C	No
	Latch input	No
Reset counter value via	zero pulse C	Yes
	Latch input	Yes
Save counter value via	zero pulse C	Yes
	Latch input	Yes
	Gate input/Latch extern 2	No
Lock counter value via	PLC variable	No
	Gate input/Latch extern 2	Yes
Detect counting direction		No
Detect reversion of rotation		No
Frequency calculation		No
Period duration calculation		No
Duty cycle evaluation		No
Micro-increments		No
Timestamp function		No
Filter function		Yes
Plausibility check		Yes

4.1.3 Basic functions in single-channel mode 1xABC

4.1.3.1 Counter value

The counter value is displayed in the input process data “Counter value” (0x60n0:11). It indicates the current counter value in the terminal. You can adapt it to the application using the following settings.

- [Selection of encoder type \[► 61\]](#) (Index 0x80n1:1D “Counter mode”)
- [Evaluation of the counter value \[► 62\]](#) (Index 0x80n0:06 “Evaluation mode”)
- [Determination of the counter limits \[► 62\]](#) (Index 0x80n1:1B “Reset counter value”/
Index 0x80n1:1A “Limit counter value”)
- [Reversion of rotation \[► 65\]](#) (Index 0x80n0:0E “Reversion of rotation”)

4.1.3.1.1 Selection of encoder type (Counter mode)

To ensure a correct acquisition of the counter value, you must first select the appropriate encoder type.

The connected encoder is selected via index 0x80n1:1D “Counter mode”. Explanations of the supported encoder and signal types can be found in chapter “Supported encoder/signal types [► 14]”.

Choice of the encoder via the index 0x80n1:1D “Counter mode” (n = 0 for Ch.1, n = 1 for Ch.2, depending on the number of channels)	
Value	Meaning
0: Encoder RS422 (diff. input)	RS422 encoder with or without zero pulse
1: Counter RS422 (diff. input)	RS422 counter/pulse generator, with or without zero pulse. Direction preset via track B
2: Encoder TTL (single ended)	TTL encoder with or without zero pulse
3: Counter TTL (single ended)	TTL counter/pulse generator with or without zero pulse. Direction preset via track B
4: Encoder open collector	Open collector encoder with or without zero pulse
5: Counter open collector	Open collector counter/pulse generator with or without zero pulse. Direction preset via track B

In the following sections, the settings under subindices 0, 2 and 4 are generally referred to as “encoder” and the settings under subindices 1, 3 and 5 as “counter/pulse generator”.

● Enabling error detection for the C track

i By default, error detection on the C track is disabled; the index 0x80n0:0D “Error detection C” is set to FALSE by default.

If an encoder or counter/pulse generator with zero pulse C is used, index 0x80n0:0D “Error detection C” can be set to TRUE at the module. The corresponding LED will then also indicate the error.

4.1.3.1.2 Encoder operating voltage (supply voltage)

The encoder supply is generated internally from the 24 V of the power contacts. The encoder supply can be set in index [0x8001:17 \[► 151\]](#) "Supply voltage". An operating voltage of 5 V DC is preset. Voltage values of 5 V DC, 12 V DC, and 24 V DC can be selected. The setting applies to both channels. Before switching to higher voltages, ensure that both encoders support the voltage range.

The following tolerances apply:

Voltage range	Tolerance
5 V DC	+/-5% (4.75 V...5.25 V)
12 V DC	+/-10% (10.8 V...13.2 V)
24 V DC	-15% to +20% (20.4 V...28.8 V)



Setting the encoder supply via index [0x8001:17 \[► 151\]](#)

The encoder supply is set centrally for both channels via the index [0x8001:17 \[► 151\]](#) (channel 1). The corresponding index [0x8011:17](#) of the second channel has no parameterization function.

NOTICE

Setting the encoder supply voltage

- Before switching to a higher voltage, make sure that the connected encoders support the selected voltage range!
- To write to [0x80n1:17](#) "Supply voltage" you have to set the value [0x72657375](#) (ASCII: "user") in index [0xF008 \[► 182\]](#) "Code word".

4.1.3.1.3 Evaluation of the counter value

Evaluation of the "Counter value" is set through index [0x80n0:06](#) "Evaluation mode".

- Evaluation of the input signals (index [0x80n0:06](#) "Evaluation mode"): The input signal can be subject to 4-fold, 2-fold or 1-fold evaluation.
 - 1-fold evaluation: the rising edges at track A are counted.
 - 2-fold evaluation: the rising and falling edges at track A are counted.
 - 4-fold evaluation: the rising and falling edges at tracks A and B are counted.

In the delivery state 4-fold evaluation is selected, as this enables the highest resolution of the input signal.

4.1.3.1.4 Determining the counter limits (Reset counter value / Limit counter value)

Counter limits in delivery state

In delivery state the counter value "Counter Value" counts in the range from 0 to the maximum counter depth. When the maximum counter depth is exceeded "Counter overflow" the counter starts counting up from zero again. When the counter limit is exceeded, this is indicated by the "Counter overflow" bits (see chapter ["Determining the counter limits \("Reset counter value"/"Limit counter value" \[► 64\]\)"](#)).

- PDO Assignment "Standard": 0 to $2^{32}-1$
- PDO Assignment "Compact": 0 to $2^{16}-1$

When a counter underflow occurs, the count continues at the maximum counter depth even if e.g. "Enable extern reset" is enabled in index [0x80n0:02](#). The underflow is identified with the corresponding "Counter underflow" bit.

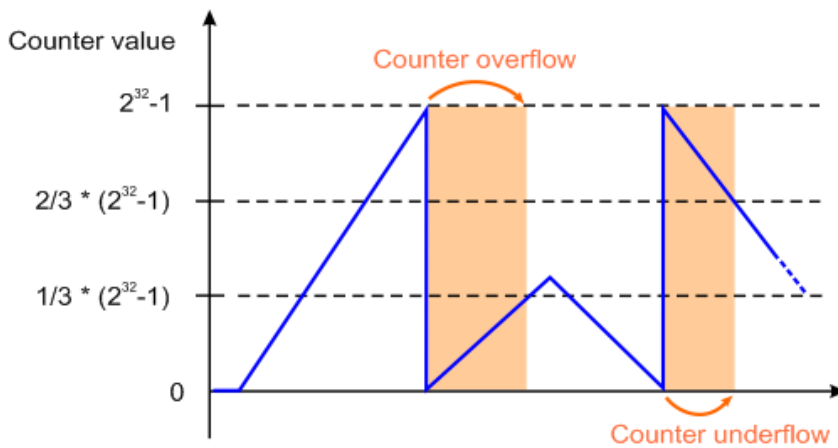


Fig. 33: Counter overflow and underflow in delivery state

Counter limits with defined value range

If counting is only to take place in a defined value range, the counter limits can be adjusted.

● Set counter limits

i For writing to index 0x80n1:1B “Reset counter value” and index 0x80n1:1A “Limit counter value”, the value 0x72657375 (ASCII: “user”) must be set in 0xF008 [► 182] “Code word”.

- Specify the lower counter limit in index 0x80n1:1B “Reset counter value”.
- Specify the upper counter limit in index 0x80n1:1A “Limit counter value”.

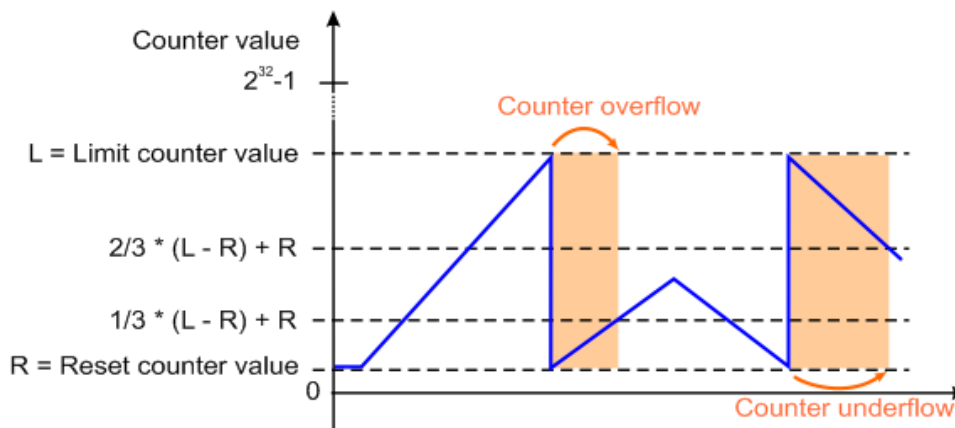


Fig. 34: Counter overflow and underflow with defined value range

● Counter limits

- i**
- The lower counter limit index 0x80n1:1B “Reset counter value” must always be less than the upper counter limit 0x80n1:1A “Limit counter value”. If this is not the case, the last value entered is not accepted.
 - If the lower counter limit in index 0x80n1:1B “Reset counter value” is greater than 0, the Motion Control application (NC/CNC) can only be used in a limited range.

If the counter is parameterized to a counter value outside the counter limits during runtime, this counter value is applied. Exceeding the counter limit is indicated by the process data “Counter value out of range” (index 0x60n2:15).

Example:

The process data “Set counter value” (0x70n0:11) contains a value that exceeds the counter limits, and the bit in the process data “Set counter” (0x70n0:03) is activated.

- The value specified in the process data “Set counter value” (0x70n0:11) is used.

- The bit in the process data “Counter value out of range” (0x60n2:15) is set.

If the counter limits are parameterized in such a way that the current counter value is outside these limits, the underflow/overflow of the counter limit is also shown via the process data “Counter value out of range” (0x60n2:15).

Counter overflow and Counter underflow

An overflow or underflow of the counter limits is indicated by the process data “Counter underflow” (0x60n0:04) or “Counter overflow” (0x60n0:05).

- The bit in the process data “Counter underflow” (0x60n0:04) is set when an underflow occurs 0x80n1:1B “Reset counter value” → 0x80n1:1A “Limit counter value”.
 - With the preset parameters this corresponds to “..00 → ..FF”
It is reset if 2/3 of the counting range are underrun.
 - For counting limits with fixed values, this corresponds to:
 $\frac{2}{3} * (\text{“Limit counter value”} - \text{“Reset counter value”}) + \text{“Reset counter value”}$
- The bit in the process data “Counter overflow” (0x60n0:05) is set when an overflow occurs 0x80n1:1A “Limit counter value” → 0x80n1:1B “Reset counter value”.
 - With default parameters “..FF → ..00”
It is reset if 1/3 of the counter range is exceeded.
 - For counting limits with fixed values, this corresponds to:
 $\frac{1}{3} * (\text{“Limit counter value”} - \text{“Reset counter value”}) + \text{“Reset counter value”}$

Example 1:

0x80n1:1A “Limit counter value” = $2^{12} - 1 = 4095$

0x80n1:1B “Reset counter value” = 0

The “Counter underflow” bit is reset when: $\frac{2}{3} \times 4095 = 2730$ is reached.

The “Counter overflow” bit is reset when: $\frac{1}{3} \times 4095 = 1365$ is reached.

Example 2:

0x80n1:1A “Limit counter value” = $2^{12} - 1 = 4095$

0x80n1:1B “Reset counter value” = 400

The “Counter underflow” bit is reset when: $\frac{2}{3} \times (4095 - 400) + 400 = 2463$ is reached.

The “Counter overflow” bit is reset when: $\frac{1}{3} \times (4095 - 400) + 400 = 1632$ is reached.

4.1.3.1.5 Reversion of rotation

- **With an encoder**, the counting direction is determined by the phase position of the signals on tracks A and B.
 - Forward (cw): Signal on track A leads track B by 90°
 - Reverse (ccw): Signal on track A lags track B by 90°

To adapt the counting direction to the application, this logic can be inverted by setting the bit in index 0x80n0:0E "Reversion of rotation".

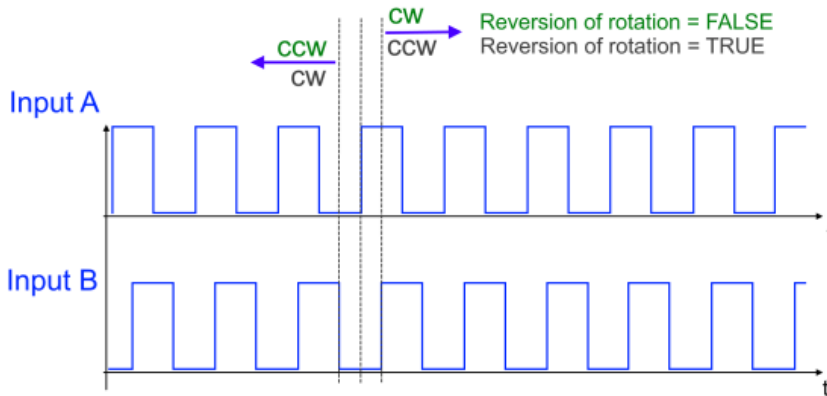


Fig. 35: Reversion of counting direction (Index 0x80n0:0E "Reversion of rotation") for an encoder

- **With a counter/pulse generator** the counting direction is determined by the level at track B.
 - Forward (cw): LOW level at track B or input open
 - Reverse (ccw): HIGH level at track B

Setting the bit in index 0x80n0:0E "Reversion of rotation" also inverts the logic of the counting direction. An overview of the resulting counting direction is shown in the following table.

The current level at input B is displayed via process data "Status of input B" (0x60n0:0A).

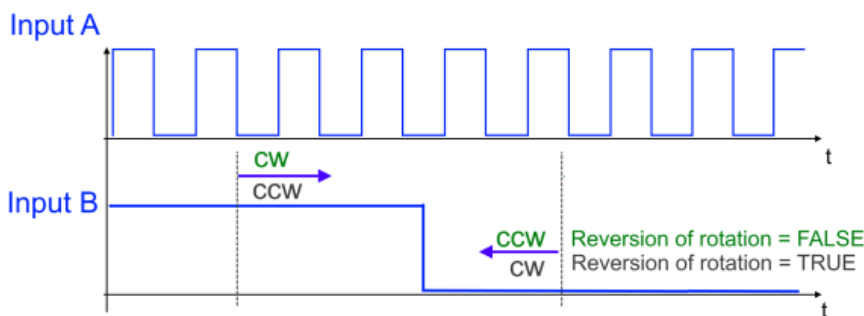


Fig. 36: Reversion of counting direction (Index 0x80n0:0E "Reversion of rotation") for a counter/pulse generator

0x80n1:1D "Counter mode"	Level at input track B	0x80n0:0E "Reversion of rotation"	Resulting counting direction
1: Counter RS422 (diff. input)	Input open / LOW level	FALSE	positive
		TRUE	negative
	RS422 signal level	FALSE	negative
		TRUE	positive
3: Counter TTL (single ended)	Input open / LOW level, voltage level < 0.8 V	FALSE	positive
		TRUE	negative
	TTL voltage level 2.0 V to 6.0 V, with min. 2.1 mA current	FALSE	negative
		TRUE	positive
5: Counter open collector	Input open / LOW level, voltage level < 0.8 V	FALSE	positive
		TRUE	negative
	Open collector voltage level 2.0 V to 6.0 V, with min. 2.1 mA current	FALSE	negative
		TRUE	positive

● **Status LED input B as counter RS422 (diff. input)**

i If the input of track B is open in counter mode "RS422 (diff. input)", a broken wire is detected and the status LED of input B lights up red. The error detection and indication via the LED can be deactivated via index 0x80n0:0C "Error detection B".

4.1.3.2 Counter value reset

A recurring reset of the counter value in the process data "Counter value" (0x60n0:11 [▶ 152]) to "0" can be done in the following ways:

- Input zero pulse C: [▶ 67] a positive edge at the zero pulse C input ("Enable C reset")
- Latch input: [▶ 67] an edge (positive/negative) at the "Latch extern" input ("Enable extern reset")

The settings are made in the configuration data, so it is not necessary to reactivate the device after a reset.

It is not possible to activate the "Enable C reset" (Index 0x80n0:01 [▶ 150]) and "Enable extern reset" (Index 0x80n0:02) functions at the same time.

Counter value reset via the zero pulse C input (Enable C reset)

The counter value can be set to the value specified in index 0x80n1:1B [▶ 151] "Reset counter value" for every full revolution of the encoder via the zero pulse C.

- Presetting of the reset value via index 0x80n1:1B [▶ 151] "Reset counter value" (Default: 0)
- To activate this function set the bit in index 0x80n0:01 [▶ 150] "Enable C reset".
- There is no status message via the process data.

Counter value reset via the "Latch extern" input (Enable extern reset)

The counter value can be set to "0" via the "Latch extern" input.

- Setting the reset value via index 0x80n1:1B [▶ 151] "Reset counter value" (default: 0)
- To activate this function set the bit in index 0x80n0:02 [▶ 150] "Enable extern reset".
- Index 0x80n0:10 [▶ 150] "Extern reset polarity" can be used to specify at which edge the "Latch extern" input is active.
 - 0: "Fall" - the counter is set to "0" with a negative edge
 - 1: "Rise" - the counter is set to "0" with a positive edge

There is no status message via the process data.

4.1.3.3 Set counter value

The counter value can be set to a predefined value at runtime and thus be used for synchronization with other processes. The preset can be activated in the following ways:

- **PLC variable:** [► 68] the counter value can be set from the PLC application ("Set counter value")
- **Zero pulse C input:** [► 68] via the zero pulse C of the encoder ("Set counter on latch C")
- **Latch input:** [► 69] a positive or negative edge at the "Latch extern" input ("Set counter on latch extern on positive/negative edge")

● Multiple activation of "Set counter on ..."

I If several commands are activated to accept the preset counter value, only the command that is set first is accepted by the terminal. All other commands are ignored but remain activated, depending on the system.

- The counter value is set to the preset counter value at the first activated event and confirmed by the bit in process data "Set counter done" (0x60n0:03 [► 152]).
- The counter value specification cannot be reactivated until all activated commands for the transfer of the counter value have been deactivated. This is confirmed by setting the bit in process data "Set counter done" (0x60n0:03) to FALSE.

Set counter value via a PLC variable (Set counter value)

The counter value can be set to a predefined value during runtime via the process data "Set counter" (0x70n0:03). In the PLC this bit can be linked to a digital input, for example, or used directly as a variable.

- Setting the counter value using the process data "Set counter value" (0x70n0:11)
- Activation of the counter value setting via the PLC variable: "Set counter" (0x70n0:03)
- To confirm, the "Set counter done" bit (0x60n0:03) is set to TRUE.
- The counter value setting can only be reactivated once the bit in the process data "Set counter" (0x70n0:03) has been set to FALSE.

Set counter value via input zero pulse C (Set counter on latch C)

The counter value can be set to a preset value during runtime via the process data by means of the zero pulse C.

- Setting the counter value using the process data "Set counter value" (0x70n0:11 [► 155])
- Activation of the counter value setting via zero pulse C:
 - Process data "Set counter on latch C" (0x70n0:08 [► 155]) = TRUE
At the next zero pulse, the counter value (Counter value) is set to the counter value specified in the process data "Set counter value" (0x70n0:11 [► 155]).
- To confirm, the bit in the process data "Set counter done" (0x60n0:03) is set to TRUE.
- The count value preset can only be reactivated via the zero pulse C once the bit in the process data "Set counter on latch C" (0x70n0:08) has been set to FALSE.

Set counter via the “Latch extern” input (Set counter on latch extern on positive/negative edge)

The counter value can be set to a preset value during runtime via the process data by the positive or negative edge at the “Latch extern” input.

- Setting the counter value via the process data “Set counter value” (0x70n0:11)
- Activation of the counter value setting via
 - the positive edge at the “Latch extern” input:
Process data “Set counter on latch extern on positive edge” (0x70n0:0A)
 - the negative edge at the “Latch extern” input:
Process data “Set counter on latch extern on negative edge” (0x70n0:0B)
- If the bit is set (TRUE) in the process data “Set counter on latch extern on positive edge” (0x70n0:0A) or “Set counter on latch extern on negative edge” (0x70n0:0B), the counter value (Counter value) is set to the value specified in the process data “Set counter value” at the next positive or negative edge at the Latch extern input.
- To confirm, the bit in the process data “Set counter done” (0x60n0:03) is set to TRUE.
- The counter value setting cannot be reactivated until the process data “Set counter on latch extern on positive/negative edge” (0x70n0:0A/0B) has been set to FALSE.

4.1.3.4 Detect counting direction

The terminal can be configured via Index 0x80n1:1C "Direction inversion hysteresis" as follows:

- Detect counting direction [► 70]: A positive rotation direction is output as "0" and a negative rotation direction as "1" in the process data "Direction inversion detected" (0x60n2:13).

or

- Detect reversion of rotation: [► 71] If a reversal in the direction of rotation is detected, this is reported in the process data "Direction inversion detected" (0x60n2:13). This function can also be used for standstill monitoring [► 71].

Detect counting direction

- Set the hysteresis via index 0x80n1:1C "Direction inversion hysteresis" = 0
- To detect the counting direction, the position value of the last PLC cycle (pos 1) is subtracted from the position value of the current PLC cycle (pos 2).
- The result is output during the next PLC cycle via the process data "Direction inversion detected" (0x60n2:13). In this case,
 - a positive result is interpreted as a positive direction of rotation
"Direction inversion detected" (0x60n2:13) = 0,
 - a negative result is interpreted as a negative direction of rotation
"Direction inversion detected" (0x60n2:13) = 1.

0x80n1:1C "Direction inversion hysteresis" = 0		
Change in position	Direction of rotation	0x60n2:13 "Direction inversion detected"
pos 2 – pos 1 > 0	Positive direction of rotation (CW)	0
pos 2 – pos 1 < 0	Negative direction of rotation (CCW)	1
pos 2 – pos 1 = 0	No change of direction of rotation	No state change
Counter overflow	No change of direction of rotation	No state change
Counter underflow	No change of direction of rotation	No state change

- When the terminal is powered up, a positive direction of rotation is assumed in the first PLC cycle: "Direction inversion detected" (0x60n2:13) = 0, because a second position value is initially missing for the calculation.
- If an overflow "Counter overflow" (0x60n0:05) or underflow "Counter underflow" (0x60n0:04) of the counter value is detected, the result is corrected internally for the next PLC cycle. See figure (A) below.
- If the counter value is changed externally via the C track or the "Latch extern" input [► 68] and this leads to a negative position jump, this is indicated via process data "Direction inversion detected" (0x60n2:13). See figure (B) below
- If reversion of rotation [► 65] is enabled (index 0x80n0:0E "Reversion of rotation" = TRUE), the logic of the direction of rotation detection also changes.

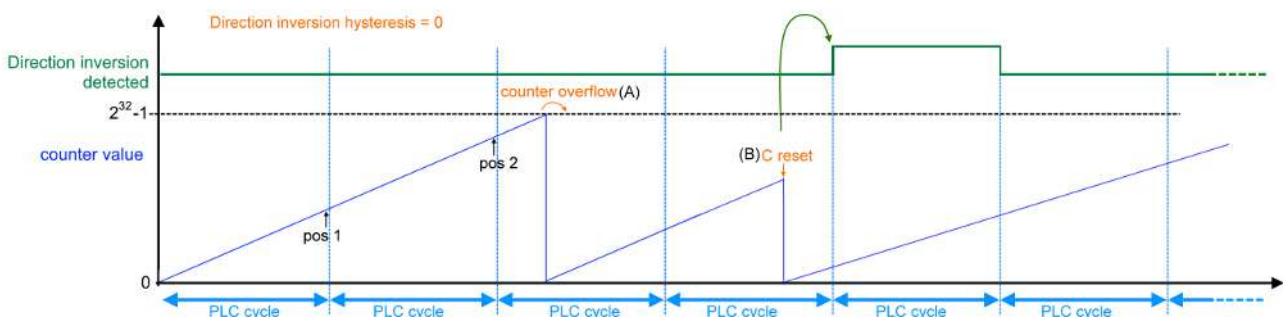


Fig. 37: Detection of the counting direction

Detect reversion of rotation

- Enter the hysteresis as the number of increments via the index 0x80n1:1C "Direction inversion hysteresis". Select a value greater than 0.
- If a direction inversion is detected, an internal counter evaluates the edges detected directly one after the other for each direction of rotation and compares them with the number entered in index 0x80n1:1C.
- If the counter value exceeds the value entered in index 0x80n1:1C, the bit in the process data "Direction inversion detected" (0x60n2:13) is set during the next PLC cycle. The bit remains active for one cycle only.
- The bit remains active if a further direction inversion is detected within the next cycle.
- The hysteresis is considered separately for each PLC cycle, so the counter is restarted for each cycle. There is no monitoring across PLC cycles.
- If reversion of rotation [► 65] is enabled (index 0x80n0:0E "Reversion of rotation" = TRUE), the logic of the direction of rotation detection also changes.
- If several changes of direction occur within one PLC cycle, the display only indicates that at least one change of direction has been detected.

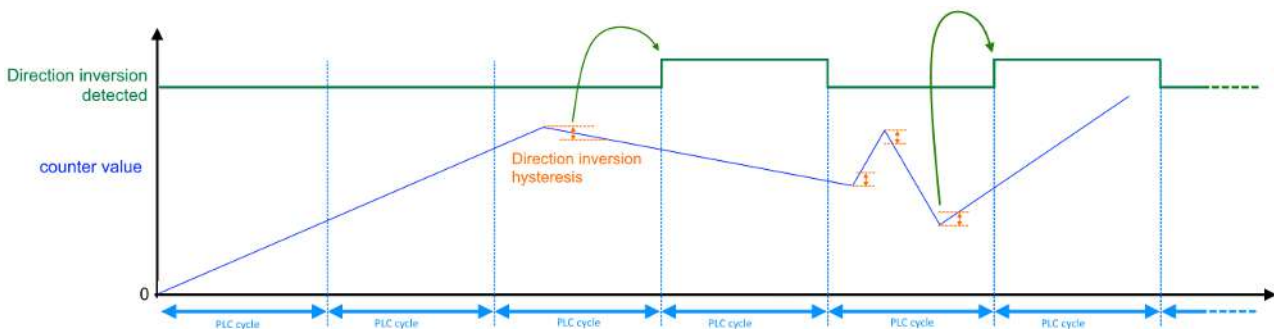


Fig. 38: Detection of reversion of rotation

Standstill monitoring

Detection of direction inversion can also be used for standstill monitoring. If an almost constant counter value is expected, the hysteresis (index 0x80n1:1C) can be used to monitor whether the value is within the window. A slight jitter of the counter value is therefore still accepted as a permissible value. If the limit is exceeded, the bit in the process data "Direction inversion detected" (0x60n2:13) is set during the next PLC cycle.

- If the direction changes again within the hysteresis [number of increments] specified in index 0x80n1:1C, no change of direction is indicated (standstill). See figure (A) below.
- If the hysteresis [number of increments] specified in index 0x80n1:1C is exceeded after a change of direction, the change of direction is indicated in the next cycle by setting the bit in the process data "Direction inversion detected" (0x60n2:13). See figure (B) below.

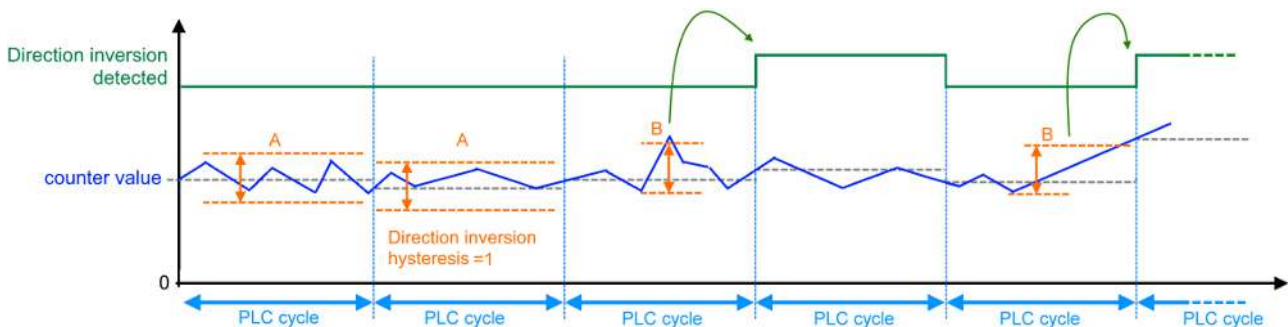


Fig. 39: Standstill monitoring with hysteresis and detection of reversion of rotation

Drifting of the counter value

i Reliable detection of a drifting counter value can only be guaranteed if the value in index 0x80n1:1C "Direction inversion hysteresis" is "1". Or additional monitoring of the counter value in the PLC.

4.1.3.5 Save counter value

The latch function enables the current counter value to be stored in separate process data, independent of the cycle time. The input “Gate” can be parameterized as a second external latch input with separate process data. The latch function can be triggered as follows:

- Latch input: [► 73] positive/negative edge at the latch input
Process data “Enable latch extern on positive/negative edge”
- Gate input [► 74]: positive/negative edge at the input “Gate”
Process data “Enable latch extern 2 on positive/negative edge”
- Zero pulse C input: [► 75] via zero pulse C
Process data “Enable latch C”

Index 0x80n0:22 [► 150] “Enable continuous latch extern” and 0x80n0:23 [► 150] “Enable continuous latch extern 2” can be used to parameterize whether the function is executed at every parameterized external edge at the latch input or only once after every activation.

A workpiece measurement [► 75] can be realized by using two independent latch inputs.

i Multiple activation of the latch function

If several commands are activated simultaneously to save the counter value in the “Latch value” process data (0x60n0:12 [► 152]), only the command that is set first is accepted by the terminal.

- The counter value is stored in the process data “Latch value” (0x60n0:12) at the next occurring event and confirmed with the corresponding bit.
 - All other activated events are ignored.
 - The counter value storage cannot be reactivated until all activated commands for latching the value have been deactivated. This also applies if they were activated after confirmation by the occurring event.
-

Save the counter value via a positive/negative edge at the latch input (Enable latch extern on positive/negative edge)

- The counter value at the “Latch extern” input can be saved via:
 - Process data “Enable latch extern on positive edge” (0x70n0:02 [► 155]) = TRUE
At the first external latch pulse with positive edge, the current counter value is stored in the process data “Latch value” (0x60n0:12 [► 152]).
 - Process data “Enable latch extern on negative edge” (0x70n0:04 [► 155]) = TRUE
At the first external latch pulse with negative edge the current counter value is stored in the process data “Latch value” (0x60n0:12 [► 152]).
 - Simultaneous activation of the bits in the process data “Enable latch extern on positive edge” (0x70n0:02) and “Enable latch extern on negative edge” (0x70n0:04)
The current counter value is stored in the process data “Latch value” (0x60n0:12), at the first external latch pulse, independent of the edge polarity.
- Specification whether it is necessary to reactivate the command to save the counter value via:
 - “Enable continuous latch extern” Index 0x80n0:22 [► 150] = FALSE
The following pulses at the “Latch extern” input have no effect on the latch value in the process data “Enable latch extern on positive edge” (0x70n0:02) and “Enable latch extern on negative edge” (0x70n0:04) when the bit in the process data “Latch value” (0x60n0:12) is set.
Only when the bit in the process data “Latch extern valid” (0x60n0:02 [► 152]) is set to FALSE can a new counter value be written to the latch input in the process data “Latch value” (0x60n0:12)
 - “Enable continuous latch extern” Index 0x80n0:22 [► 150] = TRUE
The counter value is written to the process data “Latch value” (0x60n0:12) each time a configured edge occurs at the “Latch extern” input.
There is no need to reactivate the process data “Enable latch extern on positive edge” (0x70n0:02) and “Enable latch extern on negative edge” (0x70n0:04).
- Saving of the count value in the process data “Latch value” (0x60n0:12) is confirmed by the bit in the process data “Latch extern valid” (0x60n0:02).
- The status of the “Latch extern” input can be monitored using the process data “Status of extern latch” (0x60n2:14 [► 154]).

i Simultaneous activation of “Enable continuous latch extern” and “Enable latch C”

When using the process data “Enable latch extern on positive/negative edge” (0x70n0:02/0x70n0:04) simultaneously while activating 0x80n0:22 “Enable continuous latch extern,” with the process data “Enable latch C” (0x70n0:01)

- only the first event, either pos./neg. edge at the “Latch extern” input or the zero pulse C, is written to the process data “Latch value” (0x60n0:12).
- saving of the count value is confirmed in each case via the process data “Latch extern valid” (0x60n0:02) or “Latch C valid” (0x60n0:01 [► 152]).
- all further edges at the “Latch extern” input are ignored.
- The counter value storage cannot be reactivated until all activated commands for latching the value have been deactivated.

Save the counter value via a positive/negative edge on the “Gate” input (Enable latch extern 2 on positive/negative edge)

The “Gate” input may be used as a second latch input (Latch extern 2). To do this, the gate should be disabled.

Deactivation of the gate



Set the “Gate polarity” bit (index 0x80n0:04 [► 150]) to “0 – Disable gate” in order to be able to use the “Latch extern 2” input without locking the counter value after the latch event.

- The counter value at the “Latch extern 2” input can be saved via:
 - Process data “Enable latch extern 2 on positive edge” (0x70n0:0C [► 155]) = TRUE
At the first external pulse with positive edge at the “Gate” input, the current counter value is stored in the process data “Latch value 2” (0x60n0:22 [► 152]).
 - Process data “Enable latch extern 2 on negative edge” (0x70n0:0D [► 155]) = TRUE
At the first external pulse with negative edge at the “Gate” input, the current counter value is stored in the process data “Latch value 2” (0x60n0:22).
 - Simultaneous activation of the bits in the process data “Enable latch extern 2 on positive edge” (0x70n0:0C) and “Enable latch extern 2 on negative edge” (0x70n0:0D)
When the first pulse is received at the “Gate” input—regardless of the polarity of the edge—the current counter value is stored in the process data “Latch value 2” (0x60n0:22).
- Specification whether it is necessary to reactivate the command to save the counter value via:
 - “Enable continuous latch extern 2” Index 0x80n0:23 [► 150] = FALSE
The following pulses at the “Gate” input have no effect on the latch value in the process data “Latch value 2” (0x60n0:22) when the bit in the process data “Enable latch extern 2 on positive edge” (0x70n0:0C) or “Enable latch extern 2 on negative edge” (0x70n0:0D) is set.
Only when the bit in the process data “Latch extern 2 valid” (0x60n2:12 [► 154]) is FALSE can a new counter value be written to the “Gate” input in the process data “Latch value 2” (0x60n0:22).
 - “Enable continuous latch extern 2” Index 0x80n0:23 [► 150] = TRUE
The counter value is written to the process data field “Latch value 2” (0x60n2:22) each time a configured edge is detected at the “Gate” input.
There is no need to reactivate the bits in the process data “Enable latch extern 2 on positive edge” (0x70n0:0C) or “Enable latch extern 2 on negative edge” (0x70n0:0D).
- The status of the input “Gate” can be recorded via the process data “Status of input gate” (0x60n0:0C [► 152]).
- Saving of the counter value in the process data “Latch value 2” (0x60n0:22) is confirmed by the bit in the process data “Latch extern 2 valid” (0x60n2:12).

Simultaneous use of Gate and Latch extern 2



When using the index 0x80n0:04 [► 150] “Gate polarity” (1 = “Enable pos. gate”) and simultaneous activation of the output process data “Enable latch extern 2 on positive edge” (0x70n0:0C [► 155]), a positive edge on the “Gate” input first stores the current counter value in the input process data “Latch value 2” (0x60n0:22 [► 152]). After that, the counter value is locked.

The same applies to the use of index 0x80n0:04 “Gate polarity” (2 = “Enable neg. gate”) and the simultaneous activation of the output process data “Enable latch extern 2 on negative edge” (0x70n0:0D [► 155]) when a negative edge occurs at the “Gate” input.

Save counter value via the zero pulse C input (Enable latch C)

The counter value can be stored at runtime via the process data and the zero pulse in "Latch value" (0x60n0:12 [► 152]).

- The function is activated by setting the bit in process data "Enable latch C" (0x70n0:01) [► 155] to TRUE.
- The current counter value is saved in the process data "Latch value" (0x60n0:12) with the next zero pulse at input C. The subsequent pulses have no influence on the latch value.
- The bit in process data "Latch C valid" (0x60n0:01) [► 152]) is set to TRUE.
- After reactivating the process data "Enable latch C" (0x70n0:01) a new counter value cannot be written to the Latch input until the values of the "Enable latch C" bit (0x70n0:01) and the "Latch C valid" bit (0x60n0:01) are FALSE.

Workpiece measurement

The two latch functions "Latch extern" and "Latch extern 2" can be used to measure workpieces or distances between two workpieces. To use the "Latch extern 2" function, the gate should be disabled via the index 0x80n0:04 [► 150] "Gate polarity" ("Disable gate" = 0).

Depending on the activation of the indices, the counter value may be stored via a positive or negative edge.



"Continuous latch" for workpiece measurement

To prevent the stored value from being overwritten, it is advisable to set the setting in index 0x80n0:22 [► 150] "Enable continuous latch extern" to FALSE for the workpiece measurement.

Exemplary workpiece measurement sequence

- Process data "Enable latch extern on positive edge" (0x70n0:02 [► 155]) = TRUE:
When the first pulse with a positive edge is received at the "Latch extern" input, the current counter value is stored in the process data "Latch value" (0x60n0:12 [► 152]).
- The count value is stored in the process data "Latch value" (0x60n0:12) via the bit in the process data "Latch extern valid" (0x60n0:02 [► 152]).
- Process data "Enable latch extern 2 on negative edge" (0x70n0:0D [► 155]) = TRUE:
At the first external pulse with negative edge at the "Gate" input the current counter value is stored in the process data "Latch value 2" (0x60n0:22 [► 152]).
- Saving of the counter value in the process data "Latch value 2" (0x60n0:22) is confirmed by the bit in the process data "Latch extern 2 valid" (0x60n2:12).
- The end of the measurement is confirmed by the two set bits in the process data "Latch extern valid" (0x60n0:02) and "Latch extern 2 valid" (0x60n2:12).
- The workpiece length can be calculated from the difference between the two values "Latch value" and "Latch value 2".
- A new workpiece measurement can be started after the bits in the process data "Enable latch extern on positive edge" (0x70n0:02) and "Enable latch extern 2 on negative edge" (0x70n0:0D) have been deactivated.

4.1.3.6 Lock counter value

The gate function enables locking of the counter (0x60n0:11 [► 152]).

The counter is locked at the first pulse at the “Gate” input. Subsequent pulses have no influence on the counter value. This allows a timeframe to be defined in which counting signals are acquired. The gate function can be triggered by:

- Gate input: [► 76] a positive/negative edge at the “Gate” input (Enable pos./neg. gate),
- PLC variable: [► 76] the counter can be locked from the PLC application (Set software gate).

The “Gate” input may be used as a second latch input (Latch extern 2).

Lock counter value via a positive/negative edge at the gate input (Enable pos./neg. gate)

- The level at the gate input at which the counter value is locked during runtime can be specified via index 0x80n0:04 [► 150] “Gate polarity”.
 - 0: Disable gate
The “Gate” input is disabled. It can still be used as “Latch extern 2” input.
 - 1: Enable pos. gate
The counter value is locked with a HIGH level at the “Gate” input.
 - 2: Enable neg. gate
The counter value is locked with LOW level at the “Gate” input.
- The current level at the “Gate” input is displayed via process data “Status of input gate” (0x60n0:0C [► 152]).

● Simultaneous use of Gate and Latch extern 2

I When using the index 0x80n0:04 [► 150] “Gate polarity” (1 = “Enable pos. gate”) and simultaneous activation of the output process data “Enable latch extern 2 on positive edge” (0x70n0:0C [► 155]), a positive edge on the “Gate” input first stores the current counter value in the input process data “Latch value 2” (0x60n0:22 [► 152]). After that, the counter value is locked.

The same applies to the use of index 0x80n0:04 “Gate polarity” (2 = “Enable neg. gate”) and the simultaneous activation of the output process data “Enable latch extern 2 on negative edge” (0x70n0:0D [► 155]) when a negative edge occurs at the “Gate” input.

Lock counter value via a PLC variable (Set software gate)

The counter value can be locked from the PLC application.

- Output process data “Set software gate” (0x70n0:09 [► 155]) = TRUE
The counter is locked.
- To confirm, set the bit in the input process data “Software gate valid” (0x60n2:11 [► 154]) = TRUE.
- Output process data “Set software gate” (0x70n0:09) = FALSE
The counter is unlocked.

4.1.4 Extended functionalities single-channel mode 1xABC

4.1.4.1 Frequency measurement

In addition to the count value, the frequency value (Frequency value) can also be calculated and displayed. The following limit values apply to the determination of measured values:

Measured value output	Measured value limit		Comment
	Lower	Top	
Frequency value	0.095 Hz	5 MHz	With 4-fold evaluation Signal type: "RS422 (diff. input)"
	0.095 Hz	1 MHz	With 4-fold evaluation Signal type: "TTL (single ended), open collector"
	0.095 Hz	100 kHz	With 4-fold evaluation Signal type: "open collector"

Frequency measurement procedure (Frequency value)

The frequency is calculated from the number of increments or position value changes within a time interval. The result is output via the process data "Frequency value" (0x60n0:13 [► 152]).

Frequency = number of periods / time interval	
Number of periods	The number of complete periods on track A within the timeframe (0x80n0:11 [► 150]) is measured. Counting starts with the first positive edge within the timeframe (index 0x80n0:11 "Frequency window").
Time interval	The time measurement starts with the first positive edge on track A within the "Frequency window" and ends with the last negative edge within the "Frequency window". The time is measured with a resolution of 10 ns. Special case: If no full period is measured within the timeframe (Frequency window), another timeframe is started. The maximum time measurement for recording an entire period is limited by the wait time (Frequency wait time).

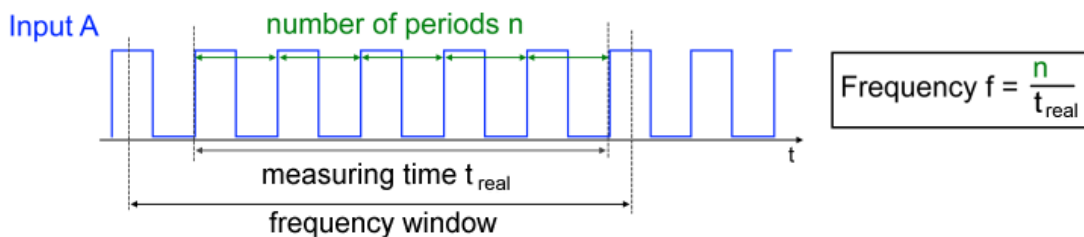


Fig. 40: Frequency measurement - "Frequency value"

- The frequency window is selected in index 0x80n0:11 "Frequency window". The default value is 10 ms. Follow the instructions below to select the correct timeframe.
- "Frequency scaling" (index 0x80n0:13 [► 150]) indicates the resolution of the output frequency. The default value is 0.01 Hz. The frequency can also be output in the unit 1 Hz (set 0x80n0:13 "Frequency scaling" to 1_{dec}). If other resolutions are required, the conversion can be done via 0x80n0:1D [► 150] "Frequency numerator".
- The calculated frequency value is output via the input process data "Frequency value" (0x60n0:13 [► 152]).
- The calculation is carried out acyclically and without reference to the distributed clock system and is therefore independent of the operation mode.
- Locking the counter value via the gate, a C-reset or external reset has no effect on the frequency calculation.

Correct selection of the timeframe:

In delivery state the timeframe for the frequency measurement is set to 10 ms.

The accuracy and size of the determined frequency depends on the size of the timeframe (0x80n0:11 [► 150] “Frequency window”), which must be selected to match the application. The minimum value to be entered here is twice the period value of the smallest measured frequency.

$$\text{Frequency window} \geq 2 * \frac{1}{f_{\min}}$$

At constant velocities, select a larger timeframe so that the best possible averaging can take place.

In situations where frequent positive or negative accelerations are encountered, select a smaller timeframe in order to be able to respond more quickly to changing position values. Alternatively, period value measurement can be used for situations with variable speeds.

Special case: frequency measurement

If no full period is detected within the “Frequency window” (see figure (1) below), another “Frequency window” timeframe is started in order to record at least one full period (see figure (2) below). This happens until the maximum waiting time (0x80n0:17 [► 150] “Frequency wait time”) has elapsed. Until then, the last valid value in the input process data “Frequency value” (0x60n0:13 [► 152]) is displayed.

If no full period is detected within the waiting time, the measurement is discarded and the output in the process data “Frequency value” (0x60n0:13) is set to “0”.

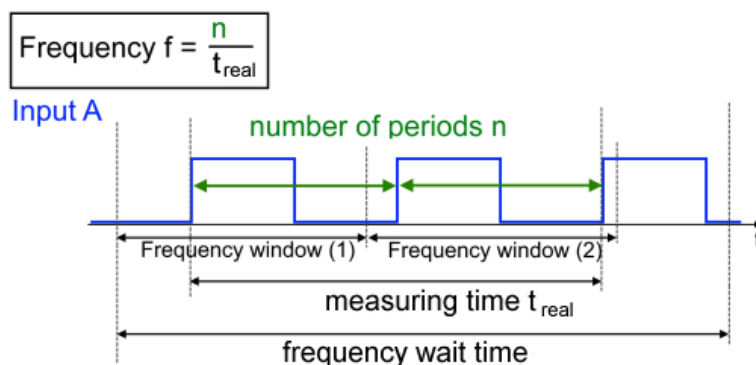


Fig. 41: Frequency measurement outside the frequency window with waiting time

**Difference between frequency and period value measurement**

The period value is recalculated for each cycle and output in the process data. The frequency measurement always averages the measured periods over a timeframe. Thus, “Period value” is a current value, and “Frequency value” is an average value.

4.1.4.2 Period value measurement

In addition to the count value, the period value (Period value) can also be calculated and displayed. The following limit values apply to the determination of measured values:

Measured value output	Measured value limit		Comment
	Lower	Top	
Period value	0.20 μ s	21 s	With 4-fold evaluation, signal type: "RS422 (diff. input)"
	1 μ s	21 s	With 4-fold evaluation, signal type: "TTL (single ended)", "open collector"

Period value measurement sequence (Period value)

- For the period value measurement, the time between two positive edges of input A is measured with a resolution of 10 ns.
- In each case the last period within the PLC cycle is considered and output as separate process data "Period value" (0x60n0:14 [► 152]).
- "Period scaling" (index 0x80n0:14) indicates the resolution of the output period value. The default value is 10 ns. Alternatively the period value can be output in the unit 100 ns (set 0x80n0:14 "Period scaling" to 100_{dec}) or 500 ns (set 0x80n0:14 "Period scaling" to 500_{dec}).

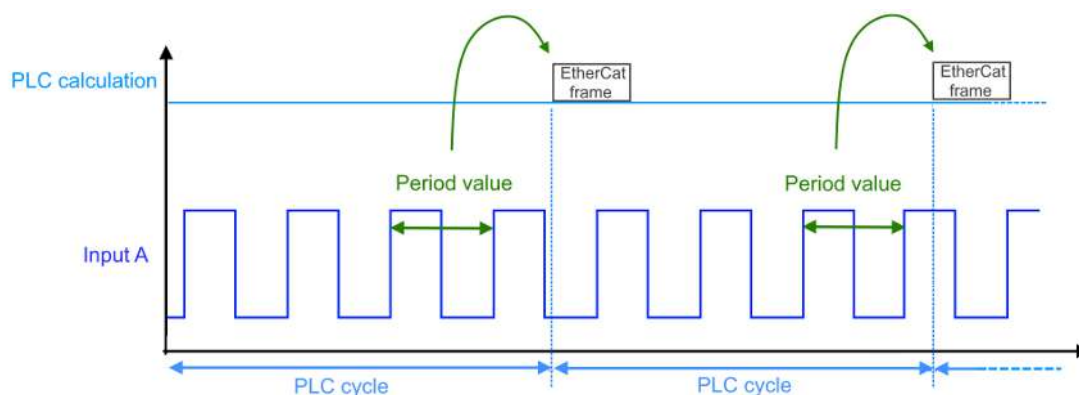


Fig. 42: Period value measurement

- If no full period is detected within a PLC cycle (two positive edges of input A), the last valid value is output.
- The period measurement continues across cycles. As soon as a new value is available, the process data "Period value" (0x60n0:14 [► 152]) is updated.
- If no full period is detected within 21 s, the measurement is discarded and the output in the process data "Period value" (0x60n0:14 [► 152]) is set to the maximum value 2147483648.

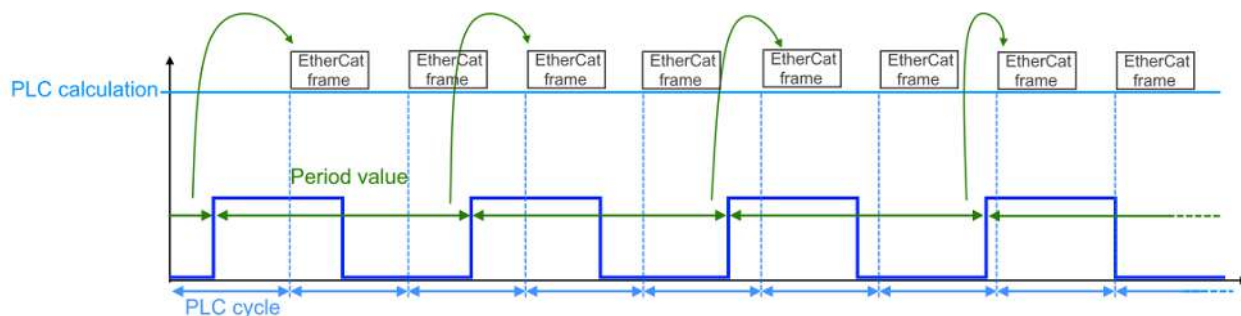


Fig. 43: Period value measurement for long periods



Difference between frequency and period value measurement

The period value is recalculated for each cycle and output in the process data. The frequency measurement always averages the measured periods over a timeframe. Thus, "Period value" is a current value, and "Frequency value" is an average value.

4.1.4.3 Velocity, speed calculation

In addition to the counter value, the velocity and speed are also be measured. The measured values are determined through parameterization of the frequency values. The following limit values apply:

Measured value output	Measured value limit		Comment
	lower	top	
Frequency value	0.095 Hz	5 MHz	with 4-fold evaluation Signal type: "RS422 (diff. input)"
	0.095 Hz	1 MHz	with 4-fold evaluation Signal type: "TTL (single ended)"
	0.095 Hz	100 kHz	with 4-fold evaluation Signal type: "open collector"

The frequency measurement is carried out as described in chapter "Frequency measurement (Frequency value)". In addition, the frequency value can be converted using the two indices [0x80n0:1D](#) [[150](#)] "Frequency numerator" and [0x80n0:1E](#) [[150](#)] "Frequency denominator".

Index (hex)	Name	Meaning	Default
80n0:1D	Frequency numerator	Frequency numerator Factor for normalizing the frequency, e.g. the time unit	0x0000001 (1 _{dec})
80n0:1E	Frequency denominator	Frequency denominator, Factor for normalizing the frequency, e.g. speed calculation	0x0000001 (1 _{dec})

Thus, the frequency can be normalized for application-specific speed measurement. The measured value continues to be output in the process data via "Frequency value" ([0x60n0:13](#) [[152](#)]).

The calculated measured value has the following relationship to the frequency:

$$\text{Determination of measured values} = \text{Frequency} * \frac{\text{Frequency numerator}}{\text{Frequency denominator}}$$

Example for velocity calculation in m/s

- 200 mm travel corresponds to one full mechanical revolution of an encoder.
- The encoder has a 12-bit resolution, i.e. 4096 lines, which corresponds to 4096 periods on track A.

The velocity value is determined as follows:

$$v \left[\frac{\text{mm}}{\text{s}} \right] = \text{Frequency value} \cdot \frac{\text{periods}}{\text{s}} * \frac{200 \text{ mm}}{4096 \text{ periods}}$$

$$v \left[\frac{\text{m}}{\text{s}} \right] = \text{Frequency value} \cdot \frac{\text{periods}}{\text{s}} * \frac{200 \text{ mm}}{4096 \text{ periods}} * \frac{1 \text{ m}}{1000 \text{ mm}}$$

Index (hex)	Name	Example: velocity in m/s	Comment
80n0:1D [150]	Frequency numerator	0x00000C8 (200 _{dec})	Travel path, conversion to m via "Frequency denominator"
80n0:1E [150]	Frequency denominator	0x003E8000 (4096000 _{dec})	Specification of the number of periods over the travel path and conversion of the travel path to m

Example Calculation of speed f_{rot} in revolutions/s

- After one full rotation, 4-fold evaluation (0x80n0:06 [► 150] "Evaluation mode") results in a numerator value of 16384 increments. This corresponds to 4096 periods on track A.
- "Frequency numerator" can be used to convert the time unit into minutes. Note the scaling of the frequency value (0x80n0:13 [► 150] "Frequency scaling"):

Conversion to minutes depending on "Frequency scaling"			
Index (hex)	Entry	Index (hex)	Entry
0x80n0:13 [► 150] Frequency scaling	100 _{dec} : 0.01 Hz	0x80n0:1D [► 150] Frequency numerator	0x00001770 (6000 _{dec})
	1 _{dec} : 1 Hz		0x0000003C (60 _{dec})

$$f_{\text{rot}} \left[\frac{\text{rotations}}{\text{s}} \right] = \text{Frequency value} \frac{\text{periods}}{\text{s}} * \frac{6000 \text{ rotations}}{4096 \text{ periods}}$$

$$f_{\text{rot}} \left[\frac{\text{rotations}}{\text{min}} \right] = \text{Frequency value} \frac{\text{periods}}{\text{s}} * 60 \frac{\text{s}}{\text{min}} * \frac{6000 \text{ rotations}}{4096 \text{ periods}}$$

Index (hex)	Example: Speed f_{rot} in rpm	Comment
80n0:1D [► 150] Frequency numerator	0x0001770 (6000 _{dec})	Output of the value in 0.01 rpm
80n0:1E [► 150] Frequency denominator	0x0001000 (4096 _{dec})	Conversion factor in periods / m

4.1.4.4 Duty cycle evaluation

The duty cycle describes the ratio of pulse duration t_{ON} to period value T .

Duty cycle [0.01%] = Pulse duration t_{ON} / Period value T * 100

The following process data are available:

Index (hex)	Name	Meaning	Default
60n0:23	Duty cycle	Ratio of pulse duration t_{ON} to period value T . Output in 1/100	0x0000 (0 _{dec})
60n0:24	Duty cycle min	Smallest measured "duty cycle" value during the current measurement	0x2710 (10000 _{dec})
60n0:25	Duty cycle max	Largest measured "duty cycle" value during the current measurement	0x0000 (0 _{dec})

The duty cycle is measured as follows:

- The pulse duration t_{ON} is measured. This is the time between the positive and negative edge of input A.
- The period value T is measured. This is the time between two positive edges of input A.
- The times are measured with a resolution of 10 ns.
- The last period within each PLC cycle is considered and output as separate input process data "Duty cycle" (0x60n0:23).
- The output is 1/100 of the measured value.
- The duty cycle measurement delivers valid results in RS422 mode up to 1 MHz with an accuracy of typically 1...2%. Larger measuring errors may occur at input frequencies above 1 MHz.

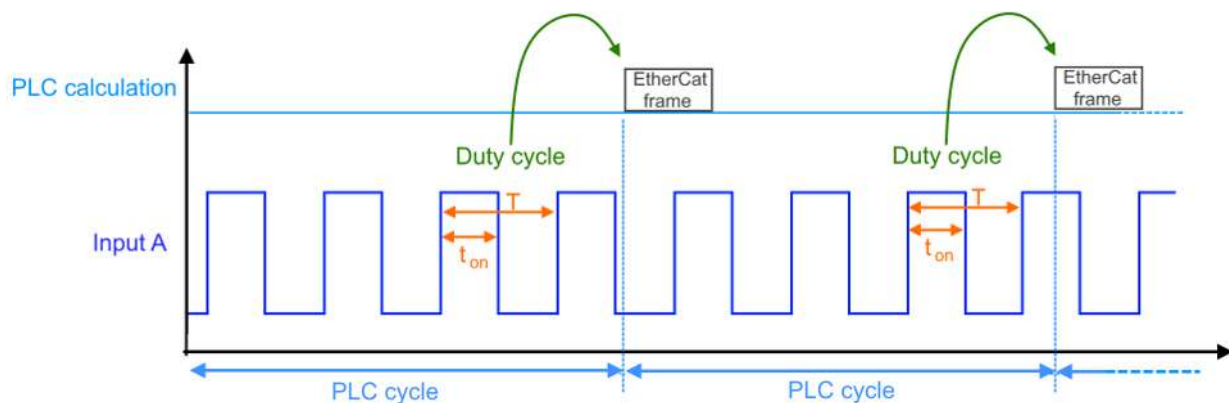


Fig. 44: Duty cycle measurement

The smallest and largest measured "Duty cycle" value can be reset via the command object in index 0xFB00:01 "Request".

0xFB00:01 "Request"	Description
0x9130	Set the index 0x6000:24 "Duty cycle min" for channel 1 to zero
0x9140	Set the index 0x6000:25 "Duty cycle max" for channel 1 to zero
0x9131	Set the index 0x6010:24 "Duty cycle min" for channel 2 to zero
0x9141	Set the index 0x6010:25 "Duty cycle max" for channel 2 to zero

4.1.4.5 Micro-increments

The "micro-increments" function offers the option to interpolate additional increments between the counted encoder increments and thus increase the resolution of the counter value.

Functional principle of micro-increments

The following figure illustrates the functional principle of micro-increments. It is based on the interpolation of increments (orange) within real measured encoder increments (blue). To simplify the display, only four micro-increments are shown between the encoder increments. The current velocity is measured based on the internal period value measurement, and the micro-increments are interpolated accordingly. The interpolation resolution is 8 bits, which corresponds to 256 values. The counter value with micro-increments comes close to the real axis position. This is particularly useful at slow velocities, since an encoder with low resolution becomes a high-resolution axis encoder when micro-increments are enabled.

Example:

- Encoder with 1,024 lines
- 4-fold evaluation
- Micro-increments enabled, 8 bits

$$1024 \text{ lines} * 4\text{-fold evaluation} * 256 \text{ micro-increments} = 1,048,576 \text{ lines}$$

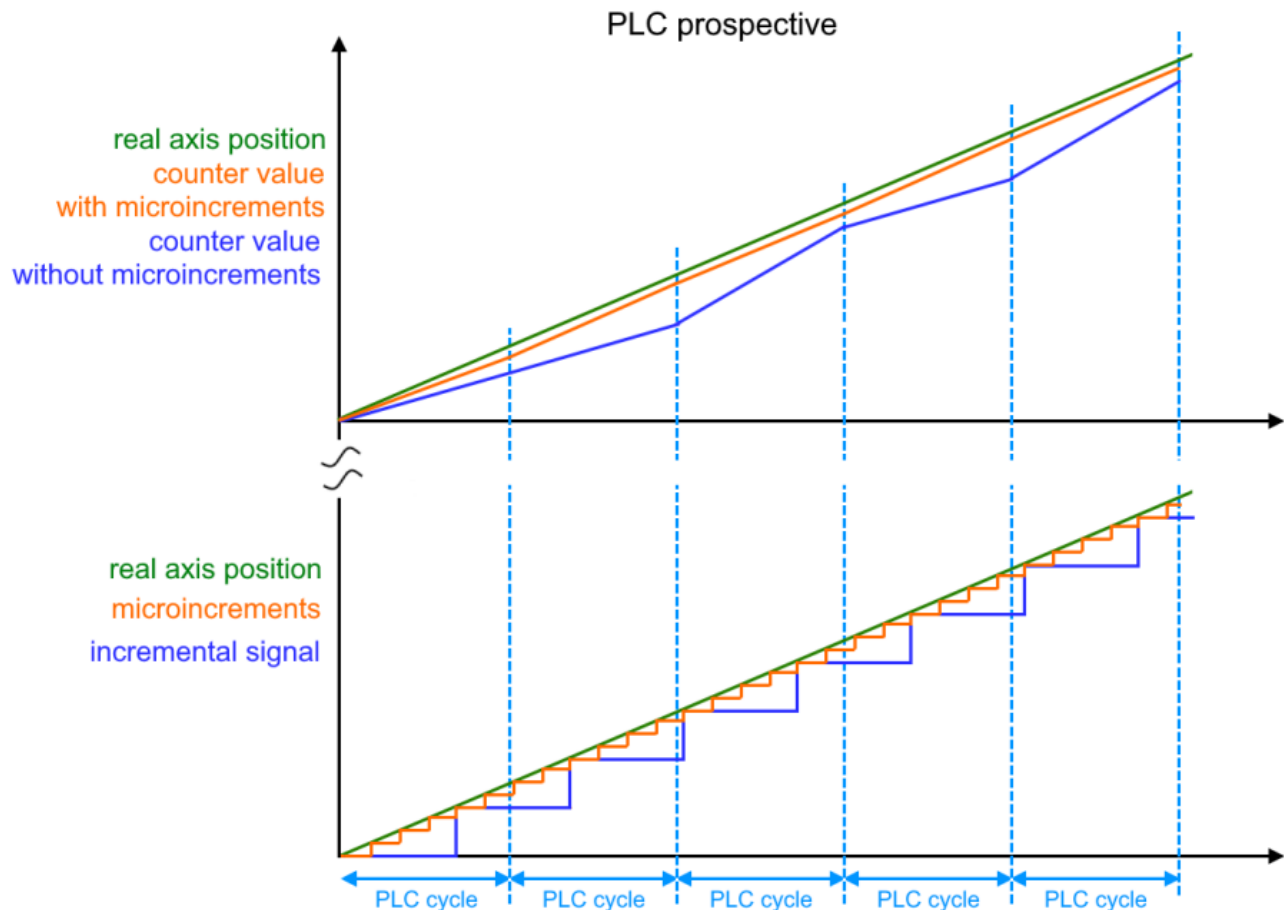


Fig. 45: Functional principle of micro-increments



DC mode for micro-increments

In order to be able to use the micro-increments function in a meaningful way, the terminal should be operated in "DC-Synchron" or "DC-Synchron (input based)" mode. Due to the distributed clocks technology the counter value is determined in a cyclically constant manner.

Microincrements sequence

- Enable microincrements via the index 0x80n0:0A “Enable micro increments”
- The microincrements are represented in the last 8 bits of the counter value in the input process data “Counter value” (0x60n0:11).
- The period value of the input signal should be greater than 1.34 μs , so that the microincrements can still be calculated. If this is not the case, the violation is displayed in the input process data “Extrapolation stall” (0x60n0:08).
- If the “Extrapolation stall” bit is TRUE, the 8 bits of the microincrements in the “Counter value” are set to zero.

4.1.4.6 Timestamp function

The timestamp is made possible by the distributed clocks technology in the EtherCAT system. This local clock can be used to synchronize the data acquisition.

The ED5112 provides a timestamp for the following input signals:

- Last counter change in the PLC cycle [► 85]
- Zero pulse C input: [► 85] when storing the counter value on the positive edge of the zero pulse C
- Latch input: [► 86] when storing the counter value on the selected edge of the latch input
- Gate input: [► 86] when storing the counter value on the selected edge of the “Gate” input

Note on using the timestamp function

I In order to be able to use the timestamp function, the terminal must be operated in “DC-Synchron” or “DC-Synchron (input based)” mode.

The terminal provides the timestamp in a range of 64 bits, optionally with only 32 bits. The timestamps are contained in the following “Predefined PDO Assignment [► 58]”:

Predefined PDO Assignment
1.Ch Standard, 1xABC, extended DC mode, 64 Bit time stamp
1.Ch Standard, 1xABC, extended DC mode, 32 Bit time stamp

They can be selected or deselected as optional PDOs.

PDO assignment	Name	Description
0x1A0D [► 53]	ENC Timestamp Channel 1	Contains timestamps in the 64 bit range for channel 1
0x1A0E [► 54]	ENC Timestamp Compact Channel 1	Contains timestamps in the 32 bit range for channel 1

Timestamp for the last counter change in the PLC cycle

The process data “Timestamp” (0x60n0:16 [► 152]) indicates the timestamp of the last registered counting pulse in the PLC cycle. This means, depending on the counter evaluation mode [► 62] (index 0x80n0:06 [► 150] “Evaluation mode”) the timestamp is output based on:

0x80n0:06 “Evaluation mode”	0x60n0:16 “Timestamp”
0	4-fold (default) last positive or negative edge on track A or B
1	1-fold last positive edge on track A
2	2-fold last positive or negative edge on track A

Timestamp on input zero pulse C

The process data “Timestamp C” (0x60p0:1F [► 152]) outputs the timestamp of the last registered positive edge of the zero pulse C when the counter value is saved.

Parameterization of the zero pulse C input	0x60p0:1F: “Timestamp C” returns the timestamp:
0x70p0:01	Enable latch C the positive edge of the zero pulse C at which the counter value was stored in the input process data “Latch value” (0x60p0:12 [► 152])

Depending on the number of channels, the following applies: p = 0 for Ch1, p = 1 for Ch2

Timestamp for the “Latch extern” input

The input process data “Timestamp latch” (0x60p0:20 [► 152]) specifies the timestamp for the selected edge of the “Latch extern” input. This means that, depending on the parameterization of the “Latch extern” input, the timestamp is valid for:

Parameterization of the Latch input		0x60p0:20 “Timestamp latch” returns the timestamp based on:
0x70p0:02 [► 155]	Enable latch extern on positive edge	the last positive edge at the “Latch extern” input, at which point the counter value was stored in the input process data “Latch value” (0x60p0:12 [► 152])
0x70p0:04 [► 155]	Enable latch extern on negative edge	the last negative edge at the “Latch extern” input at which the counter value was stored in the process data “Latch value” (0x60p0:12)
Depending on the number of channels, the following applies: p = 0 for Ch1, p = 1 for Ch2		

Timestamp on “Gate” input

The input process data “Timestamp latch 2” (0x60p0:21 [► 152]) specifies the timestamp on the selected edge of the “Gate” input. The “Gate” input can also be used as “Latch extern 2” input. Depending on the parameterization of the “Latch extern 2” input the timestamp is valid for:

Parameterization of the “Latch 2” input		0x60p0:21 “Timestamp latch 2” returns the timestamp based on:
0x70p0:0C [► 155]	Enable latch extern 2 on positive edge	the last positive edge at the “Gate” input, at which point the counter value was stored in the process data “Latch value 2” (0x60p0:22 [► 152])
0x70p0:0D [► 155]	Enable latch extern 2 on negative edge	the last negative edge at the “Gate” input, where the counter value was stored in the input process data “Latch value 2” (0x60p0:22)
Depending on the number of channels, the following applies: p = 0 for Ch1, p = 1 for Ch2		

4.1.4.7 Adjustable interference pulse filters

Input filters are used for interference suppression at the encoder and digital inputs. Different filter frequencies can be parameterized according to the application.

The individual inputs are subject to the following filter frequencies:

Inputs	Max. recommended filter frequency
Encoder Inputs: Track A, Track B, Track C	RS422 mode: 5 MHz TTL mode: 1 MHz Open collector: 100 kHz
Latch input	1 MHz
Gate input	1 MHz
Digital input	100 kHz (not adjustable)

Filter function sequence

- The filter is disabled on delivery
- The filter can be enabled via index 0x80n0:08 "Disable filter" = FALSE.
- The filter is parameterized via index 0x80n1:19 "Filter settings". The following filter frequencies are available:

Index 0x80n1:19 "Filter settings"		Default parameters for 0x80n1:1D "Counter mode"	
Setting	Meaning	Setting	Meaning
10 _{dec} : 10 kHz	10 kHz filter		
25 _{dec} : 25 kHz	25 kHz filter		
50 _{dec} : 50 kHz	50 kHz filter		
100 _{dec} : 100 kHz	100 kHz filter	0x80n1:1D "Counter mode"	
		4 _{dec}	Encoder open collector
		5 _{dec}	Counter open collector
250 _{dec} : 250 kHz	250 kHz filter		
500 _{dec} : 500 kHz	500 kHz filter		
1000 _{dec} : 1 MHz	1 MHz filter	0x80n1:1D "Counter mode"	
		2 _{dec}	Encoder TTL (single ended)
		3 _{dec}	Counter TTL (single ended)
2500 _{dec} : 2.5 MHz	2.5 MHz filter		
5000 _{dec} : 5 MHz	5 MHz filter	0x80n1:1D "Counter mode"	
		0 _{dec}	Encoder RS422 (diff. input)
		1 _{dec}	Counter RS422 (diff. input)

- If the filter is parameterized < 1 MHz, it is also active for the "Latch" and "Gate" inputs.
- If a frequency overrun is detected with the activated filter (0x80n0:08 and 0x80n1:19), a counter in index 0xA0n0:16 is incremented.

Index (hex)	Name	Description
0xA0n0:14	Filter violation counter extern latch	Filter frequency overshoot counter for the "Latch extern" input
0xA0n0:15	Filter violation counter input gate	Filter frequency overshoot counter for the Gate input
0xA0n0:16	Filter violation counter	Filter frequency overshoot counter for the encoder input signals with activated filter

The internal error counters can be reset as follows:

- Terminal transition from "PREOP" to "OP" status

or

- Enter the following in the command object 0xFB00:01 "Request"

0xFB00:01 "Request"	Description
0x9152	Sets the internal error counter for 0xA000:14 "Filter violation counter extern latch" for channel 1 to zero
0x9153	Sets the internal error counter for 0xA000:15 "Filter violation counter input gate" for channel 1 to zero
0x9154	Sets the internal error counter for 0xA000:16 "Filter violation counter" for channel 1 to zero
0x9162	Sets the internal error counter for 0xA010:14 "Filter violation counter extern latch" for channel 2 to zero
0x9163	Sets the internal error counter for 0xA010:15 "Filter violation counter input gate" for channel 2 to zero
0x9164	Sets the internal error counter for 0xA010:16 "Filter violation counter" for channel 2 to zero

NOTICE

Fast digital inputs – interference from interfering devices

Please note that the input wiring has very little filtering. It has been optimized for fast signal transmission from the input to the evaluation unit. In other words, rapid level changes/pulses in the μs range and/or high-frequency interference signals from devices (e.g. proportional valves, stepper motor or DC motor output stages) arrive at the evaluation unit almost unfiltered/unattenuated. These interferences can be incorrectly detected as a signal.

- To suppress interference, an additional input filter can be parameterized.
- Furthermore, EMC-compliant cabling and the use of separate power supply units for the terminal and the devices causing interference are recommended.

4.1.4.8 Plausibility check

The plausibility check of the input signals serves as an extended diagnosis to detect interference signals and to identify and suppress the step changes in the counter value caused by them.

Functional principle of the plausibility check

The square wave signals of an incremental encoder with track A and B are phase-shifted by 90°. This means that only certain transitions in the signal curve are permitted or “plausible”, e.g. with a rising A-edge the signal on track B cannot also rise.

The plausibility of the signal sequence is checked in the terminal. If invalid signal transitions occur, these are detected and displayed accordingly if plausibility detection is activated.

Plausibility check sequence

- The plausibility check can be enabled via index 0x80n0:21 “Enable encoder plausibility check”
- If a plausibility error is detected, it is displayed as follows:

Error diagnosis	Description
DiagMessage, type “Error”, text ID 0x8312	Encoder plausibility error (channel n)
0xA0n0:13 “Encoder plausibility error counter”	The error counter is incremented when a plausibility error is detected.
0x60n2:0E TxPDO State = 1	The associated TxPDO data are not valid.

The plausibility error counter can be reset as follows:

- Transition from PREOP to OP

or

- Enter the following in the command object in Index 0xFB00:01 “Request”

0xFB00:01 “Request”	Description
0x9151	Sets the internal error counter 0xA000:13 “Encoder plausibility error counter” for channel 1 to zero
0x9161	Sets the internal error counter 0xA010:13 “Encoder plausibility error counter” for channel 2 to zero

4.1.5 Inputs in single-channel mode

Input functions in 1-channel mode

The number of available inputs depends on the operation mode.

The table provides a brief overview of the input functions in 1-channel mode.

Please refer to the detailed function descriptions in the respective chapters.

1-channel mode: 1 x ABC				
Counter value	PLC variable	Zero pulse C [► 91]	Latch input [► 93]	Gate input [► 94]
Set [► 68]	Enable setting: Output process data "Set counter" (0x7000:03) = TRUE to the value: Output process data "Set counter value" (0x7000:11)	Enable setting: Output process data "Set counter on latch C" (0x7000:08) = TRUE to the value: Process data "Set counter value" (0x7000:11)	Enable setting: Output process data "Set counter on latch extern on positive/negative edge" (0x7000:0A/0B) = TRUE to the value: Output process data "Set counter value" (0x7000:11)	–
Reset [► 67]	–	Enable resetting: 0x8000:01 "Enable C reset" to the value: 0x8001:1B "Reset counter value"	Enable resetting: 0x8000:02 "Enable extern reset" to the value: 0x8001:1B "Reset counter value"	–
Save [► 72]	–	Enable saving: Output process data "Enable latch C" (0x7000:01) = TRUE Save the current counter value in the input process data: "Latch value" (0x6000:12)	Enable saving: Output process data "Enable latch extern on positive/negative edge" (0x7000:02/04) = TRUE Save the current counter value in the input process data: "Latch value" (0x6000:12)	Enable saving via latch 2 input: Output process data "Enable latch extern 2 on positive/negative edge" (0x7000:0C/0D) = TRUE Save the current counter value in the input process data: "Latch value 2" (0x6000:22)
Lock [► 76]	Lock: Output process data "Set software gate" (0x7000:09) = TRUE	–	–	Enable locking with HIGH level: 0x8000:04 "Gate polarity" = 1 with LOW level: 0x8000:04 "Gate polarity" = 2

4.1.5.1 Zero pulse C input

With incremental encoders, a full revolution is marked by a special marker, the zero pulse C. This pulse can be used in the terminal as follows:

- **Counter value reset:** [► 91] The counter value is reset to the value specified in Index 0x80n1:1B [► 151] "Reset counter value" (default setting: "0") (index 80n0:01 "Enable C reset")
- **Set counter value:** [► 91] the counter value is set to a predefined value (output process data "Set counter on latch C")
- **Save counter value:** [► 92] the counter value is saved in the latch register (output process data "Enable latch C")

The "Status of input C" input process data 0x60n0:0B [► 153] displays the current level at the zero pulse C input.

● Status of input C

i Zero pulse C has only a short pulse duration, depending on the rotational speed. Due to the cyclic request, it is possible that the HIGH level of the zero pulse is not transferred congruently into the process data "Status of input C" (0x60n0:0B [► 153]).

Counter value reset via the zero pulse C input (Enable C reset)

The counter value can be set to the value specified in index 0x80n1:1B [► 151] "Reset counter value" for every full revolution of the encoder via the zero pulse C.

- Presetting of the reset value via index 0x80n1:1B [► 151] "Reset counter value" (Default: 0)
- To activate this function set the bit in index 0x80n0:01 [► 150] "Enable C reset".
- There is no status message via the process data.

Set counter value via input zero pulse C (Set counter on latch C)

The counter value can be set to a preset value during runtime via the process data by means of the zero pulse C.

- Setting the counter value using the process data "Set counter value" (0x70n0:11 [► 155])
- Activation of the counter value setting via zero pulse C:
 - Process data "Set counter on latch C" (0x70n0:08 [► 155]) = TRUE
At the next zero pulse, the counter value (Counter value) is set to the counter value specified in the process data "Set counter value" (0x70n0:11 [► 155]).
- To confirm, the bit in the process data "Set counter done" (0x60n0:03) is set to TRUE.
- The count value preset can only be reactivated via the zero pulse C once the bit in the process data "Set counter on latch C" (0x70n0:08) has been set to FALSE.

● Multiple activation of "Set counter on ..."

i If several commands are activated to accept the preset counter value, only the command that is set first is accepted by the terminal. All other commands are ignored but remain activated, depending on the system.

- The counter value is set to the preset counter value at the first activated event and confirmed by the bit in process data "Set counter done" (0x60n0:03 [► 152]).
- The counter value specification cannot be reactivated until all activated commands for the transfer of the counter value have been deactivated. This is confirmed by setting the bit in process data "Set counter done" (0x60n0:03) to FALSE.

Save counter value via the zero pulse C input (Enable latch C)

The counter value can be stored at runtime via the process data and the zero pulse in “Latch value” (0x60n0:12 [► 152]).

- The function is activated by setting the bit in process data “Enable latch C” (0x70n0:01) [► 155] to TRUE.
- The current counter value is saved in the process data “Latch value” (0x60n0:12) with the next zero pulse at input C. The subsequent pulses have no influence on the latch value.
- The bit in process data “Latch C valid” (0x60n0:01 [► 152]) is set to TRUE.
- After reactivating the process data “Enable latch C” (0x70n0:01) a new counter value cannot be written to the Latch input until the values of the “Enable latch C” bit (0x70n0:01) and the “Latch C valid” bit (0x60n0:01) are FALSE.

i Multiple activation of the latch function

If several commands are activated simultaneously to save the counter value in the “Latch value” process data (0x60n0:12 [► 152]), only the command that is set first is accepted by the terminal.

- The counter value is stored in the process data “Latch value” (0x60n0:12) at the next occurring event and confirmed with the corresponding bit.
 - All other activated events are ignored.
 - The counter value storage cannot be reactivated until all activated commands for latching the value have been deactivated. This also applies if they were activated after confirmation by the occurring event.
-

4.1.5.2 Latch input (Latch extern)

A latch input (Latch extern) for 24 V DC signals with a minimum pulse duration of $t_{ON} > 1 \mu s$ is available and can be used as follows:

- **Reset counter value [► 93]:**
Reset the counter to the value set in index 0x80n1:1B "Reset counter value" (default setting: "0") (index 0x80n0:02 "Enable extern reset")
- **Set counter value [► 93]:**
Set the counter value to a predefined counter value via a positive or negative edge (output process data "Set counter on latch extern on positive/negative edge" (0x70n0:0A/0B))
- **Save counter value [► 94]:**
Save the counter value, in separate process data, via a positive or negative edge (output process data "Enable latch extern on positive/negative edge" (0x70n0:02/04))

Counter value reset via the "Latch extern" input (Enable extern reset)

The counter value can be set to "0" via the "Latch extern" input.

- Setting the reset value via index 0x80n1:1B [► 151] "Reset counter value" (default: 0)
- To activate this function set the bit in index 0x80n0:02 [► 150] "Enable extern reset".
- Index 0x80n0:10 [► 150] "Extern reset polarity" can be used to specify at which edge the "Latch extern" input is active.
 - 0: "Fall" - the counter is set to "0" with a negative edge
 - 1: "Rise" - the counter is set to "0" with a positive edge

There is no status message via the process data.

Set counter via the "Latch extern" input (Set counter on latch extern on positive/negative edge)

The counter value can be set to a preset value during runtime via the process data by the positive or negative edge at the "Latch extern" input.

- Setting the counter value via the process data "Set counter value" (0x70n0:11)
- Activation of the counter value setting via
 - the positive edge at the "Latch extern" input:
Process data "Set counter on latch extern on positive edge" (0x70n0:0A)
 - the negative edge at the "Latch extern" input:
Process data "Set counter on latch extern on negative edge" (0x70n0:0B)
- If the bit is set (TRUE) in the process data "Set counter on latch extern on positive edge" (0x70n0:0A) or "Set counter on latch extern on negative edge" (0x70n0:0B), the counter value (Counter value) is set to the value specified in the process data "Set counter value" at the next positive or negative edge at the Latch extern input.
- To confirm, the bit in the process data "Set counter done" (0x60n0:03) is set to TRUE.
- The counter value setting cannot be reactivated until the process data "Set counter on latch extern on positive/negative edge" (0x70n0:0A/0B) has been set to FALSE.

Save the counter value via a positive/negative edge at the latch input (Enable latch extern on positive/negative edge)

- The counter value at the “Latch extern” input can be saved via:
 - Process data “Enable latch extern on positive edge” (0x70n0:02 [► 155]) = TRUE
At the first external latch pulse with positive edge, the current counter value is stored in the process data “Latch value” (0x60n0:12 [► 152]).
 - Process data “Enable latch extern on negative edge” (0x70n0:04 [► 155]) = TRUE
At the first external latch pulse with negative edge the current counter value is stored in the process data “Latch value” (0x60n0:12 [► 152]).
 - Simultaneous activation of the bits in the process data “Enable latch extern on positive edge” (0x70n0:02) and “Enable latch extern on negative edge” (0x70n0:04)
The current counter value is stored in the process data “Latch value” (0x60n0:12), at the first external latch pulse, independent of the edge polarity.
- Specification whether it is necessary to reactivate the command to save the counter value via:
 - “Enable continuous latch extern” Index 0x80n0:22 [► 150] = FALSE
The following pulses at the “Latch extern” input have no effect on the latch value in the process data “Enable latch extern on positive edge” (0x70n0:02) and “Enable latch extern on negative edge” (0x70n0:04) when the bit in the process data “Latch value” (0x60n0:12) is set.
Only when the bit in the process data “Latch extern valid” (0x60n0:02 [► 152]) is set to FALSE can a new counter value be written to the latch input in the process data “Latch value” (0x60n0:12)
 - “Enable continuous latch extern” Index 0x80n0:22 [► 150] = TRUE
The counter value is written to the process data “Latch value” (0x60n0:12) each time a configured edge occurs at the “Latch extern” input.
There is no need to reactivate the process data “Enable latch extern on positive edge” (0x70n0:02) and “Enable latch extern on negative edge” (0x70n0:04).
- Saving of the count value in the process data “Latch value” (0x60n0:12) is confirmed by the bit in the process data “Latch extern valid” (0x60n0:02).
- The status of the “Latch extern” input can be monitored using the process data “Status of extern latch” (0x60n2:14 [► 154]).

4.1.5.3 Gate input

An external input, “Gate”, for 24 V DC signals with a minimum pulse duration of $t_{ON} > 1 \mu s$ is available and can be used as follows:

- Lock counter value: [► 94]
Lock the counter value via a positive or negative edge (index 0x80n0:04 “Gate polarity” = “Enable pos/neg. gate”)
- Save counter value: [► 95]
Save the counter value, in separate process data, via a positive or negative edge (output process data “Enable latch extern 2 on positive/negative edge” (0x70n0:0C/0D))

Lock counter value via a positive/negative edge at the gate input (Enable pos./neg. gate)

- The level at the gate input at which the counter value is locked during runtime can be specified via index 0x80n0:04 [► 150] “Gate polarity”.
 - 0: Disable gate
The “Gate” input is disabled. It can still be used as “Latch extern 2” input.
 - 1: Enable pos. gate
The counter value is locked with a HIGH level at the “Gate” input.
 - 2: Enable neg. gate
The counter value is locked with LOW level at the “Gate” input.
- The current level at the “Gate” input is displayed via process data “Status of input gate” (0x60n0:0C [► 152]).

Save the counter value via a positive/negative edge on the “Gate” input (Enable latch extern 2 on positive/negative edge)

The “Gate” input may be used as a second latch input (Latch extern 2). To do this, the gate should be disabled.

● Deactivation of the gate

i Set the “Gate polarity” bit (index 0x80n0:04 [► 150]) to “0 – Disable gate” in order to be able to use the “Latch extern 2” input without locking the counter value after the latch event.

- The counter value at the “Latch extern 2” input can be saved via:
 - Process data “Enable latch extern 2 on positive edge” (0x70n0:0C [► 155]) = TRUE
At the first external pulse with positive edge at the “Gate” input, the current counter value is stored in the process data “Latch value 2” (0x60n0:22 [► 152]).
 - Process data “Enable latch extern 2 on negative edge” (0x70n0:0D [► 155]) = TRUE
At the first external pulse with negative edge at the “Gate” input, the current counter value is stored in the process data “Latch value 2” (0x60n0:22).
 - Simultaneous activation of the bits in the process data “Enable latch extern 2 on positive edge” (0x70n0:0C) and “Enable latch extern 2 on negative edge” (0x70n0:0D)
When the first pulse is received at the “Gate” input—regardless of the polarity of the edge—the current counter value is stored in the process data “Latch value 2” (0x60n0:22).
- Specification whether it is necessary to reactivate the command to save the counter value via:
 - “Enable continuous latch extern 2” Index 0x80n0:23 [► 150] = FALSE
The following pulses at the “Gate” input have no effect on the latch value in the process data “Latch value 2” (0x60n0:22) when the bit in the process data “Enable latch extern 2 on positive edge” (0x70n0:0C) or “Enable latch extern 2 on negative edge” (0x70n0:0D) is set.
Only when the bit in the process data “Latch extern 2 valid” (0x60n2:12 [► 154]) is FALSE can a new counter value be written to the “Gate” input in the process data “Latch value 2” (0x60n0:22).
 - “Enable continuous latch extern 2” Index 0x80n0:23 [► 150] = TRUE
The counter value is written to the process data field “Latch value 2” (0x60n2:22) each time a configured edge is detected at the “Gate” input.
There is no need to reactivate the bits in the process data “Enable latch extern 2 on positive edge” (0x70n0:0C) or “Enable latch extern 2 on negative edge” (0x70n0:0D).
- The status of the input “Gate” can be recorded via the process data “Status of input gate” (0x60n0:0C [► 152]).
- Saving of the counter value in the process data “Latch value 2” (0x60n0:22) is confirmed by the bit in the process data “Latch extern 2 valid” (0x60n2:12).

● Simultaneous use of Gate and Latch extern 2

i When using the index 0x80n0:04 [► 150] “Gate polarity” (1 = “Enable pos. gate”) and simultaneous activation of the output process data “Enable latch extern 2 on positive edge” (0x70n0:0C [► 155]), a positive edge on the “Gate” input first stores the current counter value in the input process data “Latch value 2” (0x60n0:22 [► 152]). After that, the counter value is locked.

The same applies to the use of index 0x80n0:04 “Gate polarity” (2 = “Enable neg. gate”) and the simultaneous activation of the output process data “Enable latch extern 2 on negative edge” (0x70n0:0D [► 155]) when a negative edge occurs at the “Gate” input.

● Multiple activation of the latch function

i If several commands are activated simultaneously to save the counter value in the “Latch value” process data (0x60n0:12 [► 152]), only the command that is set first is accepted by the terminal.

- The counter value is stored in the process data “Latch value” (0x60n0:12) at the next occurring event and confirmed with the corresponding bit.
- All other activated events are ignored.
- The counter value storage cannot be reactivated until all activated commands for latching the value have been deactivated. This also applies if they were activated after confirmation by the occurring event.

4.1.5.4 Input “Digital input”

If the encoder has an alarm or status output, in 1-channel mode this can be connected to the “Digital input” of the terminal and evaluated. The input is 5 V compatible.

The alarm or status output at the encoder is usually implemented with negative logic. This is indicated by the terminal as follows:

Encoder	ED5112 (1-channel mode)		
Alarm output	“Digital input” (0x60n0:06 “Status of input status”)	LED “Ch. 1 DI”	Meaning
HIGH level / output open	TRUE	off	e.g. encoder OK
LOW level / PullDown - level is actively pulled down to LOW	FALSE	red	e.g. encoder malfunction

If an overvoltage is present at the “Digital input” input, it is displayed as follows:

Fault diagnosis in case of overvoltage at the “Digital input” at channel n	Display
DiagMessage, type “Error”, text ID 0x8315	Error status input (channel n)
0xA0n0:05 “Error input status”	TRUE
LED: Ch. 1 DI	red

NOTICE

Wiring of the input “Digital input”

In the terminal the input “Digital input” is internally connected to 5 V via a pull-up resistor (1 kΩ). The encoder output must actively pull the signal against GND. The resistance must be dimensioned so that it is less than 120 Ω.

External power supply is not recommended. If an external supply is used, the maximum permitted voltage is 5 V against GND.

4.2 2-channel mode

4.2.1 Overview of functions

The terminal ED5112 offers a wide range of functions. The following table provides an overview of the functions provided in 2-channel mode. A detailed description can be found in the individual chapters.

To use the extended functions, the corresponding functions must be selected via the “Predefined PDO Assignment”. The assignment is described in chapter “[Process data](#) [\[► 105\]](#)”.

Basic functions	Description
Selection of encoder type [► 109]	Encoders or counters/pulse generators with signal levels according to RS422, TTL or Open Collector can be selected.
Encoder operating voltage [► 110]	The encoder supply is set centrally for both channels either to 5 V DC, 12 V DC or 24 V DC.
Evaluation of the counter value [► 110]	The input signal can be subject to 4-fold, 2-fold or 1-fold evaluation.
Counter limits [► 111]	The value range within which counting takes place can be defined.
Counter overflow / counter underflow [► 112]	If the count limit is exceeded or underrun, this is indicated in separate process data.
Counting direction [► 113]	The counting direction can be adapted to the application.
Reset counter value [► 115]	Allows a recurring reset of the counter value via an edge (positive/negative) at the gate/latch combination input.
Set counter value [► 116]	The counter value can be set at runtime to a predefined counter value via a PLC variable or an edge (positive/negative) at the gate/latch combination input.
Save counter value [► 118]	The current counter value can be stored, independent of the cycle time, in separate process data via an edge (positive/negative) at the gate/latch combination input. You can parameterize whether the function is executed at each external edge or only once after each activation.
Lock counter value [► 120]	The counter value can be locked via an edge (positive/negative) at the gate/latch combination input or a PLC variable.

Extended functionalities	Description
Frequency measurement [► 121]	The average frequency of the input signal within a given timeframe can be output directly.
Period value measurement [► 123]	The period value of the last period within the PLC cycle can be output directly.
Velocity, speed calculation [► 124]	The average velocity or speed of the input signal within a specified timeframe can be output directly.
Adjustable interference pulse filters [► 126]	To suppress interference, a filter can be set for each of the input signals.
Diagnostic data [► 132]	Error messages are communicated to the EtherCAT Master/TwinCAT via “DiagMessages”.

Process data	Description
Operation modes [► 105]	The scope of the process data can be selected via “Predefined PDO Assignment”.
Synchronicity mode [► 107]	In addition to the frame-triggered operation mode (SM mode), a mode based on synchronization via the distributed clocks is available.

Description of the inputs	Description
Gate/Latch combination input [► 130]	One gate/latch combination input is provided per channel for 24 V DC signals with a minimum pulse duration of $t_{ON} > 1 \mu s$. This can be used for resetting, setting and storing the counter value.

4.2.2 Process data for two-channel mode

4.2.2.1 Sync Manager (SM)

For a detailed description of how to configure the process data, see the “[EtherCAT device configuration](#)” chapter in the EtherCAT System Manual.

● Process data can be read via CoE but cannot be set.

I In the following descriptions, the corresponding CoE index is always included as a reference in addition to the name of the process data.

- Please note that while the input and output process data (0x6xxx/0x7xxx) can be read via the CoE directory, they cannot be set via the CoE directory!

The scope of process data offered can be modified via the “Process Data” tab (see Fig. *Process Data tab SM3, ED5112 (default)* below).

Sync Manager:

SM	Size	Type	Flags
0	256	MbxOut	
1	256	MbxIn	
2	6	Outputs	
3	16	Inputs	

PDO List:

Index	Size	Name	Flags	SM	SU
0x1A00	16.0	ENC Status Channel 1	F	3	0
0x1A01	10.0	ENC Status Compact Channel 1	F		0
0x1A02	12.0	ENC Status Channel 1	F		0
0x1A03	8.0	ENC Status Compact Channel 1	F		0
0x1A04	8.0	ENC Status Counter Channel 1	F		0
0x1A05	6.0	ENC Status Compact Counter Channel 1	F		0
0x1A06	10.0	ENC Status Legacy Channel 1	F		0
0x1A07	6.0	ENC Status Compact Legacy Channel 1	F		0
0x1A08	4.0	ENC Frequency Channel 1	F		0
0x1A09	2.0	ENC Frequency Compact Channel 1	F		0
0x1A0A	4.0	ENC Period Channel 1	F		0
0x1A0B	2.0	ENC Period Compact Channel 1	F		0
0x1A0C	6.0	ENC Duty Cycle Channel 1	F		0
0x1A0D	32.0	ENC Timestamp Channel 1	F		0
0x1A0E	16.0	ENC Timestamp Compact Channel 1	F		0
0x1A11	12.0	ENC Status Channel 2	F		0

PDO Assignment (0x1C13):

☒	0x1A00
☐	0x1A01 (excluded by 0x1A00)
☐	0x1A02 (excluded by 0x1A00)
☐	0x1A03 (excluded by 0x1A00)
☐	0x1A04 (excluded by 0x1A00)
☐	0x1A05 (excluded by 0x1A00)
☐	0x1A06 (excluded by 0x1A00)
☐	0x1A07 (excluded by 0x1A00)
☐	0x1A08
☐	0x1A09
☐	0x1A0A
☐	0x1A0B
☐	0x1A0C
☐	0x1A0D
☐	0x1A0E
☐	0x1A11 (excluded by 0x1A00)
☐	0x1A12 (excluded by 0x1A00)
☐	0x1A13 (excluded by 0x1A00)
☐	0x1A14 (excluded by 0x1A00)
☐	0x1A17 (excluded by 0x1A00)
☐	0x1A18 (excluded by 0x1A00)
☐	0x1A19 (excluded by 0x1A00)
☐	0x1A1A (excluded by 0x1A00)

PDO Content (0x1A00):

Index	Size	Offs	Name	Type	Default (hex)
0x6000:01	0.1	0.0	Status__Latch C valid	BIT	
0x6000:02	0.1	0.1	Status__Latch exten valid	BIT	
0x6000:03	0.1	0.2	Status__Set counter done	BIT	
0x6000:04	0.1	0.3	Status__Counter underflow	BIT	
0x6000:05	0.1	0.4	Status__Counter overflow	BIT	
0x6000:06	0.1	0.5	Status__Status of input status	BIT	
0x6000:07	0.1	0.6	Status__Open circuit	BIT	
0x6000:08	0.1	0.7	Status__Extrapolation stall	BIT	
0x6000:09	0.1	1.0	Status__Status of input A	BIT	
0x6000:0A	0.1	1.1	Status__Status of input B	BIT	
0x6000:0B	0.1	1.2	Status__Status of input C	BIT	
0x6000:0C	0.1	1.3	Status__Status of input gate	BIT	
0x6002:0D	0.1	1.4	Status__Diag	BIT	
0x6002:0E	0.1	1.5	Status__TxPDO State	BIT	
0x6002:0F	0.2	1.6	Status__Input cycle counter	BIT2	
0x6002:11	0.1	2.0	Status__Software gate valid	BIT	
0x6002:12	0.1	2.1	Status__Latch exten 2 valid	BIT	
0x6002:13	0.1	2.2	Status__Direction inversion detec...	BIT	

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☒ PDO Assignment

☐ PDO Configuration

Predefined PDO Assignment: "1.Ch Standard, 1xABC"

Load PDO info from device

Sync Unit Assignment...

Fig. 46: ED5112 - Process data tab SM3 (default)

4.2.2.2 PDO assignment in two-channel mode

A wide range of functions and, consequently, a wide range of process data is available.

4.2.2.2.1 SM3 - Inputs (0x1A00...0x1A1A)

Channel 1 (0x1A02...0x1A0E):

0x1A02 - ENC Status Channel 1 (12.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x6000:02 [153] - Status_Latch extern valid (0.1)	0x1A00 [170] - ENC Status Channel 1 (16.0)
0x6000:03 [153] - Status_Set counter done (0.1)	0x1A01 [171] - ENC Status Compact Channel 1 (10.0)
0x6000:04 [153] - Status_Counter underflow (0.1)	0x1A03 [173] - ENC Status Compact Channel 1 (8.0)
0x6000:05 [153] - Status_Counter overflow (0.1)	0x1A04 [173] - ENC Status Counter Channel 1 (8.0)
0x6000:07 [153] - Status_Open circuit (0.1)	0x1A05 [174] - ENC Status Compact Counter Channel 1 (6.0)
0x6000:09 [153] - Status_Status of input A (0.1)	0x1A06 [174] - ENC Status Legacy Channel 1 (10.0)
0x6000:0A [153] - Status_Status of input B (0.1)	0x1A07 [175] - ENC Status Compact Legacy Channel 1 (6.0)
0x6000:0C [153] - Status_Status of input gate (0.1)	
0x6002:0D [154] - Status_Diag (0.1)	
0x6002:0E [154] - Status_TxPDO State (0.1)	
0x6002:0F [154] - Status_Input cycle counter (0.2)	
0x6002:11 [154] - Status_Software gate valid (0.1)	
0x6002:15 [154] - Status_Counter value out of range (0.1)	
0x6000:11 [153] - Counter value (4.0)	
0x6000:12 [153] - Latch value (4.0)	

0x1A03 - ENC Status Compact Channel 1 (8.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index name size (byte.bit)
0x6000:02 [153] - Status_Latch extern valid (0.1)	0x1A00 [170] - ENC Status Channel 1 (16.0)
0x6000:03 [153] - Status_Set counter done (0.1)	0x1A01 [171] - ENC Status Compact Channel 1 (10.0)
0x6000:04 [153] - Status_Counter underflow (0.1)	0x1A02 [172] - ENC Status Channel 1 (12.0)
0x6000:05 [153] - Status_Counter overflow (0.1)	0x1A04 [173] - ENC Status Counter Channel 1 (8.0)
0x6000:07 [153] - Status_Open circuit (0.1)	0x1A05 [174] - ENC Status Compact Counter Channel 1 (6.0)
0x6000:09 [153] - Status_Status of input A (0.1)	0x1A06 [174] - ENC Status Legacy Channel 1 (10.0)
0x6000:0A [153] - Status_Status of input B (0.1)	0x1A07 [175] - ENC Status Compact Legacy Channel 1 (6.0)
0x6000:0C [153] - Status_Status of input gate (0.1)	
0x6002:0D [154] - Status_Diag (0.1)	
0x6002:0E [154] - Status_TxPDO State (0.1)	
0x6002:0F [154] - Status_Input cycle counter (0.2)	
0x6002:11 [154] - Status_Software gate valid (0.1)	
0x6002:15 [154] - Status_Counter value out of range (0.1)	
0x6000:11 [153] - Counter value (2.0)	
0x6000:12 [153] - Latch value (2.0)	

0x1A04 - ENC Status Counter Channel 1 (8.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x6000:03 [153] - Status_Set counter done (0.1)	0x1A00 [170] - ENC Status Channel 1 (16.0)
0x6002:0D [154] - Status_Status Diag (0.1)	0x1A01 [171] - ENC Status Compact Channel 1 (10.0)
0x6002:0E [154] - Status_Status TxPDO State (0.1)	0x1A02 [172] - ENC Status Channel 1 (12.0)
0x6002:0F [154] - Status_Input cycle counter (0.2)	0x1A03 [173] - ENC Status Compact Channel 1 (8.0)
0x6002:11 [154] - Status_Software gate valid (0.1)	0x1A05 [174] - ENC Status Compact Counter Channel 1 (6.0)
0x6000:11 [153] - Counter value (4.0)	0x1A06 [174] - ENC Status Legacy Channel 1 (10.0)
	0x1A07 [175] - ENC Status Compact Legacy Channel 1 (6.0)

0x1A05 - ENC Status Compact Counter Channel 1 (6.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x6000:03 [▶ 153] - Status_Set counter done (0.1)	0x1A00 [▶ 170] - ENC Status Channel 1 (16.0)
0x6002:0D [▶ 154] - Status_Diag (0.1)	0x1A01 [▶ 171] - ENC Status Compact Channel 1 (10.0)
0x6002:0E [▶ 154] - Status_TxPDO State (0.1)	0x1A02 [▶ 172] - ENC Status Channel 1 (12.0)
0x6002:0F [▶ 154] - Status_Input cycle counter (0.2)	0x1A03 [▶ 173] - ENC Status Compact Channel 1 (8.0)
0x6002:11 [▶ 154] - Status_Software gate valid (0.1)	0x1A04 [▶ 173] - ENC Status Counter Channel 1 (8.0)
0x6000:11 [▶ 153] - Counter value (2.0)	0x1A06 [▶ 174] - ENC Status Legacy Channel 1 (10.0)
	0x1A07 [▶ 175] - ENC Status Compact Legacy Channel 1 (6.0)

0x1A08 - ENC Frequency Channel 1 (4.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index name size (byte.bit)
0x6000:13 [▶ 153] - Frequency value (4.0)	0x1A09 [▶ 175] - ENC Frequency Compact Channel 1 (2.0)

0x1A09 - ENC Frequency Compact Channel 1 (2.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index name size (byte.bit)
0x6000:13 [▶ 153] - Frequency value (2.0)	0x1A08 [▶ 175] - ENC Frequency Channel 1 (4.0)

0x1A0A - ENC Period Channel 1 (4.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index name size (byte.bit)
0x6000:14 [▶ 153] - Period value (4.0)	0x1A0B [▶ 176] - ENC Period Compact Channel 1 (2.0)

0x1A0B - ENC Period Compact Channel 1 (2.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index name size (byte.bit)
0x6000:14 [▶ 153] - Period value (2.0)	0x1A0A [▶ 175] - ENC Period Channel 1 (4.0)

0x1A0C - ENC Duty Cycle Channel 1 (6.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index name size (byte.bit)
0x6000:23 [▶ 153] - Duty cycle (2.0)	-
0x6000:24 [▶ 153] - Duty cycle min (2.0)	
0x6000:25 [▶ 153] - Duty cycle max (2.0)	

0x1A0D - ENC Timestamp Channel 1 (32.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x6000:16 [▶ 153] - Timestamp (8.0)	0x1A0E [▶ 176] - ENC Timestamp Compact Channel 1 (16)
0x6000:1F [▶ 153] - Timestamp C (8.0)	
0x6000:20 [▶ 153] - Timestamp latch (8.0)	
0x6000:21 [▶ 153] - Timestamp latch 2 (8.0)	

0x1A0E - ENC Timestamp Compact Channel 1 (16.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x6000:16 [▶ 153] - Timestamp (4.0)	0x1A0D [▶ 176] - ENC Timestamp Channel 1 (32.0)
0x6000:1F [▶ 153] - Timestamp C (4.0)	
0x6000:20 [▶ 153] - Timestamp latch (4.0)	
0x6000:21 [▶ 153] - Timestamp latch 2 (4.0)	

Channel 2 (0x1A11 .. 0x1A1A):

0x1A11 - ENC Status Channel 2 (12.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x6010:02 [▶ 153] - Status_Latch extern valid (0.1)	0x1A12 [▶ 178] - ENC Status Compact Channel 2 (8.0)
0x6010:03 [▶ 153] - Status_Set counter done (0.1)	0x1A13 [▶ 178] - ENC Status Counter Channel 2 (8.0)
0x6010:04 [▶ 153] - Status_Counter underflow (0.1)	0x1A14 [▶ 179] - ENC Status Compact Counter Channel 2 (6.0)
0x6010:05 [▶ 153] - Status_Counter overflow (0.1)	
0x6010:07 [▶ 153] - Status_Open circuit (0.1)	
0x6010:09 [▶ 153] - Status_Status of input A (0.1)	
0x6010:0A [▶ 153] - Status_Status of input B (0.1)	
0x6010:0C [▶ 153] - Status_Status of input gate (0.1)	
0x6012:0D [▶ 154] - Status_Diag (0.1)	
0x6012:0E [▶ 154] - Status_TxPDO State (0.1)	
0x6012:0F [▶ 154] - Status_Input cycle counter (0.2)	
0x6012:11 [▶ 154] - Status_Software gate valid (0.1)	
0x6012:15 [▶ 154] - Status_Counter value out of range (0.1)	
0x6010:11 [▶ 153] - Counter value (4.0)	
0x6010:12 [▶ 153] - Latch value (4.0)	

0x1A12 - ENC Status Compact Channel 2 (8.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x6010:02 [▶ 153] - Status_Latch extern valid (0.1)	0x1A11 [▶ 177] - ENC Status Channel 2 (12.0)
0x6010:03 [▶ 153] - Status_Set counter done (0.1)	0x1A13 [▶ 178] - ENC Status Counter Channel 2 (8.0)
0x6010:04 [▶ 153] - Status_Counter underflow (0.1)	0x1A14 [▶ 179] - ENC Status Compact Counter Channel 2 (6.0)
0x6010:05 [▶ 153] - Status_Counter overflow (0.1)	
0x6010:07 [▶ 153] - Status_Open circuit (0.1)	
0x6010:09 [▶ 153] - Status_Status of input A (0.1)	
0x6010:0A [▶ 153] - Status_Status of input B (0.1)	
0x6010:0C [▶ 153] - Status_Status of input gate (0.1)	
0x6012:0D [▶ 154] - Status_Diag (0.1)	
0x6012:0E [▶ 154] - Status_TxPDO State (0.1)	
0x6012:0F [▶ 154] - Status_Input cycle counter (0.2)	
0x6012:11 [▶ 154] - Status_Software gate valid (0.1)	
0x6012:15 [▶ 154] - Status_Counter value out of range (0.1)	
0x6010:11 [▶ 153] - Counter value (2.0)	
0x6010:12 [▶ 153] - Latch value (2.0)	

0x1A13 - ENC Status Counter Channel 2 (8.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index name size (byte.bit)
0x6010:03 [▶ 153] - Status_Set counter done (0.1)	0x1A11 [▶ 177] - ENC Status Channel 2 (12.0)
0x6012:0D [▶ 154] - Status_Diag (0.1)	0x1A12 [▶ 178] - ENC Status Compact Channel 2 (8.0)
0x6012:0E [▶ 154] - Status_TxPDO State (0.1)	0x1A14 [▶ 179] - ENC Status Compact Counter Channel 2 (6.0)
0x6012:0F [▶ 154] - Status_Input cycle counter (0.2)	
0x6012:11 [▶ 154] - Status_Software gate valid (0.1)	
0x6010:11 [▶ 153] - Counter value (4.0)	

0x1A14 - ENC Status Compact Counter Channel 2 (6.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index name size (byte.bit)
0x6010:03 [▶ 153] - Status_Set counter done (0.1)	0x1A11 [▶ 177] - ENC Status Channel 2 (12.0)
0x6012:0D [▶ 154] - Status_Diag (0.1)	0x1A12 [▶ 178] - ENC Status Compact Channel 2 (8.0)
0x6012:0E [▶ 154] - Status_TxPDO State (0.1)	0x1A13 [▶ 178] - ENC Status Counter Channel 2 (8.0)
0x6012:0F [▶ 154] - Status_Input cycle counter (0.2)	
0x6012:11 [▶ 154] - Status_Software gate valid (0.1)	
0x6010:11 [▶ 153] - Counter value (2.0)	

0x1A17 - ENC Frequency Channel 2 (4.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index name size (byte.bit)
0x6010:13 [► 153] - Frequency value (4.0)	0x1A18 [► 179] - ENC Frequency Compact Channel 2 (2.0)

0x1A18 - ENC Frequency Compact Channel 2 (2.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index name size (byte.bit)
0x6010:13 [► 153] - Frequency value (2.0)	0x1A17 [► 179] - ENC Frequency Channel 2 (4.0)

0x1A19 - ENC Period Channel 2 (4.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index name size (byte.bit)
0x6010:14 [► 153] - Period value (4.0)	0x1A1A [► 179] - ENC Period Compact Channel 2 (2.0)

0x1A1A - ENC Period Compact Channel 2 (2.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index name size (byte.bit)
0x6010:14 [► 153] - Period value (2.0)	0x1A19 [► 179] - ENC Period Channel 2 (4.0)

4.2.2.2 SM2 - Outputs (0x1600 .. 0x160D)

Channel 1 (0x1600 .. 0x1605):

0x1600 - ENC Control Channel 1 (6.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7000:01 [► 155] - Control_Enable latch C (0.1)	0x1601 [► 161] - ENC Control Compact Channel 1 (4.0)
0x7000:02 [► 155] - Control_Enable latch extern on positive edge (0.1)	0x1602 [► 162] - ENC Control Channel 1 (6.0)
0x7000:03 [► 155] - Control_Set counter (0.1)	0x1603 [► 162] - ENC Control Compact Channel 1 (4.0)
0x7000:04 [► 155] - Control_Enable latch extern on negative edge (0.1)	0x1604 [► 162] - ENC Control Counter Channel 1 (6.0)
0x7000:08 [► 155] - Control_Set counter on latch C (0.1)	0x1605 [► 163] - ENC Control Compact Counter Channel 1 (4.0)
0x7000:09 [► 155] - Control_Set software gate (0.1)	0x1606 [► 163] - ENC Control Legacy Channel 1 (6.0)
0x7000:0A [► 155] - Control_Set counter on latch extern on positive edge (0.1)	0x1607 [► 163] - ENC Control Compact Legacy Channel 1 (4.0)
0x7000:0B [► 155] - Control_Set counter on latch extern on negative edge (0.1)	
0x7000:0C [► 155] - Control_Enable latch extern 2 on positive edge (0.1)	
0x7000:0D [► 155] - Control_Enable latch extern 2 on negative edge (0.1)	
0x7000:11 [► 155] - Set counter value (4.0)	

0x1601 - ENC Control Compact Channel 1 (4.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7000:01 [► 155] - Control_Enable latch C (0.1)	0x1600 [► 161] - ENC Control Channel 1 (6.0)
0x7000:02 [► 155] - Control_Enable latch extern on positive edge (0.1)	0x1602 [► 162] - ENC Control Channel 1 (6.0)
0x7000:03 [► 155] - Control_Set counter (0.1)	0x1603 [► 162] - ENC Control Compact Channel 1 (4.0)
0x7000:04 [► 155] - Control_Enable latch extern on negative edge (0.1)	0x1604 [► 162] - ENC Control Counter Channel 1 (6.0)
0x7000:08 [► 155] - Control_Set counter on latch C (0.1)	0x1605 [► 163] - ENC Control Compact Counter Channel 1 (4.0)
0x7000:09 [► 155] - Control_Set software gate (0.1)	0x1606 [► 163] - ENC Control Legacy Channel 1 (6.0)
0x7000:0A [► 155] - Control_Set counter on latch extern on positive edge (0.1)	0x1607 [► 163] - ENC Control Compact Legacy Channel 1 (4.0)
0x7000:0B [► 155] - Control_Set counter on latch extern on negative edge (0.1)	
0x7000:0C [► 155] - Control_Enable latch extern 2 on positive edge (0.1)	
0x7000:0D [► 155] - Control_Enable latch extern 2 on negative edge (0.1)	
0x7000:11 [► 155] - Set counter value (2.0)	

0x1602 - ENC Control Channel 1 (6.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7000:02 [P 155] - Control_Enable latch extern on positive edge (0.1)	0x1600 [P 161] - ENC Control Channel 1 (6.0)
0x7000:03 [P 155] - Control_Set counter (0.1)	0x1601 [P 161] - ENC Control Compact Channel 1 (4.0)
0x7000:04 [P 155] - Control_Enable latch extern on negative edge (0.1)	0x1603 [P 162] - ENC Control Compact Channel 1 (4.0)
0x7000:09 [P 155] - Control_Set software gate (0.1)	0x1604 [P 162] - ENC Control Counter Channel 1 (6.0)
0x7000:0A [P 155] - Control_Set counter on latch extern on positive edge (0.1)	0x1605 [P 163] - ENC Control Compact Counter Channel 1 (4.0)
0x7000:0B [P 155] - Control_Set counter on latch extern on negative edge (0.1)	0x1606 [P 163] - ENC Control Legacy Channel 1 (6.0)
0x7000:11 [P 155] - Set counter value (4.0)	0x1607 [P 163] - ENC Control Compact Legacy Channel 1 (4.0)

0x1603 - ENC Control Compact Channel 1 (4.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7000:02 [P 155] - Control_Enable latch extern on positive edge (0.1)	0x1600 [P 161] - ENC Control Channel 1 (6.0)
0x7000:03 [P 155] - Control_Set counter (0.1)	0x1601 [P 161] - ENC Control Compact Channel 1 (4.0)
0x7000:04 [P 155] - Control_Enable latch extern on negative edge (0.1)	0x1602 [P 162] - ENC Control Channel 1 (6.0)
0x7000:09 [P 155] - Control_Set software gate (0.1)	0x1604 [P 162] - ENC Control Counter Channel 1 (6.0)
0x7000:0A [P 155] - Control_Set counter on latch extern on positive edge (0.1)	0x1605 [P 163] - ENC Control Compact Counter Channel 1 (4.0)
0x7000:0B [P 155] - Control_Set counter on latch extern on negative edge (0.1)	0x1606 [P 163] - ENC Control Legacy Channel 1 (6.0)
0x7000:11 [P 155] - Set counter value (2.0)	0x1607 [P 163] - ENC Control Compact Legacy Channel 1 (4.0)

0x1604 - ENC Control Counter Channel 1 (6.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7000:03 [P 155] - Control_Set counter (0.1)	0x1600 [P 161] - ENC Control Channel 1 (6.0)
0x7000:09 [P 155] - Control_Set software gate (0.1)	0x1601 [P 161] - ENC Control Compact Channel 1 (4.0)
0x7000:11 [P 155] - Set counter value (4.0)	0x1602 [P 162] - ENC Control Channel 1 (6.0)
	0x1603 [P 162] - ENC Control Compact Channel 1 (4.0)
	0x1605 [P 163] - ENC Control Compact Counter Channel 1 (4.0)
	0x1606 [P 163] - ENC Control Legacy Channel 1 (6.0)
	0x1607 [P 163] - ENC Control Compact Legacy Channel 1 (4.0)

0x1605 - ENC Control Compact Counter Channel 1 (4.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7000:03 [P 155] - Control_Set counter (0.1)	0x1600 [P 161] - ENC Control Channel 1 (6.0)
0x7000:09 [P 155] - Control_Set software gate (0.1)	0x1601 [P 161] - ENC Control Compact Channel 1 (4.0)
0x7000:11 [P 155] - Set counter value (2.0)	0x1602 [P 162] - ENC Control Channel 1 (6.0)
	0x1603 [P 162] - ENC Control Compact Channel 1 (4.0)
	0x1604 [P 162] - ENC Control Counter Channel 1 (6.0)
	0x1606 [P 163] - ENC Control Legacy Channel 1 (6.0)
	0x1607 [P 163] - ENC Control Compact Legacy Channel 1 (4.0)

Channel 2 (0x160A .. 0x160D):

0x160A - ENC Control Channel 2 (6.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7010:02 [▶ 155] - Control_Enable latch extern on positive edge (0.1)	0x160B [▶ 164] - ENC Control Compact Channel 2 (4.0)
0x7010:03 [▶ 155] - Control_Set counter (0.1)	0x160C [▶ 164] - ENC Control Counter Channel 2 (6.0)
0x7010:04 [▶ 155] - Control_Enable latch extern on negative edge (0.1)	0x160D [▶ 165] - ENC Control Compact Counter Channel 2 (4.0)
0x7010:09 [▶ 155] - Control_Set software gate (0.1)	
0x7010:0A [▶ 155] - Control_Set counter on latch extern on positive edge (0.1)	
0x7010:0B [▶ 155] - Control_Set counter on latch extern on negative edge (0.1)	
0x7010:11 [▶ 155] - Set counter value (4.0)	

0x160B - ENC Control Compact Channel 2 (4.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7010:02 [▶ 155] - Control_Enable latch extern on positive edge (0.1)	0x160A [▶ 164] - ENC Control Channel 2 (6.0)
0x7010:03 [▶ 155] - Control_Set counter (0.1)	0x160C [▶ 164] - ENC Control Counter Channel 2 (6.0)
0x7010:04 [▶ 155] - Control_Enable latch extern on negative edge (0.1)	0x160D [▶ 165] - ENC Control Compact Counter Channel 2 (4.0)
0x7010:09 [▶ 155] - Control_Set software gate (0.1)	
0x7010:0A [▶ 155] - Control_Set counter on latch extern on positive edge (0.1)	
0x7010:0B [▶ 155] - Control_Set counter on latch extern on negative edge (0.1)	
0x7010:11 [▶ 155] - Set counter value (2.0)	

0x160C - ENC Control Counter Channel 2 (6.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7010:03 [▶ 155] - Control_Set counter (0.1)	0x160A [▶ 164] - ENC Control Channel 2 (6.0)
0x7010:09 [▶ 155] - Control_Set software gate (0.1)	0x160B [▶ 164] - ENC Control Compact Channel 2 (6.0)
0x7010:11 [▶ 155] - Set counter value (4.0)	0x160D [▶ 165] - ENC Control Compact Counter Channel 2 (4.0)

0x160D - ENC Control Compact Counter Channel 2 (4.0)	
Contents Index - name size (byte.bit)	Excluded PDOs Index - name size (byte.bit)
0x7010:03 [▶ 155] - Control_Set counter (0.1)	0x160A [▶ 164] - ENC Control Channel 2 (6.0)
0x7010:09 [▶ 155] - Control_Set software gate (0.1)	0x160B [▶ 164] - ENC Control Compact Channel 2 (6.0)
0x7010:11 [▶ 155] - Set counter value (2.0)	0x160C [▶ 164] - ENC Control Counter Channel 2 (6.0)

4.2.2.3 Predefined PDO Assignment for two-channel mode

The “Predefined PDO Assignment” enables a simplified selection of the process data. The desired function is selected on the lower part of the Process data tab. As a result, all necessary PDOs are automatically enabled and the unnecessary PDOs are disabled.

General | EtherCAT | DC | Process Data | Startup | CoE - Online | Diag History | Online

Sync Manager:

SM	Size	Type	Flags
0	128	MbxCOut	
1	128	MbxCIn	
2	6	Outputs	
3	16	Inputs	

PDO List:

Index	Size	Name	Flags	SM
0x1A00	16.0	ENC Status Channel 1	F	3
0x1A01	10.0	ENC Status Compact Channel 1	F	
0x1A02	12.0	ENC Status Channel 1	F	
0x1A03	8.0	ENC Status Compact Channel 1	F	
0x1A04	8.0	ENC Status Counter Channel 1	F	
0x1A05	6.0	ENC Status Compact Counter Channel 1	F	
0x1A06	10.0	ENC Status Legacy Channel 1	F	
0x1A07	6.0	ENC Status Compact Legacy Channel 1	F	
0x1A08	4.0	ENC Frequency Channel 1	F	
0x1A09	2.0	ENC Frequency Compact Channel 1	F	
0x1A0A	4.0	ENC Period Channel 1	F	
0x1A0B	2.0	ENC Period Compact Channel 1	F	

PDO Assignment (0x1C12):

☒ 0x1A00
☐ 0x1A01 (excluded by 0x1A00)
☐ 0x1A02 (excluded by 0x1A00)
☐ 0x1A03 (excluded by 0x1A00)
☐ 0x1A04 (excluded by 0x1A00)
☐ 0x1A05 (excluded by 0x1A00)
☐ 0x1A06 (excluded by 0x1A00)
☐ 0x1A07 (excluded by 0x1A00)
☐ 0x1A08
☐ 0x1A09
☐ 0x1A0A
☐ 0x1A0B

Download
☒ PDO Assignment
☐ PDO Configuration

Predefined PDO Assignment: (none)
 Predefined PDO Assignment: '1.Ch Standard, 1xABC, Legacy EL5101'
 Predefined PDO Assignment: '1.Ch Compact, 1xABC, Legacy EL5101'
Predefined PDO Assignment: '1.Ch Standard, 1xABC'
 Predefined PDO Assignment: '2.Ch Standard, 2xAB'
 Predefined PDO Assignment: '1.Ch Compact, 1xABC'
 Predefined PDO Assignment: '2.Ch Compact, 2xAB'
 Predefined PDO Assignment: '1.Ch Standard, 1xABC, extended DC mode, 32Bit time stamp'
 Predefined PDO Assignment: '1.Ch Standard, 1xABC, extended DC mode, 64Bit time stamp'
 Predefined PDO Assignment: '1.Ch Standard, 1xABC, Period mode'
 Predefined PDO Assignment: '2.Ch Standard, 2xAB, Period mode'
 Predefined PDO Assignment: '1.Ch Standard, 1xABC, Frequency mode'
 Predefined PDO Assignment: '2.Ch Standard, 2xAB, Frequency mode'
 Predefined PDO Assignment: '1.Ch Standard, 1xABC, Duty Cycle mode'
 Predefined PDO Assignment: '2.Ch Standard, 2xAB, counter mode'
 Predefined PDO Assignment: '2.Ch Compact, 2xAB, counter mode'

Predefined PDO Assignment: '1.Ch Standard, 1xABC'

Load PDO info from device

Sync Unit Assignment...

Fig. 47: Process data, Predefined PDO (default: 1.Ch Standard, 1xABC)

15 PDO assignments are available for 1-channel mode [► 57] and 2-channel mode in the modes “Standard”, “Compact”, “Counter” and “Legacy” (1-channel mode only).

● Note on using the timestamp function

I In order to be able to use the timestamp function, the ED5112 should be operated in “DC-Synchron” or “DC-Synchron (input based)” mode.

In 2-channel mode the following predefined PDOs are available:

Predefined PDO Assignments for Compact mode (two-channel mode)

Predefined PDO Assignment	PDO Assignment
2.Ch Compact, 2xAB	SM3: 0x1A03 [► 173] - ENC Status Compact Channel 1 (8.0) 0x1A12 [► 178] - ENC Status Compact Channel 2 (8.0) SM2: 0x1603 [► 162] - ENC Control Compact Channel 1 (4.0) 0x160B [► 164] - ENC Control Compact Channel 2 (4.0)

Predefined PDO Assignments for Standard mode (two-channel mode)

Predefined PDO Assignment	PDO Assignment
2.Ch Standard, 2xAB	SM3: 0x1A02 [► 172] - ENC Status Channel 1 (12.0) 0x1A11 [► 177] - ENC Status Channel 2 (12.0) SM2: 0x1602 [► 162] - ENC Control Channel 1 (6.0) 0x160A [► 164] - ENC Control Channel 2 (6.0)
2.Ch Standard, 2xAB, Period mode	SM3: 0x1A02 [► 172] - ENC Status Channel 1 (12.0) 0x1A0A [► 175] - ENC Period Channel 1 (4.0) 0x1A11 [► 177] - ENC Status Channel 2 (12.0) 0x1A19 [► 179] - ENC Period Channel 2 (4.0) SM2: 0x1602 [► 162] - ENC Control Channel 1 (6.0) 0x160A [► 164] - ENC Control Channel 2 (6.0)
2.Ch Standard, 2xAB, Frequency mode,	SM3: 0x1A02 [► 172] - ENC Status Channel 1 (12.0) 0x1A08 [► 175] - ENC Frequency Channel 1 (4.0) 0x1A11 [► 177] - ENC Status Channel 2 (12.0) 0x1A17 [► 179] - ENC Frequency Channel 2 (4.0) SM2: 0x1602 [► 162] - ENC Control Channel 1 (6.0) 0x160A [► 164] - ENC Control Channel 2 (6.0)

Predefined PDO assignments for Counter mode (two-channel mode)

Predefined PDO Assignment	PDO Assignment
2.Ch Standard, 2xAB, counter mode,	SM3: 0x1A04 [► 173] - ENC Status Counter Channel 1 (8.0) 0x1A13 [► 178] - ENC Status Counter Channel 2 (8.0) SM2: 0x1604 [► 162] - ENC Control Counter Channel 1 (6.0) 0x160C [► 164] - ENC Control Counter Channel 2 (6.0)
2.Ch Compact, 2xAB counter mode,	SM3: 0x1A05 [► 174] - ENC Status Compact Counter Channel 1 (6.0) 0x1A14 [► 179] - ENC Status Compact Counter Channel 2 (6.0) SM2: 0x1605 [► 163] - ENC Control Compact Counter Channel 1 (4.0) 0x160D [► 165] - ENC Control Compact Counter Channel 2 (4.0)

4.2.2.4 Synchronicity mode

The terminal can be operated in three different operation modes. Depending on the operation mode, the process data are synchronized by the terminal at different times and made available to the EtherCAT frame.

The following operation modes are available for selection in the “DC” tab:

Operation mode	Description
FreeRun/SM Synchron	Cyclic, frame-triggered exchange of process data. An Ethernet frame triggers the process data provision for the next retrieving frame.
DC-Synchron	Cyclically constant determination of the counter value by the integrated distributed clocks unit. The configuration corresponds to an output module. The local SYNC event is triggered shortly after the passage of the EtherCAT frame. This means that the output data just delivered is output immediately.
DC-Synchron (input based)	Cyclically constant determination of the counter value by the integrated distributed clocks unit. The configuration corresponds to an input module. The local SYNC event is triggered before the EtherCAT frame. This makes current input data available for onward transport.

NOTICE



Further information

For more information, see the chapter “[I/O Synchronization via Distributed Clocks](#)” in the EtherCAT system manual.

4.2.2.5 EtherCAT cycle time

The EtherCAT cycle time depends on the selection of the process data to be transferred. The following table provides an overview of the recommended cycle time, depending on the “Predefined PDO Assignment”. The specifications refer to a multiple of the “Base Time” to be set via the TwinCAT Master. If a faster cycle time is used, the process data “Input cycle counter” 0x6002:0F must be used to monitor when new process data are delivered.

ED5112 - Predefined PDO assignment in 2-channel mode	EtherCAT cycle time	
	Min.	Max.
2. Ch. Standard, 2xAB	typ. 125 µs	typ. 150 µs
2. Ch. Compact, 2xAB	typ. 125 µs	typ. 150 µs
2. Ch. Standard, 2xAB, Period mode	typ. 125 µs	typ. 150 µs
2. Ch. Standard, 2xAB, Frequency mode	typ. 125 µs	typ. 150 µs
2. Ch. Standard, 2xAB, Counter mode	typ. 125 µs	typ. 150 µs
2. Ch. Compact, 2xAB, Counter mode	typ. 125 µs	typ. 150 µs

4.2.2.6 “Legacy EL5101” mode

The process image of the terminal is based on the MDP511 profile. This profile has been extended for improved functionality in terms of status bits. The terminal provides various status information in the respective “Predefined PDO Assignments”. A process image compatible with the EL5101 is provided via “Legacy EL5101” mode. The process image of the terminal outside “Legacy EL5101” mode differs by the following status bits in the PDO assignment:

EL5101		ED5112			
“Standard / Line Motion” mode		“Legacy EL5101” mode (Ch.1 n = 0, Ch.2 n = 1)		“n.Ch. Standard / Compact / counter” mode (Ch.1 n = 0, Ch.2 n = 1)	
0x6010:0D	Status_Status of extern latch	0x60n0:0D	Status_Status of extern latch	0x60n2:0D	Status_Diag
0x6010:0E	Status_Sync error	0x60n0:0E	Status_Sync error	0x60n2:0E	Status_TxPDO State
0x6010:0F	Status_Status TxPDO State	0x60n0:0F	Status_Status TxPDO State	0x60n2:0F	Status_Status Input cycle counter
0x6010:10	Status_Status TxPDO Toggle	0x60n0:10	Status_Status TxPDO Toggle	0x60n2:10	-
-	-	-	-	0x60n2:14	Status_Status of extern latch

“Legacy EL5101” mode enables the use of existing function blocks based on the modified status bits.

i ED5112 in conjunction with older TwinCAT versions

From TwinCAT version 3.1 Build 4024 and higher, all predefined PDOs of the ED5112 can be automatically linked to the NC. For older TwinCAT versions the “Legacy EL5101” mode must be used. Note the associated functionality restrictions.

i Functional compatibility with EL5101

ED5112 is not functionally compatible with the EL5101. Internal calculation methods and timings may differ. Compatibility with existing projects must be checked on a case-by-case basis.

Limitations of “Legacy EL5101” mode

The following table provides an overview of the functions available in “Legacy EL5101” mode:

Function		“Legacy” mode
Set counter value via	PLC variable	Yes
	zero pulse C	No
	Latch input	No
Reset counter value via	zero pulse C	Yes
	Latch input	Yes
Save counter value via	zero pulse C	Yes
	Latch input	Yes
	Gate input/Latch extern 2	No
Lock counter value via	PLC variable	No
	Gate input/Latch extern 2	Yes
Detect counting direction		No
Detect reversion of rotation		No
Frequency calculation		No
Period duration calculation		No
Duty cycle evaluation		No
Micro-increments		No
Timestamp function		No
Filter function		Yes
Plausibility check		Yes

4.2.3 Basic functions in two-channel mode 2xAB

4.2.3.1 Counter value

The counter value is displayed in the input process data "Counter value" (0x60n0:11). It indicates the current counter value in the terminal. You can adapt it to the application using the following settings.

- [Selection of encoder type \[► 109\]](#) (Index 0x80n1:1D "Counter mode")
- [Evaluation of the counter value \[► 110\]](#) (Index 0x80n0:06 "Evaluation mode")
- [Determination of the counter limits \[► 111\]](#) (Index 0x80n1:1B "Reset counter value"/
Index 0x80n1:1A "Limit counter value")
- [Reversion of rotation \[► 113\]](#) (Index 0x80n0:0E "Reversion of rotation")

4.2.3.1.1 Selection of encoder type (Counter mode)

To ensure a correct acquisition of the counter value, you must first select the appropriate encoder type.

The connected encoder is selected via index 0x80n1:1D "Counter mode". Explanations of the supported encoder and signal types can be found in chapter "[Supported encoder / signal types \[► 14\]](#)"

Index (hex)	Name	Meaning
80n1:1D	Counter mode	Selecting the encoder
	0: Encoder RS422 (diff. input)	RS422 encoder without zero pulse
	1: Counter RS422 (diff. input)	RS422 counter/pulse generator without zero pulse. Direction preset via track B
	2: Encoder TTL (single ended)	TTL encoder without zero pulse
	3: Counter TTL (single ended)	TTL counter/pulse generator without zero pulse. Direction preset via track B
	4: Encoder open collector	Open collector encoder without zero pulse
	5: Counter open collector	Open collector counter/pulse generator without zero pulse. Direction preset via track B

In the following sections, settings 0, 2 and 4 are generally referred to as "encoder" and settings 1, 3 and 5 as "counter/pulse generator".

4.2.3.1.2 Encoder operating voltage (supply voltage)

The encoder supply is generated internally from the 24 V of the power contacts. The encoder supply can be set in index `0x8001:17` [► 151] "Supply voltage". An operating voltage of 5 V DC is preset. Voltage values of 5 V DC, 12 V DC, and 24 V DC can be selected. The setting applies to both channels. Before switching to higher voltages, ensure that both encoders support the voltage range.

The following tolerances apply:

Voltage range	Tolerance
5 V DC	+/-5% (4.75 V...5.25 V)
12 V DC	+/-10% (10.8 V...13.2 V)
24 V DC	-15% to +20% (20.4 V...28.8 V)



Setting the encoder supply via index `0x8001:17` [► 151]

The encoder supply is set centrally for both channels via the index `0x8001:17` [► 151] (channel 1). The corresponding index `0x8011:17` of the second channel has no parameterization function.

NOTICE

Setting the encoder supply voltage

- Before switching to a higher voltage, make sure that the connected encoders support the selected voltage range!
- To write to `0x80n1:17` "Supply voltage" you have to set the value `0x72657375` (ASCII: "user") in index `0xF008` [► 182] "Code word".

4.2.3.1.3 Evaluation of the counter value

Evaluation of the "Counter value" is set through index `0x80n0:06` "Evaluation mode".

- Evaluation of the input signals (index `0x80n0:06` "Evaluation mode"): The input signal can be subject to 4-fold, 2-fold or 1-fold evaluation.
 - 1-fold evaluation: the rising edges at track A are counted.
 - 2-fold evaluation: the rising and falling edges at track A are counted.
 - 4-fold evaluation: the rising and falling edges at tracks A and B are counted.

In the delivery state 4-fold evaluation is selected, as this enables the highest resolution of the input signal.

4.2.3.1.4 Determining the counter limits (Reset counter value / Limit counter value)

Counter limits in delivery state

In delivery state the counter value "Counter Value" counts in the range from 0 to the maximum counter depth. When the maximum counter depth is exceeded "Counter overflow" the counter starts counting up from zero again. When the counter limit is exceeded, this is indicated by the "Counter overflow" bits (see chapter "Determining the counter limits ("Reset counter value"/"Limit counter value" [► 112])").

- PDO Assignment "Standard": 0 to $2^{32}-1$
- PDO Assignment "Compact": 0 to $2^{16}-1$

When a counter underflow occurs, the count continues at the maximum counter depth even if e.g. "Enable extern reset" is enabled in index 0x80n0:02. The underflow is identified with the corresponding "Counter underflow" bit.

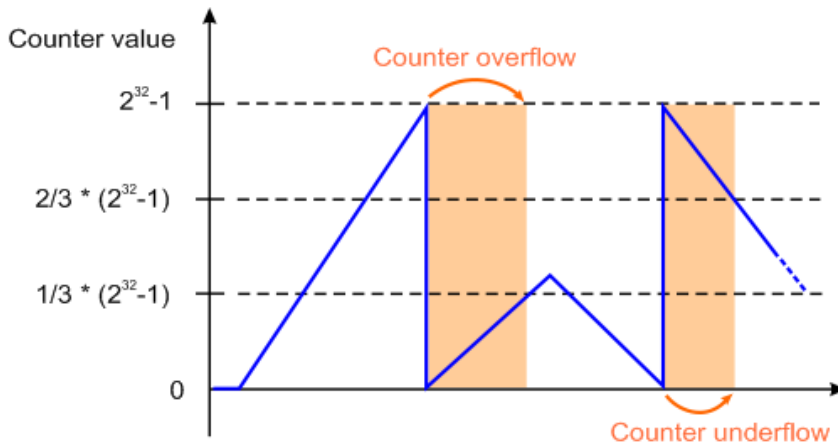


Fig. 48: Counter overflow and underflow in delivery state

Counter limits with defined value range

If counting is only to take place in a defined value range, the counter limits can be adjusted.



Set counter limits

For writing to index 0x80n1:1B "Reset counter value" and index 0x80n1:1A "Limit counter value", the value 0x72657375 (ASCII: "user") must be set in 0xF008 [► 182] "Code word".

- Specify the lower counter limit in index 0x80n1:1B "Reset counter value".
- Specify the upper counter limit in index 0x80n1:1A "Limit counter value".

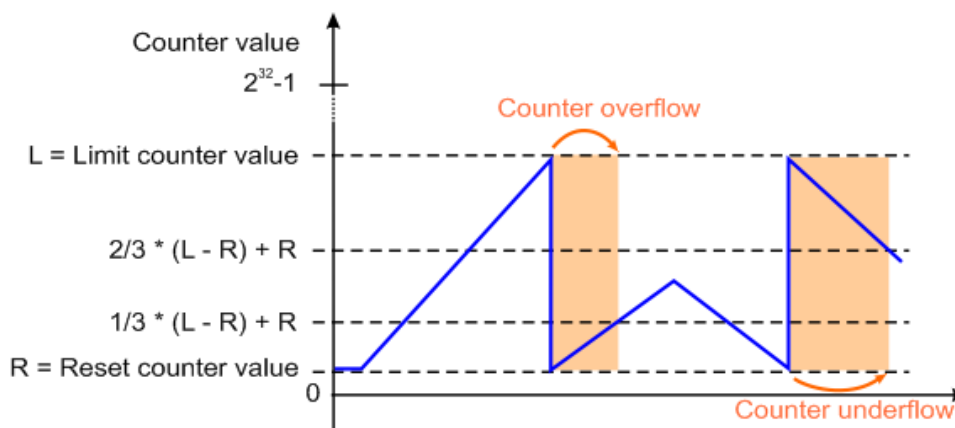


Fig. 49: Counter overflow and underflow with defined value range



Counter limits

- The lower counter limit index 0x80n1:1B “Reset counter value” must always be less than the upper counter limit 0x80n1:1A “Limit counter value”.
If this is not the case, the last value entered is not accepted.
- If the lower counter limit in index 0x80n1:1B “Reset counter value” is greater than 0, the Motion Control application (NC/CNC) can only be used in a limited range.

If the counter is parameterized to a counter value outside the counter limits during runtime, this counter value is applied. Exceeding the counter limit is indicated by the process data “Counter value out of range” (index 0x60n2:15).

Example:

The process data “Set counter value” (0x70n0:11) contains a value that exceeds the counter limits, and the bit in the process data “Set counter” (0x70n0:03) is activated.

- The value specified in the process data “Set counter value” (0x70n0:11) is used.
- The bit in the process data “Counter value out of range” (0x60n2:15) is set.

If the counter limits are parameterized in such a way that the current counter value is outside these limits, the underflow/overflow of the counter limit is also shown via the process data “Counter value out of range” (0x60n2:15).

Counter overflow and Counter underflow

An overflow or underflow of the counter limits is indicated by the process data “Counter underflow” (0x60n0:04) or “Counter overflow” (0x60n0:05).

- The bit in the process data “Counter underflow” (0x60n0:04) is set when an underflow occurs 0x80n1:1B “Reset counter value” → 0x80n1:1A “Limit counter value”.
 - With the preset parameters this corresponds to “..00 → ..FF”
It is reset if 2/3 of the counting range are underrun.
 - For counting limits with fixed values, this corresponds to:
 $\frac{2}{3} * (\text{“Limit counter value”} - \text{“Reset counter value”}) + \text{“Reset counter value”}$
- The bit in the process data “Counter overflow” (0x60n0:05) is set when an overflow occurs 0x80n1:1A “Limit counter value” → 0x80n1:1B “Reset counter value”.
 - With default parameters “..FF → ..00”
It is reset if 1/3 of the counter range is exceeded.
 - For counting limits with fixed values, this corresponds to:
 $\frac{1}{3} * (\text{“Limit counter value”} - \text{“Reset counter value”}) + \text{“Reset counter value”}$

Example 1:

0x80n1:1A “Limit counter value” = $2^{12} - 1 = 4095$

0x80n1:1B “Reset counter value” = 0

The “Counter underflow” bit is reset when: $\frac{2}{3} \times 4095 = 2730$ is reached.

The “Counter overflow” bit is reset when: $\frac{1}{3} \times 4095 = 1365$ is reached.

Example 2:

0x80n1:1A “Limit counter value” = $2^{12} - 1 = 4095$

0x80n1:1B “Reset counter value” = 400

The “Counter underflow” bit is reset when: $\frac{2}{3} \times (4095 - 400) + 400 = 2463$ is reached.

The “Counter overflow” bit is reset when: $\frac{1}{3} \times (4095 - 400) + 400 = 1632$ is reached.

4.2.3.1.5 Reversion of rotation

- **With an encoder**, the counting direction is determined by the phase position of the signals on tracks A and B.
 - Forward (cw): Signal on track A leads track B by 90°
 - Reverse (ccw): Signal on track A lags track B by 90°

To adapt the counting direction to the application, this logic can be inverted by setting the bit in index 0x80n0:0E "Reversion of rotation".

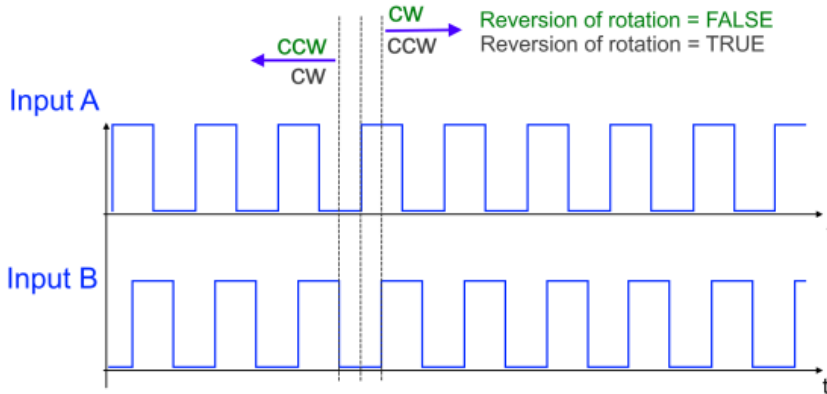


Fig. 50: Reversion of counting direction (Index 0x80n0:0E "Reversion of rotation") for an encoder

- **With a counter/pulse generator** the counting direction is determined by the level at track B.
 - Forward (cw): LOW level at track B or input open
 - Reverse (ccw): HIGH level at track B

Setting the bit in index 0x80n0:0E "Reversion of rotation" also inverts the logic of the counting direction. An overview of the resulting counting direction is shown in the following table.

The current level at input B is displayed via process data "Status of input B" (0x60n0:0A).

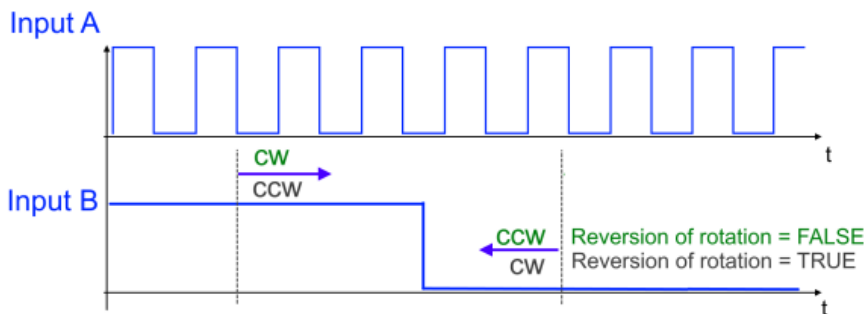


Fig. 51: Reversion of counting direction (Index 0x80n0:0E "Reversion of rotation") for a counter/pulse generator

0x80n1:1D "Counter mode"	Level at input track B	0x80n0:0E "Reversion of rotation"	Resulting counting direction
1: Counter RS422 (diff. input)	Input open / LOW level	FALSE	positive
		TRUE	negative
	RS422 signal level	FALSE	negative
		TRUE	positive
3: Counter TTL (single ended)	Input open / LOW level, voltage level < 0.8 V	FALSE	positive
		TRUE	negative
	TTL voltage level 2.0 V to 6.0 V, with min. 2.1 mA current	FALSE	negative
		TRUE	positive
5: Counter open collector	Input open / LOW level, voltage level < 0.8 V	FALSE	positive
		TRUE	negative
	Open collector voltage level 2.0 V to 6.0 V, with min. 2.1 mA current	FALSE	negative
		TRUE	positive

i Status LED input B as counter RS422 (diff. input)

If the input of track B is open in counter mode "RS422 (diff. input)", a broken wire is detected and the status LED of input B lights up red. The error detection and indication via the LED can be deactivated via index 0x80n0:0C "Error detection B".

4.2.3.2 Reset counter value via gate/latch combination input

The “Latch” and “Gate” inputs each combine gate and latch functions in a single input and are therefore referred to below as gate/latch combination inputs.

A recurring reset of the counter value (input process data “Counter value” (0x60n0:11 [► 152])) to “0” can be performed by:

- Gate/Latch combination input: one edge (positive/negative) at the “Latch extern” input (0x80n0:02 “Enable extern reset”)

The settings are made in the configuration data, so it is not necessary to reactivate the device after a reset.

Reset counter value via gate/latch combination input (Enable extern reset)

The counter value can be set to zero via the external gate/latch combination input.

- Presetting of the reset value via index 0x80n1:1B [► 151] “Reset counter value”, (Default: 0)
- To activate this function set the bit in index 0x80n0:02 [► 150] “Enable extern reset”.
- Index 0x80n0:10 [► 150] “Extern reset polarity” can be used to specify at which edge the gate/latch combination input is active.
 - 0: “Fall” - the counter is set to zero with a falling edge
 - 1: “Rise” - the counter is set to zero with a rising edge

There is no status message via the process data.



Activation of gate and latch functions via the same edge at the gate/latch combination input in 2-channel mode 2xAB

When the gate function and a latch function is activated via the same edge at the gate/latch combination input, the latch function is always executed first, after which the counter value is locked via the gate function.

Example:

Index 0x80n0:04 [► 150] “Gate polarity” (1 = “Enable pos. gate”) and

Index 0x80n0:02 “Enable extern reset” = 1 with 0x80n0:10 “Extern reset polarity” = 1 (reset on a positive edge at the gate/latch combination input)

With a positive edge at the gate/latch combination input the current counter value is first set to zero (reset). After that, the counter value is locked.

The same applies to the use of index 0x80n0:04 “Gate polarity” (2 = “Enable neg. gate”) and the simultaneous activation of index 0x80n0:02 “Enable extern reset” with 0x80n0:10 “Extern reset polarity” = 0 (reset on a negative edge at the gate/latch combination input).

4.2.3.3 Set counter value via gate/latch combination input

The counter value in the input process data “Counter value” can be set to a predefined value at runtime and thus be used for synchronization with other processes. The preset can be activated in the following ways:

- **PLC variable:** [► 116] ; the counter value can be set from within the PLC application (output process data “Set counter value”)
- **Gate input [► 116]:** a positive or negative edge at the “Latch extern” input (output process data “Set counter on latch extern on positive/negative edge”)

The “Latch” and “Gate” inputs each combine gate and latch functions in a single input and are therefore referred to below as gate/latch combination inputs.

● Multiple activation of “Set counter on ...”

I If several commands are activated to accept the preset counter value, only the command that is set first is accepted by the terminal. All other commands are ignored but remain activated, depending on the system.

- The counter value is set to the preset counter value at the first activated event and confirmed by the bit in process data “Set counter done” (0x60n0:03 [► 152]).
- The counter value specification cannot be reactivated until all activated commands for the transfer of the counter value have been deactivated. This is confirmed by setting the bit in process data “Set counter done” (0x60n0:03) to FALSE.

Set counter value via a PLC variable (Set counter value)

The counter value can be set to a predefined value during runtime via the process data “Set counter” (0x70n0:03). In the PLC this bit can be linked to a digital input, for example, or used directly as a variable.

- Setting the counter value using the process data “Set counter value” (0x70n0:11)
- Activation of the counter value setting via the PLC variable: “Set counter” (0x70n0:03)
- To confirm, the “Set counter done” bit (0x60n0:03) is set to TRUE.
- The counter value setting can only be reactivated once the bit in the process data “Set counter” (0x70n0:03) has been set to FALSE.

Setting the counter value via the gate/latch combination input (Set counter on latch extern on positive/negative edge)

The counter value can be set to a preset value during runtime via the process data by the positive or negative edge at the gate/latch combination input.

- Setting the counter value via the output process data “Set counter value” (0x70n0:11)
- Activation of the counter value setting via
 - the positive edge at the external gate/latch combination input:
output process data “Set counter on latch extern on positive edge” (0x70n0:0A)
 - the negative edge at the external gate/latch combination input:
output process data “Set counter on latch extern on negative edge” (0x70n0:0B)
- If the bit (TRUE) is set in the output process data “Set counter on latch extern on positive/negative edge” (0x70n0:0A/0B), the next positive or negative edge at the gate input/latch combination input sets the counter value in the input process data “Counter value” to the specified counter value in the output process data “Set counter value”.
- To confirm, the bit in the input process data “Set counter done” (0x60n0:03) is set to TRUE.
- The counter value setting can only be reactivated once the bit in the output process data “Set counter on latch extern on positive/negative edge” (0x70n0:0A/0B) has been set to FALSE.



Activation of gate and latch functions via the same edge at the gate/latch combination input in 2-channel mode 2xAB

When the gate function and a latch function is activated via the same edge at the gate/latch combination input, the latch function is always executed first, after which the counter value is locked via the gate function.

Example:

Index `0x80n0:04` [► 150] “Gate polarity” (1 = “Enable pos. gate”) and

Output process data “Set counter on latch extern on positive edge” (`0x70n0:0A`) = 1

When a positive edge is detected at the gate/latch combination input, the current counter value is first set to the value specified in the output process data “Set counter value” (`0x70n0:11`). After that, the counter value is locked.

The same applies to the use of index `0x80n0:04` “Gate polarity” (2 = “Enable neg. gate”) and the simultaneous activation of the output process data “Set counter on latch extern on negative edge” (`0x70n0:0B`).

4.2.3.4 Save counter value

The latch function enables the current counter value to be stored in separate process data, independent of the cycle time. The latch function can be triggered as follows:

- Gate/latch combination input [► 118] positive/negative edge at the latch input (output process data “Enable latch extern on positive/negative edge”)

Index 0x80n0:22 [► 150] “Enable continuous latch extern” can be used to parameterize whether the function is executed at every parameterized external edge at the latch input or only once after every activation.

i Multiple activation of the latch function

If several commands are activated simultaneously to save the counter value in the “Latch value” process data (0x60n0:12 [► 152]), only the command that is set first is accepted by the terminal.

- The counter value is stored in the process data “Latch value” (0x60n0:12) at the next occurring event and confirmed with the corresponding bit.
- All other activated events are ignored.
- The counter value storage cannot be reactivated until all activated commands for latching the value have been deactivated. This also applies if they were activated after confirmation by the occurring event.

Save the counter value via a positive/negative edge at the latch input (Enable latch extern on positive/negative edge)

- The counter value at the “Latch extern” input can be saved via:
 - Process data “Enable latch extern on positive edge” (0x70n0:02 [► 155]) = TRUE
At the first external latch pulse with positive edge, the current counter value is stored in the process data “Latch value” (0x60n0:12 [► 152]).
 - Process data “Enable latch extern on negative edge” (0x70n0:04 [► 155]) = TRUE
At the first external latch pulse with negative edge the current counter value is stored in the process data “Latch value” (0x60n0:12 [► 152]).
 - Simultaneous activation of the bits in the process data “Enable latch extern on positive edge” (0x70n0:02) and “Enable latch extern on negative edge” (0x70n0:04)
The current counter value is stored in the process data “Latch value” (0x60n0:12), at the first external latch pulse, independent of the edge polarity.
- Specification whether it is necessary to reactivate the command to save the counter value via:
 - “Enable continuous latch extern” Index 0x80n0:22 [► 150] = FALSE
The following pulses at the “Latch extern” input have no effect on the latch value in the process data “Enable latch extern on positive edge” (0x70n0:02) and “Enable latch extern on negative edge” (0x70n0:04) when the bit in the process data “Latch value” (0x60n0:12) is set.
Only when the bit in the process data “Latch extern valid” (0x60n0:02 [► 152]) is set to FALSE can a new counter value be written to the latch input in the process data “Latch value” (0x60n0:12)
 - “Enable continuous latch extern” Index 0x80n0:22 [► 150] = TRUE
The counter value is written to the process data “Latch value” (0x60n0:12) each time a configured edge occurs at the “Latch extern” input.
There is no need to reactivate the process data “Enable latch extern on positive edge” (0x70n0:02) and “Enable latch extern on negative edge” (0x70n0:04).
- Saving of the count value in the process data “Latch value” (0x60n0:12) is confirmed by the bit in the process data “Latch extern valid” (0x60n0:02).
- The status of the “Latch extern” input can be monitored using the process data “Status of extern latch” (0x60n2:14 [► 154]).



Activation of gate and latch functions via the same edge at the gate/latch combination input in 2-channel mode 2xAB

When the gate function and a latch function is activated via the same edge at the gate/latch combination input, the latch function is always executed first, after which the counter value is locked via the gate function.

Example:

Index `0x80n0:04` [[▶ 150](#)] “Gate polarity” (1 = “Enable pos. gate”) and

Output process data “Enable latch extern on positive edge” (`0x70n0:02`) = 1

When a positive edge is detected at the gate/latch combination input, the current counter value is first stored in the input process data “Latch value” (`0x60n0:12`). After that, the counter value is locked.

The same applies to the use of the index `0x80n0:04` “Gate polarity” (2 = “Enable neg. gate”) and the simultaneous activation of the output process data “Enable latch extern on negative edge” (`0x70n0:04`).

4.2.3.5 Lock counter value

The “Latch” and “Gate” inputs each combine gate and latch functions in a single input and are therefore referred to below as gate/latch combination inputs.

The gate function enables locking of the counter “Counter value” (0x60n0:11 [► 152]).

The counter is locked at the first pulse at the gate/latch combination input. Subsequent pulses have no influence on the counter value. This allows a timeframe to be defined in which counting signals are acquired. The gate function can be triggered by:

- Gate/latch combination input: [► 76] a positive or negative edge at the gate/latch combination input (index 0x80n0:04 “Gate polarity” = “Enable pos./neg. gate”),
- PLC variable: [► 120] The counter can be locked from the PLC application (output process data “Set software gate”).

The gate/latch combination input may be used as a second latch input “Latch extern 2”.

Lock counter value via a positive/negative edge at the gate/latch combination input (Enable pos./neg. gate)

- The level at the gate/latch combination input at which the counter value is locked during runtime can be specified via index 0x80n0:04 [► 150] “Gate polarity”.
 - 0: Disable gate
The gate/latch combination input is disabled to lock the counter. It can still be used as external latch input for storage.
 - 1: Enable pos. gate
The counter value is locked with HIGH level at the gate/latch combination input.
 - 2: Enable neg. gate
The counter value is locked with LOW level at the gate/latch combination input
- The current level at the gate/latch combination input is displayed via the input process data “Status of input gate” (0x60n0:0C [► 152]).



Activation of gate and latch functions via the same edge at the gate/latch combination input in 2-channel mode 2xAB

When the gate function and a latch function is activated via the same edge at the gate/latch combination input, the latch function is always executed first, after which the counter value is locked via the gate function.

Example:

Index 0x80n0:04 [► 150] “Gate polarity” (1 = “Enable pos. gate”) and

Index 0x80n0:02 “Enable extern reset” = 1 with 0x80n0:10 “Extern reset polarity” = 1 (reset on a positive edge at the gate/latch combination input)

With a positive edge at the gate/latch combination input the current counter value is first set to zero (reset). After that, the counter value is locked.

The same applies to the use of index 0x80n0:04 “Gate polarity” (2 = “Enable neg. gate”) and the simultaneous activation of index 0x80n0:02 “Enable extern reset” with 0x80n0:10 “Extern reset polarity” = 0 (reset on a negative edge at the gate/latch combination input).

Lock counter value via a PLC variable (Set software gate)

The counter value can be locked from the PLC application.

- Output process data “Set software gate” (0x70n0:09 [► 155]) = TRUE
The counter is locked.
- To confirm, set the bit in the input process data “Software gate valid” (0x60n2:11 [► 154]) = TRUE.
- Output process data “Set software gate” (0x70n0:09) = FALSE
The counter is unlocked.

4.2.4 Extended functionalities two-channel mode 2xAB

4.2.4.1 Frequency measurement

In addition to the count value, the frequency value (Frequency value) can also be calculated and displayed. The following limit values apply to the determination of measured values:

Measured value output	Measured value limit		Comment
	Lower	Top	
Frequency value	0.095 Hz	5 MHz	With 4-fold evaluation Signal type: "RS422 (diff. input)"
	0.095 Hz	1 MHz	With 4-fold evaluation Signal type: "TTL (single ended), open collector"
	0.095 Hz	100 kHz	With 4-fold evaluation Signal type: "open collector"

Frequency measurement procedure (Frequency value)

The frequency is calculated from the number of increments or position value changes within a time interval. The result is output via the process data "Frequency value" (0x60n0:13 [► 152]).

Frequency = number of periods / time interval	
Number of periods	The number of complete periods on track A within the timeframe (0x80n0:11 [► 150]) is measured. Counting starts with the first positive edge within the timeframe (index 0x80n0:11 "Frequency window").
Time interval	The time measurement starts with the first positive edge on track A within the "Frequency window" and ends with the last negative edge within the "Frequency window". The time is measured with a resolution of 10 ns. Special case: If no full period is measured within the timeframe (Frequency window), another timeframe is started. The maximum time measurement for recording an entire period is limited by the wait time (Frequency wait time).

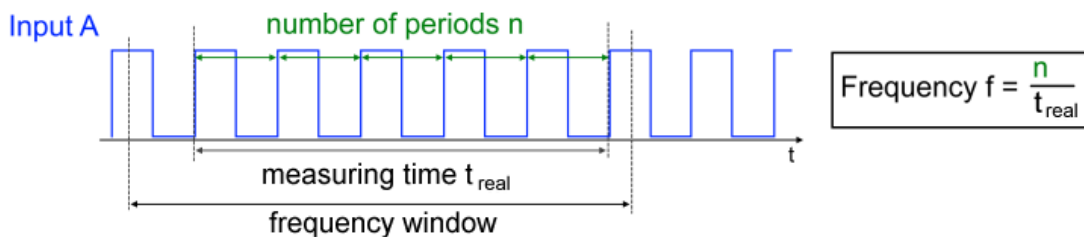


Fig. 52: Frequency measurement - "Frequency value"

- The frequency window is selected in index 0x80n0:11 "Frequency window". The default value is 10 ms. Follow the instructions below to select the correct timeframe.
- "Frequency scaling" (index 0x80n0:13 [► 150]) indicates the resolution of the output frequency. The default value is 0.01 Hz. The frequency can also be output in the unit 1 Hz (set 0x80n0:13 "Frequency scaling" to 1_{dec}). If other resolutions are required, the conversion can be done via 0x80n0:1D [► 150] "Frequency numerator".
- The calculated frequency value is output via the input process data "Frequency value" (0x60n0:13 [► 152]).
- The calculation is carried out acyclically and without reference to the distributed clock system and is therefore independent of the operation mode.
- Locking the counter value via the gate, a C-reset or external reset has no effect on the frequency calculation.

Correct selection of the timeframe:

In delivery state the timeframe for the frequency measurement is set to 10 ms.

The accuracy and size of the determined frequency depends on the size of the timeframe (0x80n0:11 [► 150] “Frequency window”), which must be selected to match the application. The minimum value to be entered here is twice the period value of the smallest measured frequency.

$$\text{Frequency window} \geq 2 * \frac{1}{f_{\min}}$$

At constant velocities, select a larger timeframe so that the best possible averaging can take place.

In situations where frequent positive or negative accelerations are encountered, select a smaller timeframe in order to be able to respond more quickly to changing position values. Alternatively, period value measurement can be used for situations with variable speeds.

Special case: frequency measurement

If no full period is detected within the “Frequency window” (see figure (1) below), another “Frequency window” timeframe is started in order to record at least one full period (see figure (2) below). This happens until the maximum waiting time (0x80n0:17 [► 150] “Frequency wait time”) has elapsed. Until then, the last valid value in the input process data “Frequency value” (0x60n0:13 [► 152]) is displayed.

If no full period is detected within the waiting time, the measurement is discarded and the output in the process data “Frequency value” (0x60n0:13) is set to “0”.

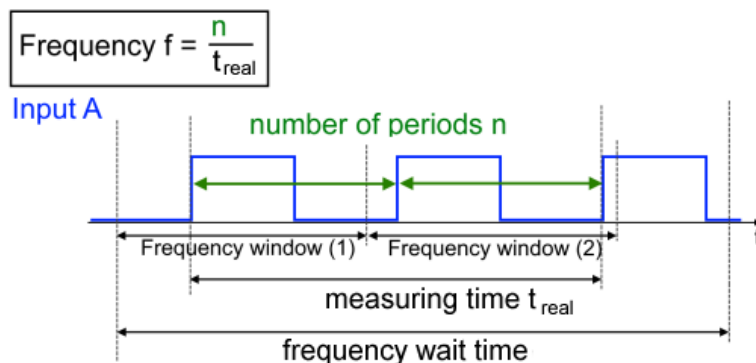


Fig. 53: Frequency measurement outside the frequency window with waiting time

**Difference between frequency and period value measurement**

The period value is recalculated for each cycle and output in the process data. The frequency measurement always averages the measured periods over a timeframe. Thus, “Period value” is a current value, and “Frequency value” is an average value.

4.2.4.2 Period value measurement

In addition to the count value, the period value (Period value) can also be calculated and displayed. The following limit values apply to the determination of measured values:

Measured value output	Measured value limit		Comment
	Lower	Top	
Period value	0.20 μ s	21 s	With 4-fold evaluation, signal type: "RS422 (diff. input)"
	1 μ s	21 s	With 4-fold evaluation, signal type: "TTL (single ended)", "open collector"

Period value measurement sequence (Period value)

- For the period value measurement, the time between two positive edges of input A is measured with a resolution of 10 ns.
- In each case the last period within the PLC cycle is considered and output as separate process data "Period value" (0x60n0:14 [► 152]).
- "Period scaling" (index 0x80n0:14) indicates the resolution of the output period value. The default value is 10 ns. Alternatively the period value can be output in the unit 100 ns (set 0x80n0:14 "Period scaling" to 100_{dec}) or 500 ns (set 0x80n0:14 "Period scaling" to 500_{dec}).

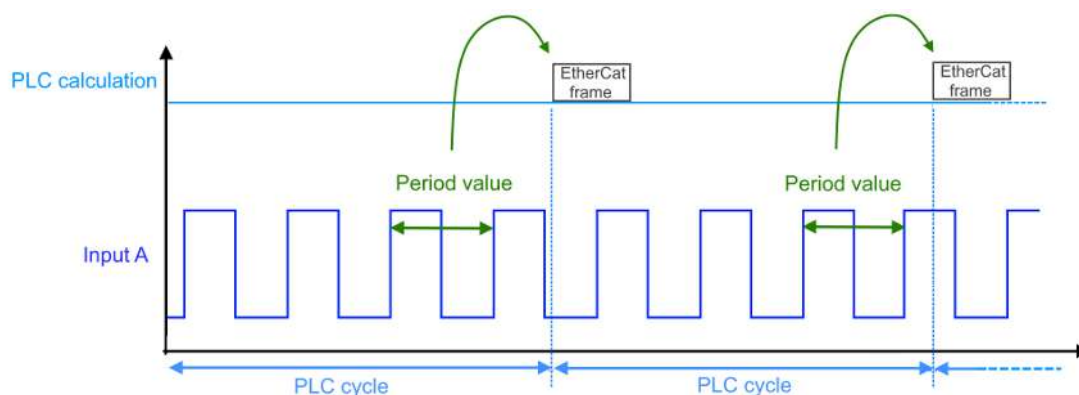


Fig. 54: Period value measurement

- If no full period is detected within a PLC cycle (two positive edges of input A), the last valid value is output.
- The period measurement continues across cycles. As soon as a new value is available, the process data "Period value" (0x60n0:14 [► 152]) is updated.
- If no full period is detected within 21 s, the measurement is discarded and the output in the process data "Period value" (0x60n0:14 [► 152]) is set to the maximum value 2147483648.

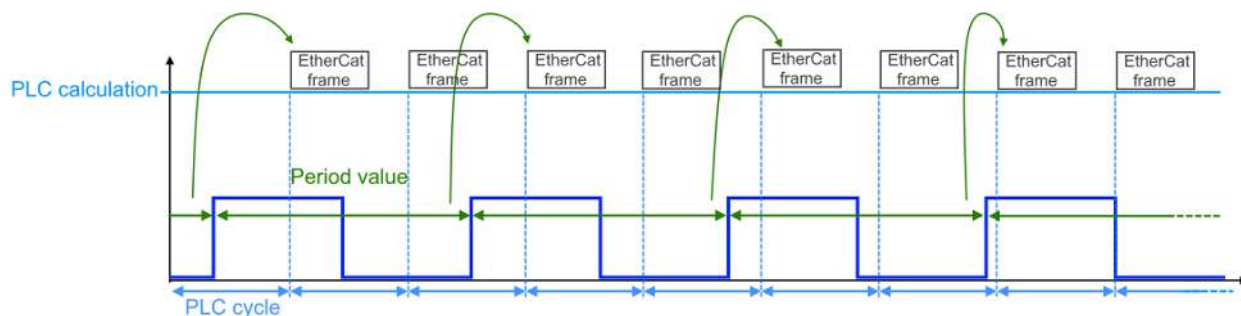


Fig. 55: Period value measurement for long periods



Difference between frequency and period value measurement

The period value is recalculated for each cycle and output in the process data. The frequency measurement always averages the measured periods over a timeframe. Thus, "Period value" is a current value, and "Frequency value" is an average value.

4.2.4.3 Velocity, speed calculation

In addition to the counter value, the velocity and speed are also be measured. The measured values are determined through parameterization of the frequency values. The following limit values apply:

Measured value output	Measured value limit		Comment
	lower	top	
Frequency value	0.095 Hz	5 MHz	with 4-fold evaluation Signal type: "RS422 (diff. input)"
	0.095 Hz	1 MHz	with 4-fold evaluation Signal type: "TTL (single ended)"
	0.095 Hz	100 kHz	with 4-fold evaluation Signal type: "open collector"

The frequency measurement is carried out as described in chapter "Frequency measurement (Frequency value)". In addition, the frequency value can be converted using the two indices [0x80n0:1D](#) [[150](#)] "Frequency numerator" and [0x80n0:1E](#) [[150](#)] "Frequency denominator".

Index (hex)	Name	Meaning	Default
80n0:1D	Frequency numerator	Frequency numerator Factor for normalizing the frequency, e.g. the time unit	0x0000001 (1 _{dec})
80n0:1E	Frequency denominator	Frequency denominator, Factor for normalizing the frequency, e.g. speed calculation	0x0000001 (1 _{dec})

Thus, the frequency can be normalized for application-specific speed measurement. The measured value continues to be output in the process data via "Frequency value" ([0x60n0:13](#) [[152](#)]).

The calculated measured value has the following relationship to the frequency:

$$\text{Determination of measured values} = \text{Frequency} * \frac{\text{Frequency numerator}}{\text{Frequency denominator}}$$

Example for velocity calculation in m/s

- 200 mm travel corresponds to one full mechanical revolution of an encoder.
- The encoder has a 12-bit resolution, i.e. 4096 lines, which corresponds to 4096 periods on track A.

The velocity value is determined as follows:

$$v \left[\frac{\text{mm}}{\text{s}} \right] = \text{Frequency value} \cdot \frac{\text{periods}}{\text{s}} * \frac{200 \text{ mm}}{4096 \text{ periods}}$$

$$v \left[\frac{\text{m}}{\text{s}} \right] = \text{Frequency value} \cdot \frac{\text{periods}}{\text{s}} * \frac{200 \text{ mm}}{4096 \text{ periods}} * \frac{1 \text{ m}}{1000 \text{ mm}}$$

Index (hex)	Name	Example: velocity in m/s	Comment
80n0:1D [150]	Frequency numerator	0x00000C8 (200 _{dec})	Travel path, conversion to m via "Frequency denominator"
80n0:1E [150]	Frequency denominator	0x003E8000 (4096000 _{dec})	Specification of the number of periods over the travel path and conversion of the travel path to m

Example Calculation of speed f_{rot} in revolutions/s

- After one full rotation, 4-fold evaluation (0x80n0:06 [► 150] "Evaluation mode") results in a numerator value of 16384 increments. This corresponds to 4096 periods on track A.
- "Frequency numerator" can be used to convert the time unit into minutes. Note the scaling of the frequency value (0x80n0:13 [► 150] "Frequency scaling"):

Conversion to minutes depending on "Frequency scaling"			
Index (hex)	Entry	Index (hex)	Entry
0x80n0:13 [► 150] Frequency scaling	100 _{dec} : 0.01 Hz	0x80n0:1D [► 150] Frequency numerator	0x00001770 (6000 _{dec})
	1 _{dec} : 1 Hz		0x0000003C (60 _{dec})

$$f_{\text{rot}} \left[\frac{\text{rotations}}{\text{s}} \right] = \text{Frequency value} \frac{\text{periods}}{\text{s}} * \frac{6000 \text{ rotations}}{4096 \text{ periods}}$$

$$f_{\text{rot}} \left[\frac{\text{rotations}}{\text{min}} \right] = \text{Frequency value} \frac{\text{periods}}{\text{s}} * 60 \frac{\text{s}}{\text{min}} * \frac{6000 \text{ rotations}}{4096 \text{ periods}}$$

Index (hex)	Example: Speed f_{rot} in rpm	Comment
80n0:1D [► 150] Frequency numerator	0x0001770 (6000 _{dec})	Output of the value in 0.01 rpm
80n0:1E [► 150] Frequency denominator	0x0001000 (4096 _{dec})	Conversion factor in periods / m

4.2.4.4 Adjustable interference pulse filters

Input filters are used for interference suppression at the encoder and digital inputs. Various filter frequencies can be parameterized for specific applications.

The individual inputs are subject to the following filter frequencies:

Inputs	Max. recommended filter frequency
Encoder Inputs: Track A, Track B	RS422 mode: 5 MHz TTL mode: 1 MHz Open collector: 100 kHz
Input Gate	1 MHz

Filter function sequence

- The filter is disabled on delivery
- The filter can be enabled via index 0x80n0:08 “Disable filter” = FALSE.
- The filter is parameterized via index 0x80n1:19 “Filter settings”. The following filter frequencies are available:

Index 0x80n1:19 “Filter settings”		Default parameters for 0x80n1:1D “Counter mode”	
Setting	Meaning	Setting	Meaning
10 _{dec} : 10 kHz	10 kHz filter		
25 _{dec} : 25 kHz	25 kHz filter		
50 _{dec} : 50 kHz	50 kHz filter		
100 _{dec} : 100 kHz	100 kHz filter	0x80n1:1D “Counter mode”	
		4 _{dec}	Encoder open collector
		5 _{dec}	Counter open collector
250 _{dec} : 250 kHz	250 kHz filter		
500 _{dec} : 500 kHz	500 kHz filter		
1000 _{dec} : 1 MHz	1 MHz filter	0x80n1:1D “Counter mode”	
		2 _{dec}	Encoder TTL (single ended)
		3 _{dec}	Counter TTL (single ended)
2500 _{dec} : 2.5 MHz	2.5 MHz filter		
5000 _{dec} : 5 MHz	5 MHz filter	0x80n1:1D “Counter mode”	
		0 _{dec}	Encoder RS422 (diff. input)
		1 _{dec}	Counter RS422 (diff. input)

- If the filter is parameterized < 1 MHz, it is also active for the “Latch” and “Gate” inputs.
- If a frequency overrun is detected with the activated filter (0x80n0:08 and 0x80n1:19), a counter in index 0xA0n0:16 is incremented.

Index (hex)	Name	Description
0xA0n0:15	Filter violation counter input gate	Filter frequency overshoot counter for the Gate input
0xA0n0:16	Filter violation counter	Filter frequency overshoot counter for the encoder input signals with activated filter

The internal error counters can be reset as follows:

- Terminal transition from “PREOP” to “OP” status

or

- Enter the following in the command object 0xFB00:01 “Request”

0xFB00:01 "Request"	Description
0x9153	Sets the internal error counter for 0xA000:15 "Filter violation counter input gate" for channel 1 to zero
0x9154	Sets the internal error counter for 0xA000:16 "Filter violation counter" for channel 1 to zero
0x9163	Sets the internal error counter for 0xA010:15 "Filter violation counter input gate" for channel 2 to zero
0x9164	Sets the internal error counter for 0xA010:16 "Filter violation counter" for channel 2 to zero

NOTICE**Fast digital inputs – interference from interfering devices**

Please note that the input wiring has very little filtering. It has been optimized for fast signal transmission from the input to the evaluation unit. In other words, rapid level changes/pulses in the μs range and/or high-frequency interference signals from devices (e.g. proportional valves, stepper motor or DC motor output stages) arrive at the evaluation unit almost unfiltered/unattenuated. These interferences can be incorrectly detected as a signal.

- To suppress interference, an additional input filter can be parameterized.
- Furthermore, EMC-compliant cabling and the use of separate power supply units for the terminal and the devices causing interference are recommended.

4.2.4.5 Plausibility check

The plausibility check of the input signals serves as an extended diagnosis to detect interference signals and to identify and suppress the step changes in the counter value caused by them.

Functional principle of the plausibility check

The square wave signals of an incremental encoder with track A and B are phase-shifted by 90°. This means that only certain transitions in the signal curve are permitted or “plausible”, e.g. with a rising A-edge the signal on track B cannot also rise.

The plausibility of the signal sequence is checked in the terminal. If invalid signal transitions occur, these are detected and displayed accordingly if plausibility detection is activated.

Plausibility check sequence

- The plausibility check can be enabled via index 0x80n0:21 “Enable encoder plausibility check”
- If a plausibility error is detected, it is displayed as follows:

Error diagnosis	Description
DiagMessage, type “Error”, text ID 0x8312	Encoder plausibility error (channel n)
0xA0n0:13 “Encoder plausibility error counter”	The error counter is incremented when a plausibility error is detected.
0x60n2:0E TxPDO State = 1	The associated TxPDO data are not valid.

The plausibility error counter can be reset as follows:

- Transition from PREOP to OP

or

- Enter the following in the command object in Index 0xFB00:01 “Request”

0xFB00:01 “Request”	Description
0x9151	Sets the internal error counter 0xA000:13 “Encoder plausibility error counter” for channel 1 to zero
0x9161	Sets the internal error counter 0xA010:13 “Encoder plausibility error counter” for channel 2 to zero

4.2.5 Inputs in two-channel mode

Input functions in 2-channel mode

The number of available inputs depends on the operation mode.

The table provides a brief overview of the ED5112 input functions in 2-channel mode.

The “Latch” and “Gate” inputs each combine gate and latch functions in a single input and are therefore referred to below as gate/latch combination inputs.

Please refer to the detailed function descriptions in the respective chapters.

2-channel mode 2 x AB		
Counter value	PLC variable	Gate/Latch combination inputs [► 130]
Set [► 116]	Enable setting: Output process data “Set counter” (0x70n0:03) = TRUE to the value: Output process data “Set counter value” (0x70n0:11)	Enable setting: Output process data “Set counter on latch extern on positive/negative edge” (0x70n0:0A/0B) = TRUE to the value: Output process data “Set counter value” (0x70n0:11)
Reset [► 115]	—	Enable resetting: 0x80n0:02 “Enable extern reset” to the value: 0x80n1:1B “Reset counter value”
Save [► 118]	—	Enable saving: Output process data “Enable latch extern on positive/negative edge” (0x70n0:02/04) = TRUE Save current counter value in: Input process data “Latch value” (0x60n0:12)
Lock [► 120]	Lock: Output process data “Set software gate” (0x70n0:09) = TRUE	Enable locking with HIGH level: 0x80n0:04 “Gate polarity” = 1 with LOW level: 0x80n0:04 “Gate polarity” = 2

i Simultaneous use of gate and latch in 2-channel mode 2xAB

When using the index [0x80n0:04 \[► 150\]](#) “Gate polarity” (1 = “Enable pos. gate”) and simultaneously activating the bit in the output process data “Enable latch extern on positive edge” (0x70n0:02), a positive edge at the gate/latch combination input causes the current counter value to be initially stored in the input process data “Latch value” (0x60n0:12). After that, the counter value is locked.

The same applies to the use of index 0x80n0:04 “Gate polarity” (2 = “Enable neg. gate”) and the simultaneous activation of the bit in the output process data “Enable latch extern on negative edge” (0x70n0:04) upon a negative edge at the gate input/latch combination input.

4.2.5.1 Gate/Latch combination input

In 2-channel mode 2xAB, there is one external gate/latch combination input available for each channel, designed for 24 V DC signals with a minimum pulse duration of $t_{ON} > 1 \mu s$. This can be used as follows:

- Set counter value: set the counter value to a specified value using a positive or negative edge (output process data "Set counter on latch extern on positive/negative edge")
- Reset counter value: reset the counter value to the value set in index 0x80n1:1B "Reset counter value" (default setting: zero) (index 0x80n0:02 "Enable extern reset")
- Save counter value: save the counter value in separate process data via a positive or negative edge (output process data "Enable latch extern on positive/negative edge")
- Lock counter value: lock the counter value via a positive or negative edge (index 0x80n0:04 "Gate polarity" = "Enable pos./neg. gate")

● Simultaneous use of gate and latch in 2-channel mode 2xAB

I When using the index 0x80n0:04 [► 150] "Gate polarity" (1 = "Enable pos. gate") and simultaneously activating the bit in the output process data "Enable latch extern on positive edge" (0x70n0:02), a positive edge at the gate/latch combination input causes the current counter value to be initially stored in the input process data "Latch value" (0x60n0:12). After that, the counter value is locked.

The same applies to the use of index 0x80n0:04 "Gate polarity" (2 = "Enable neg. gate") and the simultaneous activation of the bit in the output process data "Enable latch extern on negative edge" (0x70n0:04) upon a negative edge at the gate input/latch combination input.

Setting the counter value via the gate/latch combination input (Set counter on latch extern on positive/negative edge)

The counter value can be set to a preset value during runtime via the process data by the positive or negative edge at the gate/latch combination input.

- Setting the counter value via the output process data "Set counter value" (0x70n0:11)
- Activation of the counter value setting via
 - the positive edge at the external gate/latch combination input: output process data "Set counter on latch extern on positive edge" (0x70n0:0A)
 - the negative edge at the external gate/latch combination input: output process data "Set counter on latch extern on negative edge" (0x70n0:0B)
- If the bit (TRUE) is set in the output process data "Set counter on latch extern on positive/negative edge" (0x70n0:0A/0B), the next positive or negative edge at the gate input/latch combination input sets the counter value in the input process data "Counter value" to the specified counter value in the output process data "Set counter value".
- To confirm, the bit in the input process data "Set counter done" (0x60n0:03) is set to TRUE.
- The counter value setting can only be reactivated once the bit in the output process data "Set counter on latch extern on positive/negative edge" (0x70n0:0A/0B) has been set to FALSE.

Reset counter value via gate/latch combination input (Enable extern reset)

The counter value can be set to zero via the external gate/latch combination input.

- Presetting of the reset value via index 0x80n1:1B [► 151] "Reset counter value", (Default: 0)
- To activate this function set the bit in index 0x80n0:02 [► 150] "Enable extern reset".
- Index 0x80n0:10 [► 150] "Extern reset polarity" can be used to specify at which edge the gate/latch combination input is active.
 - 0: "Fall" - the counter is set to zero with a falling edge
 - 1: "Rise" - the counter is set to zero with a rising edge

There is no status message via the process data.

Saving the counter value via a positive/negative edge at the gate/latch combination input (Enable latch extern on positive/negative edge)

- Save the counter value at the external gate/latch combination input via:
 - Output process data “Enable latch extern on positive edge” (0x70n0:02 [► 155]) = TRUE
At the first external latch pulse with positive edge, the current counter value is stored in the input process data “Latch value” (0x60n0:12 [► 152]).
 - Output process data “Enable latch extern on negative edge” (0x70n0:04 [► 155]) = TRUE
At the first external latch pulse with negative edge the current counter value is stored in the input process data “Latch value” (0x60n0:12 [► 152]).
 - Simultaneous activation of the output process data “Enable latch extern on positive/negative edge” (0x70n0:02/04)
The current counter value is saved in the input process data “Latch value” (0x60n0:12) with the first external latch pulse, regardless of the polarity of the edge.
- Specification whether it is necessary to reactivate the command to save the counter value via:
 - “Enable continuous latch extern” Index 0x80n0:22 [► 150] = FALSE
The following pulses at the gate/latch combination input have no effect on the latch value in the process data “Latch value” (0x60n0:12) when the bit in the output process data “Enable latch extern on positive edge” (0x70n0:02 [► 155]) or “Enable latch extern on negative edge” (0x70n0:04 [► 155]) is set.
Only when the bit in the input process data “Latch extern valid” (0x60n0:02 [► 152]) is FALSE can a new counter value be written to the gate/latch combination input in the process data “Latch value” (0x60n0:12).
 - “Enable continuous latch extern” Index 0x80n0:22 [► 150] = TRUE
The counter value is written to process data “Latch value” (0x60n0:12) at every parameterized edge at the gate/latch combination input.
Reactivating the output process data “Enable latch extern on positive edge” (0x70n0:02 [► 155]) or “Enable latch extern on negative edge” (0x70n0:04 [► 155]) is no longer necessary.
- Saving of the count value in the process data “Latch value” (0x60n0:12) is confirmed by the bit in the process data “Latch extern valid” (0x60n0:02).
- The status of the gate/latch combination input can be recorded using the input process data “Status of input gate” (0x60n0:0C).

Lock counter value via a positive/negative edge at the gate/latch combination input (Enable pos./neg. gate)

- The level at the gate/latch combination input at which the counter value is locked during runtime can be specified via index 0x80n0:04 [► 150] “Gate polarity”.
 - 0: Disable gate
The gate/latch combination input is disabled to lock the counter. It can still be used as external latch input for storage.
 - 1: Enable pos. gate
The counter value is locked with HIGH level at the gate/latch combination input.
 - 2: Enable neg. gate
The counter value is locked with LOW level at the gate/latch combination input
- The current level at the gate/latch combination input is displayed via the input process data “Status of input gate” (0x60n0:0C [► 152]).

4.3 Diagnostics

4.3.1 Diagnostics - basic principles of diag messages

DiagMessages designates a system for the transmission of messages from the EtherCAT Slave to the EtherCAT Master/TwinCAT. The messages are stored by the device in its own CoE under 0x10F3 and can be read by the application or the System Manager. An error message referenced via a code is output for each event stored in the device (warning, error, status change).

Definition

The *DiagMessages* system is defined in the ETG (EtherCAT Technology Group) in the guideline ETG.1020, chapter 13 "Diagnosis handling". It is used so that pre-defined or flexible diagnostic messages can be conveyed from the EtherCAT Slave to the Master. In accordance with the ETG, the process can therefore be implemented supplier-independently. Support is optional. The firmware can store up to 250 *DiagMessages* in its own CoE.

Each *DiagMessage* consists of

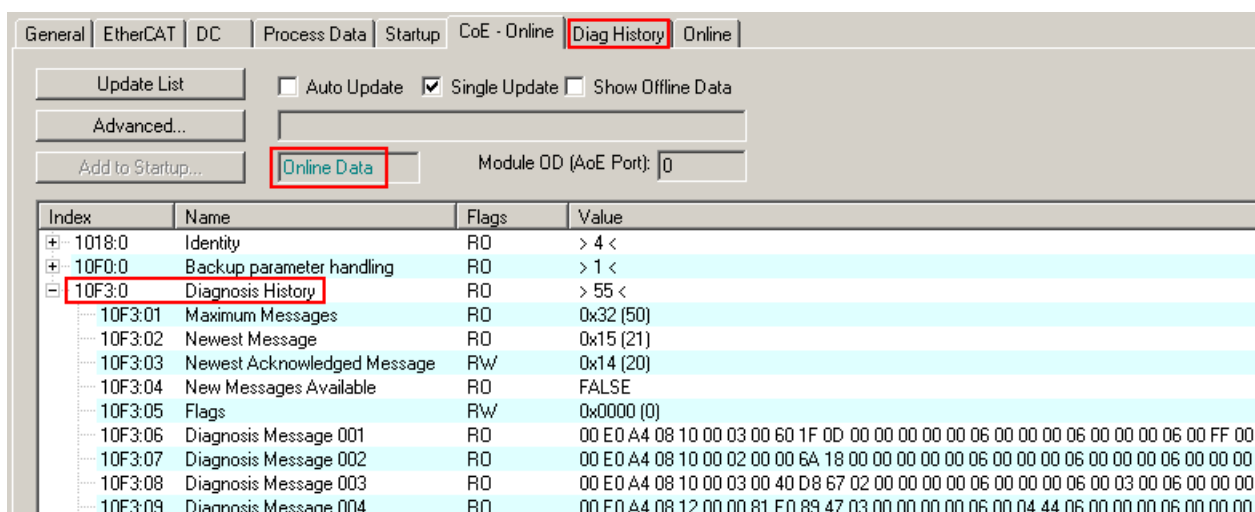
- Diag Code (4-byte)
- Flags (2-byte; info, warning or error)
- Text ID (2-byte; reference to explanatory text from the ESI/XML)
- Timestamp (8-byte, local slave time or 64-bit Distributed Clock time, if available)
- Dynamic parameters added by the firmware

The *DiagMessages* are explained in text form in the ESI/XML file belonging to the EtherCAT device: on the basis of the Text ID contained in the *DiagMessage*, the corresponding plain text message can be found in the languages contained in the ESI/XML. In the case of Beckhoff products these are usually German and English.

Via the entry *NewMessagesAvailable* the user receives information that new messages are available.

DiagMessages can be confirmed in the device: the last/latest unconfirmed message can be confirmed by the user.

In the CoE both the control entries and the history itself can be found in the CoE object 0x10F3:



Index	Name	Flags	Value
1018:0	Identity	RO	> 4 <
10F0:0	Backup parameter handling	RO	> 1 <
10F3:0	Diagnosis History	RO	> 55 <
10F3:01	Maximum Messages	RO	0x32 (50)
10F3:02	Newest Message	RO	0x15 (21)
10F3:03	Newest Acknowledged Message	R/W	0x14 (20)
10F3:04	New Messages Available	RO	FALSE
10F3:05	Flags	R/W	0x0000 (0)
10F3:06	Diagnosis Message 001	RO	00 E0 A4 08 10 00 03 00 60 1F 0D 00 00 00 00 00 06 00 00 00 06 00 00 00 06 00 FF 00
10F3:07	Diagnosis Message 002	RO	00 E0 A4 08 10 00 02 00 00 6A 18 00 00 00 00 00 06 00 00 00 06 00 00 00 06 00 00 00
10F3:08	Diagnosis Message 003	RO	00 E0 A4 08 10 00 03 00 40 D8 67 02 00 00 00 00 06 00 00 00 06 00 03 00 06 00 00 00
10F3:09	Diagnosis Message 004	RO	00 E0 A4 08 12 00 00 81 E0 89 47 03 00 00 00 00 06 00 04 44 06 00 00 00 06 00 00 00

Fig. 56: *DiagMessages* in the CoE

The subindex of the latest *DiagMessage* can be read under 0x10F3:02.

Support for commissioning

The *DiagMessages* system is to be used above all during the commissioning of the plant. The diagnostic values e.g. in the StatusWord of the device (if available) are helpful for online diagnosis during the subsequent continuous operation.

TwinCAT System Manager implementation

From TwinCAT 2.11 DiagMessages, if available, are displayed in the device's own interface. Operation (collection, confirmation) also takes place via this interface.

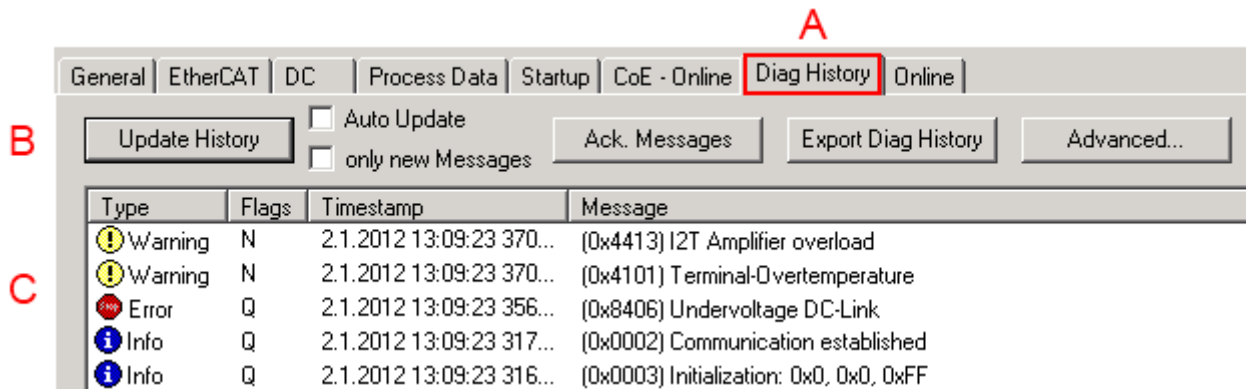


Fig. 57: Implementation of the DiagMessage system in the TwinCAT System Manager

The operating buttons (B) and the history read out (C) can be seen on the Diag History tab (A). The components of the message:

- Info/Warning/Error
- Acknowledge flag (N = unconfirmed, Q = confirmed)
- Time stamp
- Text ID
- Plain text message according to ESI/XML data

The meanings of the buttons are self-explanatory.

DiagMessages within the ADS Logger/Eventlogger

From TwinCAT 3.1 build 4022 onwards, DiagMessages sent by the terminal are shown by the TwinCAT ADS Logger. Given that DiagMessages are represented IO- comprehensive at one place, commissioning will be simplified. In addition, the logger output could be stored into a data file – hence DiagMessages are available long-term for analysis.

DiagMessages are actually only available locally in CoE 0x10F3 in the terminal and can be read out manually if required, e.g. via the DiagHistory mentioned above.

In the latest developments, the EtherCAT Terminals are set by default to report the presence of a DiagMessage as emergency via EtherCAT; the event logger can then retrieve the DiagMessage. The function is activated in the terminal via 0x10F3:05, so such terminals have the following entry in the StartUp list by default:

General EtherCAT Settings Filter DC Process Data Plc Startup CoE - Online Diag History Online					
Transition	Protocol	Index	Data	Comment	
<PS>	CoE	0x1C12 C 0	00 00	download pdo 0x1C12 index	
<PS>	CoE	0x1C13 C 0	05 00 00 1A 01 1A 10 1A ...	download pdo 0x1C13 index	
IP	CoE	0x10F3:05	0x0001 (1)		

Fig. 58: Startup List

If the function is to be deactivated because, for example, many messages come in or the EventLogger is not used, the StartUp entry can be deleted or set to 0. The value can then be set back to 1 later from the PLC via CoE access if required.

Reading messages into the PLC

- In preparation -

Interpretation

Time stamp

The time stamp is obtained from the local clock of the terminal at the time of the event. The time is usually the distributed clock time (DC) from register x910.

Please note: When EtherCAT is started, the DC time in the reference clock is set to the same time as the local IPC/TwinCAT time. From this moment the DC time may differ from the IPC time, since the IPC time is not adjusted. Significant time differences may develop after several weeks of operation without a EtherCAT restart. As a remedy, external synchronization of the DC time can be used, or a manual correction calculation can be applied, as required: The current DC time can be determined via the EtherCAT master or from register x901 of the DC slave.

Structure of the Text ID

The structure of the MessageID is not subject to any standardization and can be supplier-specifically defined. In the case of Beckhoff EtherCAT devices (EL, EP) it usually reads according to **xyzz**:

x	y	zz
0: Systeminfo 2: reserved 1: Info 4: Warning 8: Error	0: System 1: General 2: Communication 3: Encoder 4: Drive 5: Inputs 6: I/O general 7: reserved	Error number

Example: Message 0x4413 --> Drive Warning Number 0x13

Overview of text IDs

Specific text IDs are listed in the device documentation.

Text ID	Type	Place	Text Message	Additional comment
0x0001	Information	System	No error	No error
0x0002	Information	System	Communication established	Connection established
0x0003	Information	System	Initialization: 0x%X, 0x%X, 0x%X	General information; parameters depend on event. See device documentation for interpretation.
0x1000	Information	System	Information: 0x%X, 0x%X, 0x%X	General information; parameters depend on event. See device documentation for interpretation.
0x1012	Information	System	EtherCAT state change Init - PreOp	
0x1021	Information	System	EtherCAT state change PreOp - Init	
0x1024	Information	System	EtherCAT state change PreOp - Safe-Op	
0x1042	Information	System	EtherCAT state change SafeOp - PreOp	
0x1048	Information	System	EtherCAT state change SafeOp - Op	
0x1084	Information	System	EtherCAT state change Op - SafeOp	
0x1100	Information	General	Detection of operation mode completed: 0x%X, %d	Detection of the mode of operation ended
0x1135	Information	General	Cycle time o.k.: %d	Cycle time OK
0x1157	Information	General	Data manually saved (Idx: 0x%X, SubIdx: 0x%X)	Data saved manually
0x1158	Information	General	Data automatically saved (Idx: 0x%X, SubIdx: 0x%X)	Data saved automatically
0x1159	Information	General	Data deleted (Idx: 0x%X, SubIdx: 0x%X)	Data deleted
0x117F	Information	General	Information: 0x%X, 0x%X, 0x%X	Information
0x1201	Information	Communication	Communication re-established	Communication to the field side restored This message appears, for example, if the voltage was removed from the power contacts and re-applied during operation.
0x1300	Information	Encoder	Position set: %d, %d	Position set - StartInputHandler
0x1303	Information	Encoder	Encoder Supply ok	Encoder power supply unit OK
0x1304	Information	Encoder	Encoder initialization successfully, channel: %X	Encoder initialization successfully completed
0x1305	Information	Encoder	Sent command encoder reset, channel: %X	Send encoder reset command
0x1400	Information	Drive	Drive is calibrated: %d, %d	Drive is calibrated
0x1401	Information	Drive	Actual drive state: 0x%X, %d	Current drive status
0x1705	Information		CPU usage returns in normal range (< 85%%)	Processor load is back in the normal range
0x1706	Information		Channel is not in saturation anymore	Channel is no longer in saturation
0x1707	Information		Channel is not in overload anymore	Channel is no longer overloaded
0x170A	Information		No channel range error anymore	A measuring range error is no longer active
0x170C	Information		Calibration data saved	Calibration data were saved
0x170D	Information		Calibration data will be applied and saved after sending the command "0x5AFE"	Calibration data are not applied and saved until the command "0x5AFE" is sent.

Text ID	Type	Place	Text Message	Additional comment
0x2000	Information	System	%s: %s	
0x2001	Information	System	%s: Network link lost	Network connection lost
0x2002	Information	System	%s: Network link detected	Network connection found
0x2003	Information	System	%s: no valid IP Configuration - Dhcp client started	Invalid IP configuration
0x2004	Information	System	%s: valid IP Configuration (IP: %d.%d.%d.%d) assigned by Dhcp server %d.%d.%d.%d	Valid IP configuration, assigned by the DHCP server
0x2005	Information	System	%s: Dhcp client timed out	DHCP client timeout
0x2006	Information	System	%s: Duplicate IP Address detected (%d.%d.%d.%d)	Duplicate IP address found
0x2007	Information	System	%s: UDP handler initialized	UDP handler initialized
0x2008	Information	System	%s: TCP handler initialized	TCP handler initialized
0x2009	Information	System	%s: No more free TCP sockets available	No free TCP sockets available.

Text ID	Type	Place	Text Message	Additional comment
0x4000	Warning		Warning: 0x%X, 0x%X, 0x%X	General warning; parameters depend on event. See device documentation for interpretation.
0x4001	Warning	System	Warning: 0x%X, 0x%X, 0x%X	
0x4002	Warning	System	%s: %s Connection Open (IN:%d OUT:%d API:%dms) from %d. %d.%d.%d successful	
0x4003	Warning	System	%s: %s Connection Close (IN:%d OUT:%d) from %d.%d.%d.%d successful	
0x4004	Warning	System	%s: %s Connection (IN:%d OUT:%d) with %d.%d.%d.%d timed out	
0x4005	Warning	System	%s: %s Connection Open (IN:%d OUT:%d) from %d.%d.%d.%d denied (Error: %u)	
0x4006	Warning	System	%s: %s Connection Open (IN:%d OUT:%d) from %d.%d.%d.%d denied (Input Data Size expected: %d Byte(s) received: %d Byte(s))	
0x4007	Warning	System	%s: %s Connection Open (IN:%d OUT:%d) from %d.%d.%d.%d denied (Output Data Size expected: %d Byte(s) received: %d Byte(s))	
0x4008	Warning	System	%s: %s Connection Open (IN:%d OUT:%d) from %d.%d.%d.%d denied (RPI:%dms not supported -> API:%dms)	
0x4101	Warning	General	Terminal-Overtemperature	Overtemperature. The internal temperature of the terminal exceeds the parameterized warning threshold.
0x4102	Warning	General	Discrepancy in the PDO-Configuration	The selected PDOs do not match the set operating mode. Sample: Drive operates in velocity mode, but the velocity PDO is but not mapped in the PDOs.
0x417F	Warning	General	Warning: 0x%X, 0x%X, 0x%X	
0x428D	Warning	General	Challenge is not Random	
0x4300	Warning	Encoder	Subincrements deactivated: %d, %d	Sub-increments deactivated (despite activated configuration)
0x4301	Warning	Encoder	Encoder-Warning	General encoder error
0x4302	Warning	Encoder	Maximum frequency of the input signal is nearly reached (channel %d)	
0x4303	Warning	Encoder	Limit counter value was reduced because of the PDO configuration (channel %d)	
0x4304	Warning	Encoder	Reset counter value was reduced because of the PDO configuration (channel %d)	
0x4400	Warning	Drive	Drive is not calibrated: %d, %d	Drive is not calibrated
0x4401	Warning	Drive	Starttype not supported: 0x%X, %d	Start type is not supported
0x4402	Warning	Drive	Command rejected: %d, %d	Command rejected
0x4405	Warning	Drive	Invalid modulo subtype: %d, %d	Modulo sub-type invalid
0x4410	Warning	Drive	Target overrun: %d, %d	Target position exceeded
0x4411	Warning	Drive	DC-Link undervoltage (Warning)	The DC link voltage of the terminal is lower than the parameterized minimum voltage. Activation of the output stage is prevented.
0x4412	Warning	Drive	DC-Link overvoltage (Warning)	The DC link voltage of the terminal is higher than the parameterized maximum voltage. Activation of the output stage is prevented.
0x4413	Warning	Drive	I2T-Model Amplifier overload (Warning)	- The amplifier is being operated outside the specification. - The I2T-model of the amplifier is incorrectly parameterized.
0x4414	Warning	Drive	I2T-Model Motor overload (Warning)	The motor is being operated outside the parameterized rated values.

Text ID	Type	Place	Text Message	Additional comment
				The I2T-model of the motor is incorrectly parameterized.
0x4415	Warning	Drive	Speed limitation active	The maximum speed is limited by the parameterized objects (e.g. velocity limitation, motor speed limitation). This warning is output if the set velocity is higher than one of the parameterized limits.
0x4416	Warning	Drive	Step lost detected at position: 0x%X%X	Step loss detected
0x4417	Warning	Drive	Motor overtemperature	The internal temperature of the motor exceeds the parameterized warning threshold
0x4418	Warning	Drive	Limit: Current	Limit: current is limited
0x4419	Warning	Drive	Limit: Amplifier I2T-model exceeds 100%%	The threshold values for the maximum current were exceeded.
0x441A	Warning	Drive	Limit: Motor I2T-model exceeds 100%%	Limit: Motor I2T-model exceeds 100%
0x441B	Warning	Drive	Limit: Velocity limitation	The threshold values for the maximum speed were exceeded.
0x441C	Warning	Drive	STO while the axis was enabled	An attempt was made to activate the axis, despite the fact that no voltage is present at the STO input.
0x4600	Warning	General IO	Wrong supply voltage range	Supply voltage not in the correct range
0x4610	Warning	General IO	Wrong output voltage range	Output voltage not in the correct range
0x4705	Warning		Processor usage at %d %%	Processor load at %d %%
0x470A	Warning		EtherCAT Frame missed (change Settings or DC Operation Mode or Sync0 Shift Time)	EtherCAT frame missed (change DC Operation Mode or Sync0 Shift Time under Settings)

Text ID	Type	Place	Text Message	Additional comment
0x8000	Error	System	%s: %s	
0x8001	Error	System	Error: 0x%X, 0x%X, 0x%X	General error; parameters depend on event. See device documentation for interpretation.
0x8002	Error	System	Communication aborted	Communication aborted
0x8003	Error	System	Configuration error: 0x%X, 0x%X, 0x%X	General; parameters depend on event. See device documentation for interpretation.
0x8004	Error	System	%s: Unsuccessful FwdOpen-Response received from %d.%d.%d (%s) (Error: %u)	
0x8005	Error	System	%s: FwdClose-Request sent to %d.%d.%d (%s)	
0x8006	Error	System	%s: Unsuccessful FwdClose-Response received from %d.%d.%d (%s) (Error: %u)	
0x8007	Error	System	%s: Connection with %d.%d.%d (%s) closed	
0x8100	Error	General	Status word set: 0x%X, %d	Error bit set in the status word
0x8101	Error	General	Operation mode incompatible to PDO interface: 0x%X, %d	Mode of operation incompatible with the PDO interface
0x8102	Error	General	Invalid combination of Inputs and Outputs PDOs	Invalid combination of input and output PDOs
0x8103	Error	General	No variable linkage	No variables linked
0x8104	Error	General	Terminal-Overtemperature	The internal temperature of the terminal exceeds the parameterized error threshold. Activation of the terminal is prevented
0x8105	Error	General	PD-Watchdog	Communication between the fieldbus and the output stage is secured by a Watchdog. The axis is stopped automatically if the fieldbus communication is interrupted. - The EtherCAT connection was interrupted during operation. - The Master was switched to Config mode during operation.
0x8135	Error	General	Cycle time has to be a multiple of 125 µs	The IO or NC cycle time divided by 125 µs does not produce a whole number.
0x8136	Error	General	Configuration error: invalid sampling rate	Configuration error: Invalid sampling rate
0x8137	Error	General	Electronic type plate: CRC error	Content of the external name plate memory invalid.
0x8140	Error	General	Sync Error	Real-time violation
0x8141	Error	General	Sync%X Interrupt lost	Sync%X Interrupt lost
0x8142	Error	General	Sync Interrupt asynchronous	Sync Interrupt asynchronous
0x8143	Error	General	Jitter too big	Jitter limit violation
0x817F	Error	General	Error: 0x%X, 0x%X, 0x%X	
0x8200	Error	Communication	Write access error: %d, %d	Error while writing
0x8201	Error	Communication	No communication to field-side (Auxiliary voltage missing)	- There is no voltage applied to the power contacts. - A firmware update has failed.
0x8281	Error	Communication	Ownership failed: %X	
0x8282	Error	Communication	To many Keys founded	
0x8283	Error	Communication	Key Creation failed: %X	
0x8284	Error	Communication	Key loading failed	
0x8285	Error	Communication	Reading Public Key failed: %X	
0x8286	Error	Communication	Reading Public EK failed: %X	
0x8287	Error	Communication	Reading PCR Value failed: %X	
0x8288	Error	Communication	Reading Certificate EK failed: %X	
0x8289	Error	Communication	Challenge could not be hashed: %X	
0x828A	Error	Communication	Tickstamp Process failed	
0x828B	Error	Communication	PCR Process failed: %X	
0x828C	Error	Communication	Quote Process failed: %X	
0x82FF	Error	Communication	Bootmode not activated	Boot mode not activated
0x8300	Error	Encoder	Set position error: 0x%X, %d	Error while setting the position

Text ID	Type	Place	Text Message	Additional comment
0x8301	Error	Encoder	Encoder increments not configured: 0x%X, %d	Encoder increments not configured
0x8302	Error	Encoder	Encoder error	The amplitude of the resolver is too small
0x8303	Error	Encoder	Encoder power missing (channel %d)	
0x8304	Error	Encoder	Encoder communication error, channel: %X	Encoder communication error
0x8305	Error	Encoder	EnDat2.2 is not supported, channel: %X	EnDat2.2 is not supported
0x8306	Error	Encoder	Delay time, tolerance limit exceeded, 0x%X, channel: %X	Runtime measurement, tolerance exceeded
0x8307	Error	Encoder	Delay time, maximum value exceeded, 0x%X, channel: %X	Runtime measurement, maximum value exceeded
0x8308	Error	Encoder	Unsupported ordering designation, 0x%X, channel: %X (only 02 and 22 is supported)	Wrong EnDat order ID
0x8309	Error	Encoder	Encoder CRC error, channel: %X	Encoder CRC error
0x830A	Error	Encoder	Temperature %X could not be read, channel: %X	Temperature cannot be read
0x830C	Error	Encoder	Encoder Single-Cycle-Data Error, channel: %X	CRC error detected. Check the transmission path and the CRC polynomial
0x830D	Error	Encoder	Encoder Watchdog Error, channel: %X	The sensor has not responded within a predefined time period
0x8310	Error	Encoder	Initialisation error	
0x8311	Error	Encoder	Maximum frequency of the input signal is exceeded (channel %d)	
0x8312	Error	Encoder	Encoder plausibility error (channel %d)	
0x8313	Error	Encoder	Configuration error (channel %d)	
0x8314	Error	Encoder	Synchronisation error	
0x8315	Error	Encoder	Error status input (channel %d)	
0x8400	Error	Drive	Incorrect drive configuration: 0x%X, %d	Drive incorrectly configured
0x8401	Error	Drive	Limiting of calibration velocity: %d, %d	Limitation of the calibration velocity
0x8402	Error	Drive	Emergency stop activated: 0x%X, %d	Emergency stop activated
0x8403	Error	Drive	ADC Error	Error during current measurement in the ADC
0x8404	Error	Drive	Overcurrent	Overcurrent in phase U, V or W
0x8405	Error	Drive	Invalid modulo position: %d	Modulo position invalid
0x8406	Error	Drive	DC-Link undervoltage (Error)	The DC link voltage of the terminal is lower than the parameterized minimum voltage. Activation of the output stage is prevented.
0x8407	Error	Drive	DC-Link overvoltage (Error)	The DC link voltage of the terminal is higher than the parameterized maximum voltage. Activation of the output stage is prevented.
0x8408	Error	Drive	I2T-Model Amplifier overload (Error)	- The amplifier is being operated outside the specification. - The I2T-model of the amplifier is incorrectly parameterized.
0x8409	Error	Drive	I2T-Model motor overload (Error)	- The motor is being operated outside the parameterized rated values. - The I2T-model of the motor is incorrectly parameterized.
0x840A	Error	Drive	Overall current threshold exceeded	Total current exceeded
0x8415	Error	Drive	Invalid modulo factor: %d	Modulo factor invalid
0x8416	Error	Drive	Motor overtemperature	The internal temperature of the motor exceeds the parameterized error threshold. The motor stops immediately. Activation of the output stage is prevented.
0x8417	Error	Drive	Maximum rotating field velocity exceeded	Rotary field speed exceeds the value specified for dual use (EU 1382/2014).
0x841C	Error	Drive	STO while the axis was enabled	An attempt was made to activate the axis, despite the fact that no voltage is present at the STO input.

Text ID	Type	Place	Text Message	Additional comment
0x8550	Error	Inputs	Zero crossing phase %X missing	Zero crossing phase %X missing
0x8551	Error	Inputs	Phase sequence Error	Wrong direction of rotation
0x8552	Error	Inputs	Overcurrent phase %X	Overcurrent phase %X
0x8553	Error	Inputs	Overcurrent neutral wire	Overcurrent neutral wire
0x8581	Error	Inputs	Wire broken Ch %D	Wire broken Ch %d
0x8600	Error	General IO	Wrong supply voltage range	Supply voltage not in the correct range
0x8601	Error	General IO	Supply voltage to low	Supply voltage too low
0x8602	Error	General IO	Supply voltage to high	Supply voltage too high
0x8603	Error	General IO	Over current of supply voltage	Overcurrent of supply voltage
0x8610	Error	General IO	Wrong output voltage range	Output voltage not in the correct range
0x8611	Error	General IO	Output voltage to low	Output voltage too low
0x8612	Error	General IO	Output voltage to high	Output voltage too high
0x8613	Error	General IO	Over current of output voltage	Overcurrent of output voltage
0x8700	Error		Channel/Interface not calibrated	Channel/interface not synchronized
0x8701	Error		Operating time was manipulated	Operating time was manipulated
0x8702	Error		Oversampling setting is not possible	Oversampling setting not possible
0x8703	Error		No slave controller found	No slave controller found
0x8704	Error		Slave controller is not in Bootstrap	Slave controller is not in bootstrap
0x8705	Error		Processor usage to high (>= 100%%)	Processor load too high (>= 100%%)
0x8706	Error		Channel in saturation	Channel in saturation
0x8707	Error		Channel overload	Channel overload
0x8708	Error		Overloadtime was manipulated	Overload time was manipulated
0x8709	Error		Saturationtime was manipulated	Saturation time was manipulated
0x870A	Error		Channel range error	Measuring range error for the channel
0x870B	Error		no ADC clock	No ADC clock available
0xFFFF	Information		Debug: 0x%X, 0x%X, 0x%X	Debug: 0x%X, 0x%X, 0x%X

4.3.2 ED5112 – Diagnostics

The following diagnostic options are available:

- [Overflow and underflow of the counter limits \[► 142\]](#)
- [RS422 - wire break detection and short-circuit detection \(open circuit\) \[► 143\]](#)
- [Monitoring of the encoder operating voltage \[► 144\]](#)
- [Diagnostics for the input "Digital input" \[► 144\]](#)
- [Plausibility check \[► 145\]](#)
- [Filter frequency overshoot \[► 146\]](#)

4.3.2.1 Counter overflow and underflow

An overflow or underflow of the counter limits is indicated by the process data "Counter underflow" (0x60n0:04) or "Counter overflow" (0x60n0:05).

- The bit in the process data "Counter underflow" (0x60n0:04) is set when an underflow occurs 0x80n1:1B "Reset counter value" → 0x80n1:1A "Limit counter value". With default parameters this corresponds to "..00 → ..FF"
It is reset if 2/3 of the counting range are underrun.
- The bit in the process data "Counter overflow" (0x60n0:05) is set when an overflow occurs 0x80n1:1A "Limit counter value" → 0x80n1:1B "Reset counter value". With default parameters "..FF → ..00"
It is reset if 1/3 of the counter range is exceeded.

4.3.2.2 RS422 - wire break and short-circuit detection (open circuit)

In the "RS422 (diff. input)" modes it is possible to detect a wire break or short circuit at the individual encoder inputs.

- In case of wire break, e.g. between input A and input $\bar{A}$,
 - the differential voltage V_{ID} is almost 0 V,
 - which leads to an error with low differential voltage.
- In case of a short circuit, e.g. between input A and input $\bar{A}$, the error behavior is similar to a wire break and also leads to error detection.

Activation of error detection for each channel			
Index (hex)	Name	Description	
80n0:0B *	Error detection A	TRUE	Broken wire and short circuit detection for encoder input A enabled
		FALSE	Broken wire and short circuit detection for encoder input A disabled
80n0:0C *	Error detection B	TRUE	Broken wire and short circuit detection for encoder input B enabled
		FALSE	Broken wire and short circuit detection for encoder input B disabled
80n0:0D *	Error detection C	TRUE	Broken wire and short circuit detection for encoder input C enabled
		FALSE	Broken wire and short circuit detection for encoder input C disabled
*) depending on the number of channels (n = 0 for channel 1 and n = 1 for channel 2)			

Error detection using the example of a wire break or short circuit between inputs A and $\bar{A}$.		
Error diagnosis	Display	Description
LED Ch. 1 A	Green	A TRUE level is present
	Red	An error (open circuit) was detected
0x60n0:07 „Open circuit“	TRUE	Aggregate error message for "Open circuit" A wire break or short circuit has occurred at one of the encoder inputs
	FALSE	There is no "Open circuit" error.
0x60n0:0F „TxPDO State“	TRUE	The position data are invalid.
	FALSE	The position data are valid.
0xA0n0:01 „Error A“	TRUE	An "Open circuit" error (wire break or short circuit) has occurred at encoder input A.
	FALSE	There is no "Open circuit" error.
Diag Message	Text ID: 0x831B	Wire break or short circuit track A (channel n)

● Error bits not permanently set in case of wire break at an encoder input

i If a wire break is only present at one encoder input (e.g. only track A), it may happen in individual cases that the differential voltage (V_{ID}) is above the limit range (V_{IDLow}) due to the applied common mode voltage (V_{CM}).

This means that the error is not clearly identified.

The corresponding error bits ("Open circuit" and "Error A") are not permanently present!

4.3.2.3 Monitoring of the encoder operating voltage

A lack of encoder operating voltage is indicated by:

Error diagnosis	Display	Description
LED Enc. Supply	green	Encoder supply voltage is present
	off	Encoder supply voltage is not present
0xA0n0:04 „Field power failure“	TRUE	Encoder supply voltage is not present
	FALSE	Encoder supply voltage is present
DiagMessage, text ID	0x8303	Encoder supply voltage is not present

NOTICE

Encoder operating voltage generated from the 24 V DC power contacts

The encoder operating voltage is generated from the 24 V DC supply of the power contacts. If the power contacts have no supply, no encoder operating voltage can be provided.

4.3.2.4 Diagnostics for the input “Digital input”

If the encoder has an alarm or status output, in 1-channel mode this can be connected to the “Digital input” of the terminal and evaluated. The input is 5 V compatible.

The alarm or status output at the encoder is usually implemented with negative logic. This is indicated by the terminal as follows:

Encoder	ED5112 (1-channel mode)		
Alarm output	“Digital input” (0x60n0:06 “Status of input status”)	LED “Ch. 1 DI”	Meaning
HIGH level / output open	TRUE	off	e.g. encoder OK
LOW level / PullDown - level is actively pulled down to LOW	FALSE	red	e.g. encoder malfunction

If an overvoltage is present at the “Digital input” input, it is displayed as follows:

Fault diagnosis in case of overvoltage at the “Digital input” at channel n	Display
DiagMessage, type “Error”, text ID 0x8315	Error status input (channel n)
0xA0n0:05 “Error input status”	TRUE
LED: Ch. 1 DI	red

4.3.2.5 Plausibility check

The plausibility check of the input signals serves as an extended diagnosis to detect interference signals and to identify and suppress the step changes in the counter value caused by them.

Functional principle of the plausibility check

The square wave signals of an incremental encoder with track A and B are phase-shifted by 90°. This means that only certain transitions in the signal curve are permitted or “plausible”, e.g. with a rising A-edge the signal on track B cannot also rise.

The plausibility of the signal sequence is checked in the terminal. If invalid signal transitions occur, these are detected and displayed accordingly if plausibility detection is activated.

Plausibility check sequence

- The plausibility check can be enabled via index 0x80n0:21 “Enable encoder plausibility check”
- If a plausibility error is detected, it is displayed as follows:

Error diagnosis	Description
DiagMessage, type “Error”, text ID 0x8312	Encoder plausibility error (channel n)
0xA0n0:13 “Encoder plausibility error counter”	The error counter is incremented when a plausibility error is detected.
0x60n2:0E TxPDO State = 1	The associated TxPDO data are not valid.

The plausibility error counter can be reset as follows:

- Transition from PREOP to OP

or

- Enter the following in the command object in Index 0xFB00:01 “Request”

0xFB00:01 “Request”	Description
0x9151	Sets the internal error counter 0xA000:13 “Encoder plausibility error counter” for channel 1 to zero
0x9161	Sets the internal error counter 0xA010:13 “Encoder plausibility error counter” for channel 2 to zero

4.3.2.6 Filter frequency overshoot

Input filters are used for interference suppression at the encoder and digital inputs. Different filter frequencies can be parameterized according to the application.

The individual inputs are subject to the following filter frequencies:

Inputs	Max. recommended filter frequency
Encoder Inputs: Track A, Track B, Track C	RS422 mode: 5 MHz TTL mode: 1 MHz Open collector: 100 kHz
Latch input	1 MHz
Gate input	1 MHz
Digital input	100 kHz (not adjustable)

- If a frequency overrun is detected with the activated filter (0x80n0:08 and 0x80n1:19), a counter in index 0xA0n0:16 is incremented.

Index (hex)	Name	Description
0xA0n0:14	Filter violation counter extern latch	Filter frequency overshoot counter for the "Latch extern" input
0xA0n0:15	Filter violation counter input gate	Filter frequency overshoot counter for the Gate input
0xA0n0:16	Filter violation counter	Filter frequency overshoot counter for the encoder input signals with activated filter

NOTICE



Note Parameterization of adjustable interference pulse filters

Please note the description and notes for parameterization in chapter "[Adjustable interference pulse filters \[► 87\]](#)".

4.3.2.7 LED status via CoE 0xF915

The status of the LEDs can be read electronically via CoE object 0xF915:0. The status of the LEDs is displayed as a 32-bit value. The value is interpreted as follows.

- Byte 1 indicates the flashing/lighting code with
 - 0x00: LED off
 - 0x01 to 0x82: flashing codes
 - 0xFF: LED on
- Byte 4 (R), byte 3 (G) to byte 2 (B) specify the color as an RGB code.

Byte 1 (flashing code)	Byte 2 blue (B)	Byte 3 green (G)	Byte 4 red (R)	Meaning
0x00	00	00	00	LED not present
0x00	FF	00	00	LED is off (blue)
0x00	00	FF	00	LED is off (green) • Run LED: EtherCAT State Machine: INIT • Signal LED: No signal at the input/output
0x00	00	00	FF	LED is off (red) • Error LED: No error at the input/output
0x00	00	FF	FF	LED is off (yellow)
0x00	FF	FF	FF	LED is off (white)
0x01 to 0x14	00	FF	00	LED flashes at 1 Hz to 20 Hz (green)
0x80	00	FF	00	Run LED flashing uniformly (green): EtherCAT State Machine: PREOP
0x81	00	FF	00	Run LED flashing slowly (green): EtherCAT State Machine: SAFEOP
0x82	00	FF	00	Run LED flashing quickly (green): EtherCAT State Machine: BOOT
0xFF	FF	00	00	LED is on (blue)
0xFF	00	FF	00	LED on (green) • Run LED: EtherCAT State Machine: OP • Signal LED: Signal at the input/output
0xFF	00	00	FF	LED is on (red) • Error LED: Error at input/output
0xFF	00	FF	FF	LED is on (yellow)
0xFF	FF	FF	FF	LED is on (white)

LED status using the ED5112 as an example

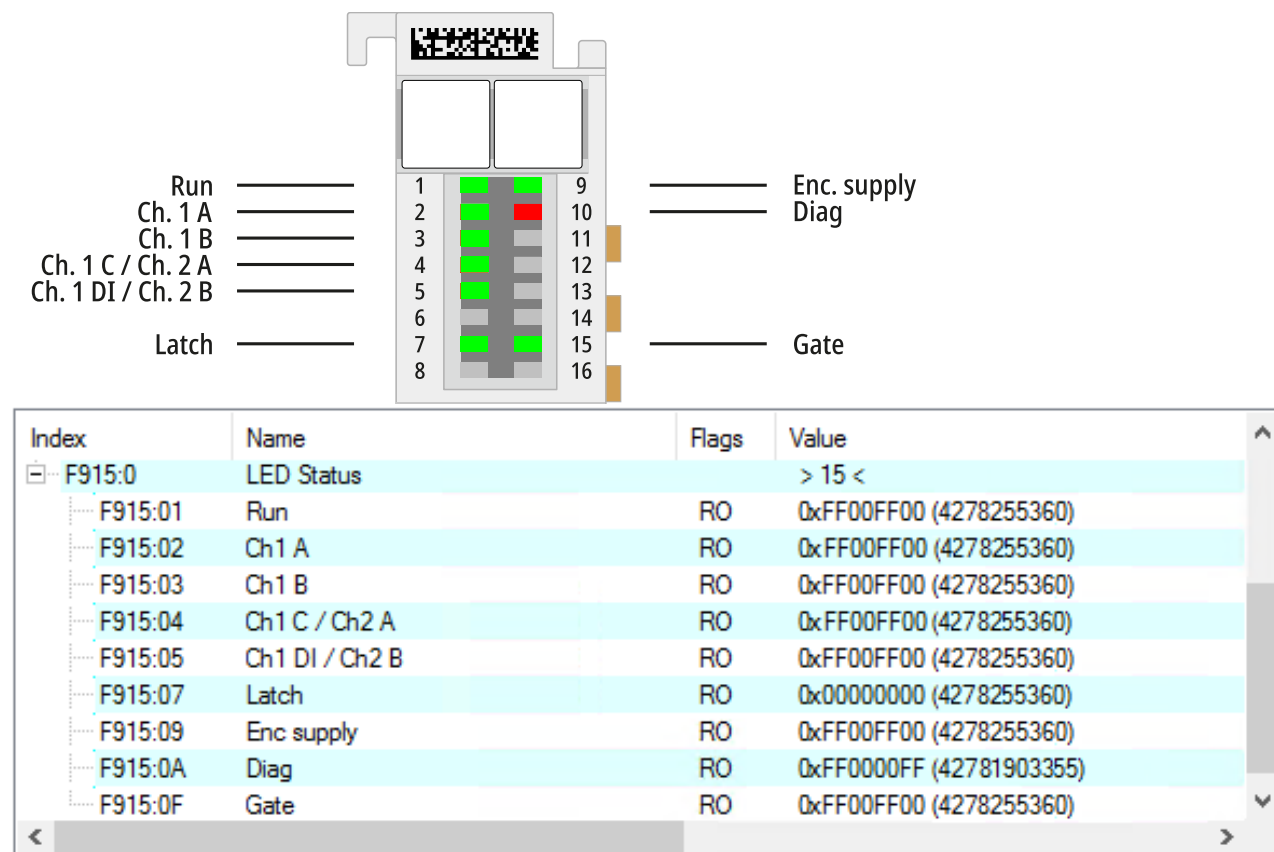


Fig. 59: ED5112 display with the corresponding CoE values in index 0xF915:0

4.4 Object description



EtherCAT XML Device Description

The display matches that of the CoE objects from the EtherCAT XML Device Description. We recommend downloading the latest XML file from the download area of the Beckhoff website and installing it according to installation instructions.

NOTICE



Parameterization via the CoE list (CAN over EtherCAT)

The EtherCAT device is parameterized via the CoE - Online tab (with a double click on the respective object) or via the Process Data tab (assignment of PDOs). A detailed description can be found in the EtherCAT System-Documentation in chapter “EtherCAT subscriber configuration”

Please note the general CoE notes in the EtherCAT System Documentation in chapter “CoE-interface” when using/manipulating the CoE parameters:

- Keep a startup list if components have to be replaced
- Differentiation between online/offline dictionary,
- existence of current XML description
- use “CoE reload” for resetting changes

Introduction

The CoE overview contains objects for different intended applications:

- Objects required for parameterization during commissioning:
 - Restore object [► 149], index 0x1011
 - Configuration data [► 150], index 0x80n0
 - Command object [► 152], index 0xFB00
- Objects intended for regular operation, e.g. through ADS access.
- Profile-specific objects:
 - Input data [► 152], index 0x60n0
 - Output data [► 155], index 0x70n0
 - Information and diagnostic data [► 156], index 0xA0n0, 0x10F08, 0xF915
- Standard objects [► 157]

The following section first describes the objects required for normal operation, followed by the remaining objects needed for a complete overview.

4.4.1 Restore object

Index 1011 Restore default parameters

Index (hex)	Name	Meaning	Data type	Flags	Default
1011:0	<u>Restore default parameters</u>	Restore default parameters	UINT8	RO	0x01 (1 _{dec})
1011:01	SubIndex 001	If this object is set to “ 0x64616F6C ” in the set value dialog, all backup objects are reset to their delivery state.	UINT32	RW	0x00000000 (0 _{dec})

4.4.2 0x80n0 | Configuration data

Index 80n0 ENC Settings 0 Ch.n (for n = 0 [channel 1], n = 1 [channel 2])

Index (hex)	Name	Meaning	Data type	Flags	Default
80n0:0	ENC Settings 0 Ch.n	Maximum subindex	UINT8	RO	0x23 (35 _{dec})
80n0:01	Enable C reset [► 67]	The counter is reset via the C input.	BOOLEAN	RW	0x00 (0 _{dec})
80n0:02	Enable extern reset	A counter reset is triggered via the external latch input (24 V)	BOOLEAN	RW	0x00 (0 _{dec})
80n0:04	Gate polarity [► 76]	0: "Disable gate" 1: "Enable pos. gate" (gate locks with HIGH signal level) 2: "Enable neg. gate" (gate locks with LOW signal level)	BIT2	RW	0x01 (1 _{dec})
80n0:06	Evaluation mode [► 110]	0: "4-fold" (four-fold evaluation) 1: "1-fold" (single evaluation) 2: "2-fold" (two-fold evaluation)	BIT2	RW	0x00 (0 _{dec})
80n0:08	Disable filter [► 126]	0: Activates the input filter (inputs A, /A, B, /B, C, /C only) 1: Deactivates the input filter If a filter is activated a signal edge must be present for at least 2.4 µs in order to be counted as an increment.	BOOLEAN	RW	0x01 (1 _{dec})
80n0:0A	Enable micro increments [► 83]	If activated, the terminal interpolates micro-increments between the integral encoder increments in DC mode. The lower 8 bits of the counter value are used in each case for the display. A 32-bit counter thus becomes a 24+8-bit counter, a 16-bit counter becomes an 8+8-bit counter.	BOOLEAN	RW	0x00 (0 _{dec})
80n0:0B	Error detection A	A broken wire or short circuit on track A is indicated in index 0x60n0:07 [► 153] and as process data. Diagnostics is only possible, if the associated input is wired differentially.	BOOLEAN	RW	0x01 (1 _{dec})
80n0:0C	Error detection B	A broken wire or short circuit on track B is indicated in index 0x60n0:07 [► 153] and as process data. Diagnostics is only possible, if the associated input is wired differentially.	BOOLEAN	RW	0x01 (1 _{dec})
80n0:0D	Error detection C	A broken wire or short circuit on track C is indicated in index 0x60n0:07 [► 153] and as process data. Diagnostics is only possible, if the associated input is wired differentially.	BOOLEAN	RW	0x00 (0 _{dec})
80n0:0E	Reversion of rotation [► 113]	Activates reversion of rotation	BOOLEAN	RW	0x00 (0 _{dec})
80n0:10	Extern reset polarity	0: "Fall" (the counter is set to zero with a falling edge) 1: "Rise" (the counter is set to zero with a rising edge)	BIT1	RW	0x01 (1 _{dec})
80n0:11	Frequency window [► 121]	Minimum time over which the frequency is determined; default value: 10 ms [resolution: 1 µs]. The frequency is calculated from the number of increments (changes of position value) in the "Frequency window" time interval. The determined frequency is output via the process data in index 0x60n0:13 [► 153] "Frequency value". The frequency calculation is carried out locally without distributed clocks function.	UINT16	RW	0x2710 (10000 _{dec})
80n0:13	Frequency scaling [► 121]	Scaling of the frequency measurement (must be divided by this value to obtain the unit in Hz): 100: "0.01 Hz" (default) 1: "1 Hz"	UINT32	RW	0x00000064 (100 _{dec})
80n0:14	Period scaling	Resolution of the period value in the process data: 10: "10 ns" Period value is a multiple of 10 ns 100: "100 ns" Period value is a multiple of 100 ns 500: "500 ns" Period value is a multiple of 500 ns	UINT32	RW	0x0000000A (10 _{dec})

Index (hex)	Name	Meaning	Data type	Flags	Default
80n0:17	Frequency Wait Time [► 121]	Waiting time [ms] for frequency measurement If no full period is detected within the “ Frequency window [► 122] ”, another frequency window is started to record a full period. This happens until the maximum frequency wait time has elapsed. At least double the period value of the minimum frequency to be measured should be entered here. $t \geq 2 * (1 / f_{min})$	UINT16	RW	0x53E2 (21474 _{dec})
80n0:1D	Frequency numerator [► 124]	Frequency counter value, frequency scaling	UINT32	RW	0x00000001 (1 _{dec})
80n0:1E	Frequency denominator [► 124]	frequency counter value, used for scaling the frequency and the velocity calculation (increments / unit).	UINT32	RW	0x00000001 (1 _{dec})
80n0:21	Enable encoder plausibility check [► 145]	Activation of plausibility check	BOOLEAN	RW	0x00 (0 _{dec})
80n0:22	Enable continuous latch extern [► 118]	FALSE: The following pulses at the Latch input have no influence on the latch value in index 0x60n0:12 “Latch value” when the bit in index 0x70n0:02 or 0x70n0:04 is set. TRUE: The counter value is written to index 0x60n0:12 “Latch value” at every parameterized edge at the Latch input. There is no need to reactivate index 0x70n0:02 or 0x70n0:04.	BOOLEAN	RW	0x00 (0 _{dec})
80n0:23	Enable continuous latch extern 2 [► 74]	FALSE: The following pulses at the “Latch extern 2” input have no influence on the latch value in index 0x60n0:22 “Latch value 2” when the bit in index 0x70n0:0C or 0x70n0:0D is set. TRUE: The counter value is written to index 0x60n0:22 “Latch value 2” at every parameterized edge at the “Latch extern 2” input. There is no need to reactivate index 0x70n0:02 or 0x70n0:04.	BOOLEAN	RW	0x00 (0 _{dec})

Index 80n1 ENC Settings 1 Ch.n (for n = 0 [channel 1], n = 1 [channel 2])

Index (hex)	Name	Meaning	Data type	Flags	Default
80n1:0	ENC Settings 1 Ch.n	Maximum subindex	UINT8	RO	0x1D (29 _{dec})
80n1:17	Supply voltage [► 110]	Setting the sensor supply 50 _{dec} : 5.0 V (default) 120 _{dec} : 12.0 V 240 _{dec} : 24.0 V Refer to the Note on setting the encoder supply [► 110]	UINT32	RW	0x00000032 (50 _{dec})
80n1:19	Filter settings [► 87]	Filter settings: 10 _{dec} : 10 kHz 25 _{dec} : 25 kHz 50 _{dec} : 50 kHz 100 _{dec} : 100 kHz 250 _{dec} : 250 kHz 500 _{dec} : 500 kHz 1000 _{dec} : 1 MHz 2500 _{dec} : 2.5 MHz 5000 _{dec} : 5 MHz (default)	UINT32	RW	0x00001388 (5000 _{dec})
80n1:1A	Limit counter value [► 111]	Specifies the value for the upper counter limit.	UINT32	RW	0xFFFFFFFF (-1 _{dez})
80n1:1B	Reset counter value [► 111]	Specifies the value for the lower counter limit.	UINT32	RW	0x00000000 (0 _{dec})
80n1:1C	Direction inversion hysteresis [► 70]	Enter the hysteresis in number of increments. A value greater than 0 must be selected. If the counter value exceeds the value, the bit in index 0x60n2:13 “Direction inversion detected” is set in the next PLC cycle.	UINT8	RW	0x0A (10 _{dec})
80n1:1D	Counter mode [► 109]	0: Encoder RS422 (diff. input) 1: Counter RS422 (diff. input) 2: Encoder TTL (single ended) 3: Counter TTL (single ended) 4: Encoder open collector 5: Counter open collector	UINT32	RW	0x00000000 (0 _{dec})

4.4.3 0xFB00 | Command object

Index FB00 Command

Index (hex)	Name	Meaning	Data type	Flags	Default	
FB00:0	Command	Max. subindex	UINT8	RO	0x03 (3 _{dec})	
FB00:01	Request	Commands can be sent to the terminal via the request object. Command:	OCTET-STRING[2]	RW	{0}	
		Reset Duty cycle min./max. value [► 82]:				
		0x9130				Index 0x6000:24 “Duty cycle min” for channel 1 is set to zero
		0x9131				Index 0x6010:24 “Duty cycle min” for channel 2 is set to zero
		0x9140				Index 0x6000:25 “Duty cycle max” for channel 1 is set to zero
		0x9141				Index 0x6010:25 “Duty cycle max” for channel 2 is set to zero
		Reset plausibility error counter [► 145]:				
		0x9151				Index 0xA000:13 “Encoder plausibility error counter” for channel 1 is set to zero
		0x9161				Index 0xA010:13 “Encoder plausibility error counter” for channel 2 is set to zero
		Reset of internal error counters [► 87]:				
		0x9152				Index 0xA000:14 “Filter violation counter extern latch” for channel 1 is set to zero
		0x9153				Index 0xA000:15 “Filter violation counter input gate” for channel 1 is set to zero
		0x9154				Index 0xA000:16 “Filter violation counter” for channel 1 is set to zero
		0x9162				Index 0xA010:14 “Filter violation counter extern latch” for channel 2 is set to zero
		0x9163				Index 0xA010:15 “Filter violation counter input gate” for channel 2 is set to zero
		0x9164				Index 0xA010:16 “Filter violation counter” for channel 2 is set to zero
FB00:02	Status	Status of the command currently being executed 0: Command executed without error. 255: Command is being executed	UINT8	RO	0x00 (0 _{dec})	
FB00:03	Response	Optional response value of the command	OCTET-STRING[4]	RO	{0}	

4.4.4 0x60n0 | Input data



Process data can be read via CoE but cannot be set.

In the following descriptions, the corresponding CoE index is always included as a reference in addition to the name of the process data.

- Please note that while the input and output process data (0x6xxx/0x7xxx) can be read via the CoE directory, they cannot be set via the CoE directory!

Index 60n0 ENC Inputs Ch.n (for n = 0 [channel 1], n = 1 [channel 2])

Index (hex)	Name	Meaning	Data type	Flags	Default
60n0:0	ENC Inputs Ch.n	Maximum subindex	UINT8	RO	0x25 (37 _{dec})
60n0:01	Latch C valid [► 75]	The counter value was stored with the zero pulse C input.	BOOLEAN	RO	0x00 (0 _{dec})
60n0:02	Latch extern valid [► 118]	The counter value was stored via the Latch extern input.	BOOLEAN	RO	0x00 (0 _{dec})
60n0:03	Set counter done [► 68]	The counter was set.	BOOLEAN	RO	0x00 (0 _{dec})
60n0:04	Counter underflow [► 142]	The value has fallen below the lower counter limit. The bit is reset when the counter value has fallen below 2/3 of the counting range.	BOOLEAN	RO	0x00 (0 _{dec})
60n0:05	Counter overflow [► 142]	The upper counter limit was exceeded. The bit is reset when the counter value has fallen below 1/3 of the counting range.	BOOLEAN	RO	0x00 (0 _{dec})
60n0:06	Status of input status [► 96]	State of the status input (alarm "Input 1")	BOOLEAN	RO	0x00 (0 _{dec})
60n0:07	Open circuit	Indicates an open circuit. Configuration via index 0x80n0:0A , 0x80n0:0B , 0x80n0:0C [► 150]	BOOLEAN	RO	0x00 (0 _{dec})
60n0:08	Extrapolation stall	The extrapolated part of the counter is invalid. The speed has fallen below the minimum speed required to use the micro-increments [► 83].	BOOLEAN	RO	0x00 (0 _{dec})
60n0:09	Status of input A	Status of input A	BOOLEAN	RO	0x00 (0 _{dec})
60n0:0A	Status of input B	Status of input B	BOOLEAN	RO	0x00 (0 _{dec})
60n0:0B	Status of input C	Status of input C	BOOLEAN	RO	0x00 (0 _{dec})
60n0:0C	Status of input gate [► 76]	The state of the gate input	BOOLEAN	RO	0x00 (0 _{dec})
60n0:0D	Status of extern latch [► 118]	Only in "Legacy" mode: Status of the "Latch extern" input	BOOLEAN	RO	0x00 (0 _{dec})
60n0:0E	Sync Error	Only in "Legacy" mode: The Sync error bit is only required for DC mode. It indicates whether a synchronization error has occurred during the previous cycle. This means a SYNC signal was triggered in the terminal, although no new process data were available (0 = OK, 1 = NOK).	BOOLEAN	RO	0x00 (0 _{dec})
60n0:0F	TxPDO State	Only in "Legacy" mode: Validity of the data of the associated TxPDO (0 = valid, 1 = invalid).	BOOLEAN	RO	0x00 (0 _{dec})
60n0:10	TxPDO Toggle	Only in "Legacy" mode: The TxPDO toggle is toggled by the slave when the data of the associated TxPDO is updated.	BOOLEAN	RO	0x00 (0 _{dec})
60n0:11	Counter value [► 109]	Counter value	UINT32	RO	0x00000000 (0 _{dec})
60n0:12	Latch value [► 118]	Latch value	UINT32	RO	0x00000000 (0 _{dec})
60n0:13	Frequency value [► 121]	Frequency (the scaling is set in index 0x80n0:13 [► 150])	UINT32	RO	0x00000000 (0 _{dec})
60n0:14	Period value [► 123]	Period value (the scaling is set in index 0x80n0:14 [► 150])	UINT32	RO	0x00000000 (0 _{dec})
60n0:16	Timestamp [► 85]	Timestamp of the last counter change	UINT64	RO	
60n0:1F	Timestamp C [► 85]	Timestamp of the last registered positive edge of zero pulse C	UINT64	RO	
60n0:20	Timestamp latch [► 86]	Timestamp of the last edge (depending on the parameterization of the Latch input) at Latch extern.	UINT64	RO	
60n0:21	Timestamp latch 2 [► 86]	When the Gate/Latch input is used as "Latch extern 2" input: Timestamp of the last edge (depending on the parameterization of the Gate/Latch input) at the "Latch extern 2" input.	UINT64	RO	
60n0:22	Latch value 2 [► 86]	Latch value of the "Latch extern 2" input (Gate input is used as second Latch input)	UINT32	RO	0x00000000 (0 _{dec})
60n0:23	Duty cycle [► 82]	Indicates the ratio of pulse duration/period value.	UINT16	RO	0x0000 (0 _{dec})
60n0:24	Duty cycle min	Returns the smallest measured duty cycle value	UINT16	RO	0x0000 (0 _{dec})
60n0:25	Duty cycle max	Returns the largest measured duty cycle value	UINT16	RO	0x0000 (0 _{dec})

Index 60n2 ENC Input status Ch. n (for n = 0 [channel 1], n = 1 [channel 2])

Index (hex)	Name	Meaning	Data type	Flags	Default
60n2:0	ENC Inputs status Ch. n	Maximum subindex	UINT8	RO	0x15 (21 _{dec})
60n2:0D	Diag	Indicates that a new message is available in the "Diag History"	BOOLEAN	RO	0x00 (0 _{dec})
60n2:0E	TxPDO State	Validity of the data of the associated TxPDO (0 = valid, 1 = invalid)	BOOLEAN	RO	0x00 (0 _{dec})
60n2:0F	Input cycle counter	2-bit counter for synchronization (incremented only if a new value is present)	BIT2	RO	0x00 (0 _{dec})
60n2:11	Software gate valid	0: Counter unlocked (index 0x70n0:09 ▶ 155] "Set software gate" = FALSE) 1: Counter locked (index 0x70n0:09 "Set software gate" = TRUE)	BOOLEAN	RO	0x00 (0 _{dec})
60n2:12	Latch extern 2 valid ▶ 74	0: a new counter value can be stored in index 0x60n0:22 ▶ 153] "Latch value 2" 1: no further counter values are stored in 0x60n0:22 "Latch value 2".	BOOLEAN	RO	0x00 (0 _{dec})
60n2:13	Direction inversion detected ▶ 70	Indicates reversal of the counting direction	BOOLEAN	RO	0x00 (0 _{dec})
60n2:14	Status of extern latch ▶ 118	Status of the ext. "Latch extern" input	BOOLEAN	RO	0x00 (0 _{dec})
60n2:15	Counter value out of range ▶ 111	Indicates that counter value is outside the parameterized counter limits	BOOLEAN	RO	0x00 (0 _{dec})

4.4.5 0x70n0 | Output data

● Process data can be read via CoE but cannot be set.

i In the following descriptions, the corresponding CoE index is always included as a reference in addition to the name of the process data.

- Please note that while the input and output process data (0x6xxx/0x7xxx) can be read via the CoE directory, they cannot be set via the CoE directory!

Index 70n0 ENC Outputs Ch.n (for n = 0 [channel 1], n = 1 [channel 2])

Index (hex)	Name	Meaning	Data type	Flags	Default
70n0:0	ENC Outputs Ch.n	Maximum subindex	UINT8	RO	0x11 (17 _{dec})
70n0:01	Enable latch C [► 75]	Enable saving via the zero pulse C input.	BOOLEAN	RO	0x00 (0 _{dec})
70n0:02	Enable latch extern on positive edge [► 118]	Enable saving via the "Latch extern" input with positive edge.	BOOLEAN	RO	0x00 (0 _{dec})
70n0:03	Set counter [► 116]	Set counter value	BOOLEAN	RO	0x00 (0 _{dec})
70n0:04	Enable latch extern on negative edge [► 118]	Enable saving via the "Latch extern" input with negative edge.	BOOLEAN	RO	0x00 (0 _{dec})
70n0:08	Set counter on latch C [► 68]	Enable counter value specification via the zero pulse C input	BOOLEAN	RO	0x00 (0 _{dec})
70n0:09	Set software gate [► 120]	Locks the counter via a PLC variable 0: Counter is unlocked 1: Counter is locked	BOOLEAN	RO	0x00 (0 _{dec})
70n0:0A	Set counter on latch extern on positive edge [► 69]	Enables counter value specification via a positive edge at the "Latch extern" input. The counter value is specified in index 0x70n0:11 "Set counter value".	BOOLEAN	RO	0x00 (0 _{dec})
70n0:0B	Set counter on latch extern on negative edge [► 69]	Enables counter value specification via a negative edge at the "Latch extern" input. The counter value is specified in index 0x70n0:11 "Set counter value".	BOOLEAN	RO	0x00 (0 _{dec})
70n0:0C	Enable latch extern 2 on positive edge [► 74]	Enable saving via the Gate/Latch input with positive edge.	BOOLEAN	RO	0x00 (0 _{dec})
70n0:0D	Enable latch extern 2 on negative edge [► 74]	Enable saving via the Gate/Latch input with negative edge.	BOOLEAN	RO	0x00 (0 _{dec})
70n0:11	Set counter value [► 69]	The counter value to be set via "Set counter" (index 0x70n0:03).	UINT32	RO	0x00000000 (0 _{dec})

4.4.6 0xA0n0 | Information and diagnostic data (channel specific)

Index A0n0 ENC Diag data Ch. n (for n = 0 [channel 1], n = 1 [channel 2])

Index (hex)	Name	Meaning	Data type	Flags	Default
A0n0:0	ENC Diag data Ch.n	Maximum subindex	UINT8	RO	0x16 (22 _{dec})
A0n0:01	Error A	An "open circuit" error is present at input A	BOOLEAN	RO	0x00 (0 _{dec})
A0n0:02	Error B	An "open circuit" error is present at input B	BOOLEAN	RO	0x00 (0 _{dec})
A0n0:03	Error C	An "open circuit" error is present at input zero pulse C	BOOLEAN	RO	0x00 (0 _{dec})
A0n0:04	Field power failure	Encoder supply voltage is not present	BOOLEAN	RO	0x00 (0 _{dec})
A0n0:05	Error Input status	Over/undervoltage at the "Status input" input (alarm input)	BOOLEAN	RO	0x00 (0 _{dec})
A0n0:13	Encoder plausibility error counter	Number of detected plausibility errors	UINT16	RO	0x0000 (0 _{dec})
A0n0:14	Filter violation counter extern latch	Number of filter overruns detected at the Latch input	UINT16	RO	0x0000 (0 _{dec})
A0n0:15	Filter violation counter input gate	Number of filter overruns detected at the Gate/Latch input	UINT16	RO	0x0000 (0 _{dec})
A0n0:16	Filter violation counter	Number of filter overruns detected at the encoder inputs	UINT16	RO	0x0000 (0 _{dec})

4.4.7 0x10F3, 0x10F8, 0xF915 | Information and diagnostic data (device-specific)

Index 10F3 Diagnosis History

Index (hex)	Name	Meaning	Data type	Flags	Default
10F3:0	Diagnosis History	Maximum subindex	UINT8	RO	0x15 (21 _{dec})
10F3:01	Maximum Messages	Maximum number of stored messages A maximum of 16 messages can be stored.	UINT8	RO	0x00 (0 _{dec})
10F3:02	Newest Messages	Subindex of the latest message	UINT8	RO	0x00 (0 _{dec})
10F3:03	Newest Acknowledged Messages	Subindex of the last confirmed message	UINT8	RW	0x00 (0 _{dec})
10F3:04	New Messages Available	Indicates that a new message is available	BOOLEAN	RO	0x00 (0 _{dec})
10F3:05	Flags	not used	UINT16	RW	0x0000 (0 _{dec})
10F3:06	Diagnosis Message 001	Message 1	OCTET-STRING[20]	RO	{0}
...	...	...	...	...	...
10F3:15	Diagnosis Message 016	Message 16	OCTET-STRING[20]	RO	{0}

Index 10F8 Timestamp Object

Index (hex)	Name	Meaning	Data type	Flags	Default
10F8:0	Timestamp Object	Timestamp	UINT64	RO	

Index F915 LED Status

Index (hex)	Name	Meaning	Data type	Flags	Default
F915:0	LED Status	Largest subindex of this object	UINT8	RO	0x10 (16 _{dec})
F915:01	Run	See the LED description [► 34] and the chapter “ LED status via CoE 0xF915 [► 147] ”	UINT32	RO	0x00000000 (0 _{dec})
F915:02	Ch1 A		UINT32	RO	0x00000000 (0 _{dec})
F915:03	Ch1 B		UINT32	RO	0x00000000 (0 _{dec})
F915:04	Ch1 C / Ch2 A		UINT32	RO	0x00000000 (0 _{dec})
F915:05	Ch1 DI / Ch2 B		UINT32	RO	0x00000000 (0 _{dec})
F915:07	Latch		UINT32	RO	0x00000000 (0 _{dec})
F915:09	Enc supply		UINT32	RO	0x00000000 (0 _{dec})
F915:0A	Diag		UINT32	RO	0x00000000 (0 _{dec})
F915:0F	Gate		UINT32	RO	0x00000000 (0 _{dec})

4.4.8 0x1000 - 0xFnnn | Standard objects**Standard objects (0x1000-0x1FFF)**

The standard objects have the same meaning for all EtherCAT slaves.

4.4.8.1 1000...10F0 | Device**Index 1000 Device type**

Index (hex)	Name	Meaning	Data type	Flags	Default
1000:0	Device type	Device type of the EtherCAT slave: - The Low-Word contains the CoE profile used (5001). - The High-Word contains the module profile according to the modular device profile.	UINT32	RO	0x01FF1389 (33493897 _{dec})

Index 1008 Device name

Index (hex)	Name	Meaning	Data type	Flags	Default
1008:0	Device name	Device name of the EtherCAT slave	STRING	RO	ED5112

Index 1009 Hardware version

Index (hex)	Name	Meaning	Data type	Flags	Default
1009:0	Hardware version	Hardware version of the EtherCAT slave	STRING	RO	09

Index 100A Software version

Index (hex)	Name	Meaning	Data type	Flags	Default
100A:0	Software version	Firmware version of the EtherCAT slave	STRING	RO	10

Index 100B Bootloader version

Index (hex)	Name	Meaning	Data type	Flags	Default
100B:0	Bootloader version	Bootloader version	STRING	RO	

Index 1018 Identity

Index (hex)	Name	Meaning	Data type	Flags	Default
1018:0	Identity	Information for identifying the slave	UINT8	RO	0x04 (4 _{dec})
1018:01	Vendor ID	Vendor ID of the EtherCAT slave	UINT32	RO	0x00000002 (2 _{dec})
1018:02	Product code	Product code of the EtherCAT slave	UINT32	RO	0x13F83052 (335032402 _{dec})
1018:03	Revision	Revision number of the EtherCAT slave: - The Low Word (bit 0-15) indicates the special terminal number. - The High Word (bit 16-31) refers to the device description.	UINT32	RO	0x00000000 (0 _{dec})
1018:04	Serial number	Serial number of the EtherCAT slave: - Low-Word - The Low Byte (bit 0-7) of the Low Word contains the year of production, - The High Byte (bit 8-15) of the Low Word contains the week of production. - The High Word (bit 16-31) is 0.	UINT32	RO	0x00000000 (0 _{dec})

Index 10E2 Manufacturer-specific Identification Code¹⁾

Index (hex)	Name	Meaning	Data type	Flags	Default
10E2:0	Manufacturer-specific Identification Code	Manufacturer-specific Identification Code	UINT8	RO	0x01 (1 _{dec})
10E2:01	SubIndex 001	reserved	STRING	RO	

Index 10F0 Backup parameter handling

Index (hex)	Name	Meaning	Data type	Flags	Default
10F0:0	Backup parameter handling	Information for standardized loading and saving of backup entries	UINT8	RO	0x01 (1 _{dec})
10F0:01	Checksum	Checksum across all backup entries of the EtherCAT slave	UINT32	RO	0x00000000 (0 _{dec})

4.4.8.2 14nn | Exclude RxPDO**Index ENC 1400 RxPDO-Par Control Ch.1**

Index (hex)	Name	Meaning	Data type	Flags	Default
1400:0	ENC RxPDO-Par Control Ch.1	PDO Parameter RxPDO 1	UINT8	RO	0x06 (6 _{dec})
1400:06	Exclude RxPDOs	Specifies the RxPDOs (index of RxPDO mapping objects) that must not be transferred together with RxPDO 1.	OCTET-STRING[22]	RO	01 16 02 16 03 16 04 16 05 16 06 16 07 16 0A 16 0B 16 0C 16 0D 16

Index 1401 ENC RxPDO-Par Control Compact Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1401:0	ENC RxPDO-Par Control Compact Ch.1	PDO Parameter RxPDO 2	UINT8	RO	0x06 (6 _{dec})
1401:06	Exclude RxPDOs	Specifies the RxPDOs (index of RxPDO mapping objects) that must not be transferred together with RxPDO 2.	OCTET-STRING[22]	RO	00 16 02 16 03 16 04 16 05 16 06 16 07 16 00 00 00 00 00 00 00 00

Index 1402 ENC RxPDO-Par Control Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1402:0	ENC RxPDO-Par Control Ch.1	PDO Parameter RxPDO 3	UINT8	RO	0x06 (6 _{dec})
1402:06	Exclude RxPDOs	Specifies the RxPDOs (index of RxPDO mapping objects) that must not be transferred together with RxPDO 3.	OCTET-STRING[22]	RO	00 16 01 16 03 16 04 16 05 16 06 16 07 16 00 00 00 00 00 00 00 00

Index 1403 ENC RxPDO-Par Control Compact Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1403:0	ENC RxPDO-Par Control Compact Ch.1	PDO Parameter RxPDO 4	UINT8	RO	0x06 (6 _{dec})
1403:06	Exclude RxPDOs	Specifies the RxPDOs (index of RxPDO mapping objects) that must not be transferred together with RxPDO 4.	OCTET-STRING[22]	RO	00 16 01 16 02 16 04 16 05 16 06 16 07 16 00 00 00 00 00 00 00 00

Index 1404 ENC RxPDO-Par Control Counter Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1404:0	ENC RxPDO-Par Control Counter Ch.1	PDO Parameter RxPDO 5	UINT8	RO	0x06 (6 _{dec})
1404:06	Exclude RxPDOs	Specifies the RxPDOs (index of RxPDO mapping objects) that must not be transferred together with RxPDO 5.	OCTET-STRING[22]	RO	00 16 01 16 02 16 03 16 05 16 06 16 07 16 00 00 00 00 00 00 00 00

Index 1405 ENC RxPDO-Par Control Compact Counter Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1405:0	ENC RxPDO-Par Control Compact Counter Ch.1	PDO Parameter RxPDO 6	UINT8	RO	0x06 (6 _{dec})
1405:06	Exclude RxPDOs	Specifies the RxPDOs (index of RxPDO mapping objects) that must not be transferred together with RxPDO 6.	OCTET-STRING[22]	RO	00 16 01 16 02 16 03 16 04 16 06 16 07 16 00 00 00 00 00 00 00 00

Index 1406 ENC RxPDO-Par Control Legacy Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1406:0	ENC RxPDO-Par Control Legacy Ch.1	PDO Parameter RxPDO 7	UINT8	RO	0x06 (6 _{dec})
1406:06	Exclude RxPDOs	Specifies the RxPDOs (index of RxPDO mapping objects) that must not be transferred together with RxPDO 7.	OCTET-STRING[22]	RO	00 16 01 16 02 16 03 16 04 16 05 16 07 16 00 00 00 00 00 00 00 00

Index 1407 ENC RxPDO-Par Control Compact Legacy Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1407:0	ENC RxPDO-Par Control Compact Legacy Ch.1	PDO Parameter RxPDO 8	UINT8	RO	0x06 (6 _{dec})
1407:06	Exclude RxPDOs	Specifies the RxPDOs (index of RxPDO mapping objects) that must not be transferred together with RxPDO 8.	OCTET-STRING[22]	RO	00 16 01 16 02 16 03 16 04 16 05 16 06 16 00 00 00 00 00 00 00 00

Index 140A ENC RxPDO-Par Control Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
140A:0	ENC RxPDO-Par Control Ch.2	PDO Parameter RxPDO 9	UINT8	RO	0x06 (6 _{dec})
140A:06	Exclude RxPDOs	Specifies the RxPDOs (index of RxPDO mapping objects) that must not be transferred together with RxPDO 9.	OCTET-STRING[22]	RO	00 16 01 16 06 16 07 16 0B 16 0C 16 00 00 00 00 00 00 00 00

Index 140B ENC RxPDO-Par Control Compact Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
140B:0	ENC RxPDO-Par Control Compact Ch.2	PDO Parameter RxPDO 10	UINT8	RO	0x06 (6 _{dec})
140B:06	Exclude RxPDOs	Specifies the RxPDOs (index of RxPDO mapping objects) that must not be transferred together with RxPDO 10.	OCTET-STRING[22]	RO	00 16 01 16 06 16 07 16 0A 16 0C 16 0D 16 00 00 00 00 00 00 00 00

Index 140C ENC RxPDO-Par Control Counter Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
140C:0	ENC RxPDO-Par Control Counter Ch.2	PDO Parameter RxPDO 11	UINT8	RO	0x06 (6 _{dec})
140C:06	Exclude RxPDOs	Specifies the RxPDOs (index of RxPDO mapping objects) that must not be transferred together with RxPDO 11.	OCTET-STRING[22]	RO	00 16 01 16 06 16 07 16 0A 16 0B 16 0D 16 00 00 00 00 00 00 00 00

Index 140D ENC RxPDO-Par Control Compact Counter Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
140D:0	ENC RxPDO-Par Control Compact Counter Ch.2	PDO Parameter RxPDO 12	UINT8	RO	0x06 (6 _{dec})
140D:06	Exclude RxPDOs	Specifies the RxPDOs (index of RxPDO mapping objects) that must not be transferred together with RxPDO 12.	OCTET-STRING[22]	RO	00 16 01 16 06 16 07 16 0A 16 0B 16 0C 16 00 00 00 00 00 00 00 00

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Index 1600 ENC RxPDO-Map Control Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1600:0	ENC RxPDO-Map Control Ch.1	PDO Mapping RxPDO 1	UINT8	RO	0x0D (13 _{dec})
1600:01	SubIndex 001	1. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x01 (Ctrl))	UINT32	RO	0x7000:01, 1
1600:02	SubIndex 002	2. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x02 (Enable latch extern on positive edge))	UINT32	RO	0x7000:02, 1
1600:03	SubIndex 003	3. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x03 (Set counter))	UINT32	RO	0x7000:03, 1
1600:04	SubIndex 004	4. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x04 (Enable latch extern on negative edge))	UINT32	RO	0x7000:04, 1
1600:05	SubIndex 005	5. PDO Mapping entry (3 bits align)	UINT32	RO	0x0000:00, 3
1600:06	SubIndex 006	6. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x08 (Set counter on latch C))	UINT32	RO	0x7000:08, 1
1600:07	SubIndex 007	7. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x09 (Set software gate))	UINT32	RO	0x7000:09, 1
1600:08	SubIndex 008	8. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x0A (Set counter on latch extern on positive edge))	UINT32	RO	0x7000:0A, 1
1600:09	SubIndex 009	9. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x0B (Set counter on latch extern on negative edge))	UINT32	RO	0x7000:0B, 1
1600:0A	SubIndex 010	10. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x0C (Enable latch extern 2 on positive edge))	UINT32	RO	0x7000:0C, 1
1600:0B	SubIndex 011	11. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x0D (Enable latch extern 2 on negative edge))	UINT32	RO	0x7000:0D, 1
1600:0C	SubIndex 012	12. PDO Mapping entry (3 bits align)	UINT32	RO	0x0000:00, 3
1600:0D	SubIndex 013	13. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x11 (Set counter value))	UINT32	RO	0x7000:11, 32

Index 1601 ENC RxPDO-Map Control Compact Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1601:0	ENC RxPDO-Map Control Compact Ch.1	PDO Mapping RxPDO 2	UINT8	RO	0x0D (13 _{dec})
1601:01	SubIndex 001	1. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x01 (Ctrl))	UINT32	RO	0x7000:01, 1
1601:02	SubIndex 002	2. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x02 (Enable latch extern on positive edge))	UINT32	RO	0x7000:02, 1
1601:03	SubIndex 003	3. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x03 (Set counter))	UINT32	RO	0x7000:03, 1
1601:04	SubIndex 004	4. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x04 (Enable latch extern on negative edge))	UINT32	RO	0x7000:04, 1
1601:05	SubIndex 005	5. PDO Mapping entry (3 bits align)	UINT32	RO	0x0000:00, 3
1601:06	SubIndex 006	6. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x08 (Set counter on latch C))	UINT32	RO	0x7000:08, 1
1601:07	SubIndex 007	7. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x09 (Set software gate))	UINT32	RO	0x7000:09, 1
1601:08	SubIndex 008	8. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x0A (Set counter on latch extern on positive edge))	UINT32	RO	0x7000:0A, 1
1601:09	SubIndex 009	9. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x0B (Set counter on latch extern on negative edge))	UINT32	RO	0x7000:0B, 1
1601:0A	SubIndex 010	10. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x0C (Enable latch extern 2 on positive edge))	UINT32	RO	0x7000:0C, 1
1601:0B	SubIndex 011	11. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x0D (Enable latch extern 2 on negative edge))	UINT32	RO	0x7000:0D, 1
1601:0C	SubIndex 012	12. PDO Mapping entry (3 bits align)	UINT32	RO	0x0000:00, 3
1601:0D	SubIndex 013	13. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x11 (Set counter value))	UINT32	RO	0x7000:11, 16

Index 1602 ENC RxPDO-Map Control Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1602:0	ENC RxPDO-Map Control Ch.1	PDO Mapping RxPDO 3	UINT8	RO	0x0A (10 _{dec})
1602:01	SubIndex 001	1. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1602:02	SubIndex 002	2. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x02 (Enable latch extern on positive edge))	UINT32	RO	0x7000:02, 1
1602:03	SubIndex 003	3. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x03 (Set counter))	UINT32	RO	0x7000:03, 1
1602:04	SubIndex 004	4. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x04 (Enable latch extern on negative edge))	UINT32	RO	0x7000:04, 1
1602:05	SubIndex 005	5. PDO Mapping entry (4 bits align)	UINT32	RO	0x0000:00, 4
1602:06	SubIndex 006	6. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x09 (Set software gate))	UINT32	RO	0x7000:09, 1
1602:07	SubIndex 007	7. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x0A (Set counter on latch extern on positive edge))	UINT32	RO	0x7000:0A, 1
1602:08	SubIndex 008	8. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x0B (Set counter on latch extern on negative edge))	UINT32	RO	0x7000:0B, 1
1602:09	SubIndex 009	9. PDO Mapping entry (5 bits align)	UINT32	RO	0x0000:00, 5
1602:0A	SubIndex 010	10. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x11 (Set counter value))	UINT32	RO	0x7000:11, 32

Index 1603 ENC RxPDO-Map Control Compact Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1603:0	ENC RxPDO-Map Control Compact Ch.1	PDO Mapping RxPDO 4	UINT8	RO	0x0A (10 _{dec})
1603:01	SubIndex 001	1. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1603:02	SubIndex 002	2. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x02 (Enable latch extern on positive edge))	UINT32	RO	0x7000:02, 1
1603:03	SubIndex 003	3. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x03 (Set counter))	UINT32	RO	0x7000:03, 1
1603:04	SubIndex 004	4. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x04 (Enable latch extern on negative edge))	UINT32	RO	0x7000:04, 1
1603:05	SubIndex 005	5. PDO Mapping entry (4 bits align)	UINT32	RO	0x0000:00, 4
1603:06	SubIndex 006	6. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x09 (Set software gate))	UINT32	RO	0x7000:09, 1
1603:07	SubIndex 007	7. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x0A (Set counter on latch extern on positive edge))	UINT32	RO	0x7000:0A, 1
1603:08	SubIndex 008	8. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x0B (Set counter on latch extern on negative edge))	UINT32	RO	0x7000:0B, 1
1603:09	SubIndex 009	9. PDO Mapping entry (5 bits align)	UINT32	RO	0x0000:00, 5
1603:0A	SubIndex 010	10. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x11 (Set counter value))	UINT32	RO	0x7000:11, 16

Index 1604 ENC RxPDO-Map Control Counter Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1604:0	ENC RxPDO-Map Control Counter Ch.1	PDO Mapping RxPDO 5	UINT8	RO	0x06 (6 _{dec})
1604:01	SubIndex 001	1. PDO Mapping entry (2 bits align)	UINT32	RO	0x0000:00, 2
1604:02	SubIndex 002	2. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x03 (Set counter))	UINT32	RO	0x7000:03, 1
1604:03	SubIndex 003	3. PDO Mapping entry (5 bits align)	UINT32	RO	0x0000:00, 5
1604:04	SubIndex 004	4. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x09 (Set software gate))	UINT32	RO	0x7000:09, 1
1604:05	SubIndex 005	5. PDO Mapping entry (7 bits align)	UINT32	RO	0x0000:00, 7
1604:06	SubIndex 006	6. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x11 (Set counter value))	UINT32	RO	0x7000:11, 32

Index 1605 ENC RxPDO-Map Control Compact Counter Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1605:0	ENC RxPDO-Map Control Counter Ch.1	PDO Mapping RxPDO 6	UINT8	RO	0x06 (6 _{dec})
1605:01	SubIndex 001	1. PDO Mapping entry (2 bits align)	UINT32	RO	0x0000:00, 2
1605:02	SubIndex 002	2. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x03 (Set counter))	UINT32	RO	0x7000:03, 1
1605:03	SubIndex 003	3. PDO Mapping entry (5 bits align)	UINT32	RO	0x0000:00, 5
1605:04	SubIndex 004	4. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x09 (Set software gate))	UINT32	RO	0x7000:09, 1
1605:05	SubIndex 005	5. PDO Mapping entry (7 bits align)	UINT32	RO	0x0000:00, 7
1605:06	SubIndex 006	6. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x11 (Set counter value))	UINT32	RO	0x7000:11, 16

Index 1606 ENC RxPDO-Map Control Legacy Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1606:0	ENC RxPDO-Map Control Legacy Ch.1	PDO Mapping RxPDO 7	UINT8	RO	0x06 (6 _{dec})
1606:01	SubIndex 001	1. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x01 (Ctrl))	UINT32	RO	0x7000:01, 1
1606:02	SubIndex 002	2. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x02 (Enable latch extern on positive edge))	UINT32	RO	0x7000:02, 1
1606:03	SubIndex 003	3. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x03 (Set counter))	UINT32	RO	0x7000:03, 1
1606:04	SubIndex 004	4. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x04 (Enable latch extern on negative edge))	UINT32	RO	0x7000:04, 1
1606:05	SubIndex 005	5. PDO Mapping entry (12 bits align)	UINT32	RO	0x0000:00, 12
1606:06	SubIndex 006	6. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x11 (Set counter value))	UINT32	RO	0x7000:11, 32

Index 1607 ENC RxPDO-Map Control Compact Legacy Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1607:0	ENC RxPDO-Map Control Compact Legacy Ch.1	PDO Mapping RxPDO 8	UINT8	RO	0x06 (6 _{dec})
1607:01	SubIndex 001	1. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x01 (Ctrl))	UINT32	RO	0x7000:01, 1
1607:02	SubIndex 002	2. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x02 (Enable latch extern on positive edge))	UINT32	RO	0x7000:02, 1
1607:03	SubIndex 003	3. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x03 (Set counter))	UINT32	RO	0x7000:03, 1
1607:04	SubIndex 004	4. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x04 (Enable latch extern on negative edge))	UINT32	RO	0x7000:04, 1
1607:05	SubIndex 005	5. PDO Mapping entry (12 bits align)	UINT32	RO	0x0000:00, 12
1607:06	SubIndex 006	6. PDO Mapping entry (object 0x7000 (ENC Outputs Ch.1), entry 0x11 (Set counter value))	UINT32	RO	0x7000:11, 16

Index 160A ENC RxPDO-Map Control Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
160A:0	ENC RxPDO-Map Control Ch.2	PDO Mapping RxPDO 9	UINT8	RO	0x0A (10 _{dec})
160A:01	SubIndex 001	1. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
160A:02	SubIndex 002	2. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x02 (Enable latch extern on positive edge))	UINT32	RO	0x7010:02, 1
160A:03	SubIndex 003	3. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x03 (Set counter))	UINT32	RO	0x7010:03, 1
160A:04	SubIndex 004	4. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x04 (Enable latch extern on negative edge))	UINT32	RO	0x7010:04, 1
160A:05	SubIndex 005	5. PDO Mapping entry (4 bits align)	UINT32	RO	0x0000:00, 4
160A:06	SubIndex 006	6. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x09 (Set software gate))	UINT32	RO	0x7010:09, 1
160A:07	SubIndex 007	7. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x0A (Set counter on latch extern on positive edge))	UINT32	RO	0x7010:0A, 1
160A:08	SubIndex 008	8. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x0B (Set counter on latch extern on negative edge))	UINT32	RO	0x7010:0B, 1
160A:09	SubIndex 009	9. PDO Mapping entry (5 bits align)	UINT32	RO	0x0000:00, 5
160A:0A	SubIndex 010	10. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x11 (Set counter value))	UINT32	RO	0x7010:11, 32

Index 160B ENC RxPDO-Map Control Compact Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
160B:0	ENC RxPDO-Map Control Compact Ch.2	PDO Mapping RxPDO 10	UINT8	RO	0x0A (10 _{dec})
160B:01	SubIndex 001	1. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
160B:02	SubIndex 002	2. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x02 (Enable latch extern on positive edge))	UINT32	RO	0x7010:02, 1
160B:03	SubIndex 003	3. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x03 (Set counter))	UINT32	RO	0x7010:03, 1
160B:04	SubIndex 004	4. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x04 (Enable latch extern on negative edge))	UINT32	RO	0x7010:04, 1
160B:05	SubIndex 005	5. PDO Mapping entry (4 bits align)	UINT32	RO	0x0000:00, 4
160B:06	SubIndex 006	6. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x09 (Set software gate))	UINT32	RO	0x7010:09, 1
160B:07	SubIndex 007	7. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x0A (Set counter on latch extern on positive edge))	UINT32	RO	0x7010:0A, 1
160B:08	SubIndex 005	8. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x0B (Set counter on latch extern on negative edge))	UINT32	RO	0x7010:0B, 1
160B:09	SubIndex 006	9. PDO Mapping entry (5 bits align)	UINT32	RO	0x0000:00, 5
160B:0A	SubIndex 007	10. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x11 (Set counter value))	UINT32	RO	0x7010:11, 16

Index 160C ENC RxPDO-Map Control Counter Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
160C:0	ENC RxPDO-Map Control Counter Ch.2	PDO Mapping RxPDO 11	UINT8	RO	0x06 (6 _{dec})
160C:01	SubIndex 001	1. PDO Mapping entry (2 bits align)	UINT32	RO	0x0000:00, 2
160C:02	SubIndex 002	2. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x03 (Set counter))	UINT32	RO	0x7010:03, 1
160C:03	SubIndex 003	3. PDO Mapping entry (5 bits align)	UINT32	RO	0x0000:00, 5
160C:04	SubIndex 004	4. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x09 (Set software gate))	UINT32	RO	0x7010:09, 1
160C:05	SubIndex 005	5. PDO Mapping entry (7 bits align)	UINT32	RO	0x0000:00, 7
160C:06	SubIndex 006	6. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x11 (Set counter value))	UINT32	RO	0x7010:11, 32

Index 160D ENC RxPDO-Map Control Compact Counter Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
160D:0	ENC RxPDO-Map Control Compact Counter Ch.2	PDO Mapping RxPDO 12	UINT8	RO	0x06 (6 _{dec})
160D:01	SubIndex 001	1. PDO Mapping entry (2 bits align)	UINT32	RO	0x0000:00, 2
160D:02	SubIndex 002	2. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x03 (Set counter))	UINT32	RO	0x7010:03, 1
160D:03	SubIndex 003	3. PDO Mapping entry (5 bits align)	UINT32	RO	0x0000:00, 5
160D:04	SubIndex 004	4. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x09 (Set software gate))	UINT32	RO	0x7010:09, 1
160D:05	SubIndex 005	5. PDO Mapping entry (7 bits align)	UINT32	RO	0x0000:00, 7
160D:06	SubIndex 006	6. PDO Mapping entry (object 0x7010 (ENC Outputs Ch.2), entry 0x11 (Set counter value))	UINT32	RO	0x7010:11, 16

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Index 1800 ENC TxPDO-Par Status Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1800:0	ENC TxPDO-Par Status Ch.1	PDO Parameter TxPDO 1	UINT8	RO	0x06 (6 _{dec})
1800:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 1.	OCTET-STRING[30]	RO	01 1A 02 1A 03 1A 04 1A 05 1A 06 1A 07 1A 11 1A 12 1A 13 1A 14 1A 17 1A 18 1A 19 1A 1A 1A

Index 1801 ENC TxPDO-Par Status Compact Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1801:0	ENC TxPDO-Par Status Compact Ch.1	PDO Parameter TxPDO 2	UINT8	RO	0x06 (6 _{dec})
1801:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 2.	OCTET-STRING[30]	RO	00 1A 02 1A 03 1A 04 1A 05 1A 06 1A 07 1A

Index 1802 ENC TxPDO-Par Status Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1802:0	ENC TxPDO-Par Status Ch.1	PDO Parameter TxPDO 3	UINT8	RO	0x06 (6 _{dec})
1802:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 3.	OCTET-STRING[30]	RO	00 1A 01 1A 03 1A 04 1A 05 1A 06 1A 07 1A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Index 1803 ENC TxPDO-Par Status Compact Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1803:0	ENC TxPDO-Par Status Compact Ch.1	PDO Parameter TxPDO 4	UINT8	RO	0x06 (6 _{dec})
1803:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 4.	OCTET-STRING[30]	RO	00 1A 01 1A 02 1A 04 1A 05 1A 06 1A 07 1A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Index 1804 ENC TxPDO-Par Status Counter Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1804:0	ENC TxPDO-Par Status Counter Ch.1	PDO Parameter TxPDO 5	UINT8	RO	0x06 (6 _{dec})
1804:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 5.	OCTET-STRING[30]	RO	00 1A 01 1A 02 1A 03 1A 05 1A 06 1A 07 1A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Index 1805 ENC TxPDO-Par Status Compact Counter Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1805:0	ENC TxPDO-Par Status Compact Counter Ch.1	PDO parameter TxPDO 6	UINT8	RO	0x06 (6 _{dec})
1805:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 6.	OCTET-STRING[14]	RO	00 1A 01 1A 02 1A 03 1A 04 1A 06 1A 07 1A

Index 1806 ENC TxPDO-Par Status Legacy Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1806:0	ENC TxPDO-Par Status Legacy Ch.1	PDO Parameter TxPDO 7	UINT8	RO	0x06 (6 _{dec})
1806:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 7.	OCTET-STRING[30]	RO	00 1A 01 1A 02 1A 03 1A 04 1A 05 1A 07 1A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Index 1807 ENC TxPDO-Par Status Compact Legacy Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1807:0	ENC TxPDO-Par Status Compact Legacy Ch.1	PDO Parameter TxPDO 8	UINT8	RO	0x06 (6 _{dec})
1807:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 8.	OCTET-STRING[30]	RO	00 1A 01 1A 02 1A 03 1A 04 1A 05 1A 06 1A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Index 1808 ENC TxPDO-Par Frequency Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1808:0	ENC TxPDO-Par Frequency Ch.1	PDO Parameter TxPDO 9	UINT8	RO	0x06 (6 _{dec})
1808:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 9.	OCTET-STRING[30]	RO	09 1A 00

Index 1809 ENC TxPDO-Par Frequency Compact Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1809:0	ENC TxPDO-Par Frequency Compact Ch.1	PDO Parameter TxPDO 10	UINT8	RO	0x06 (6 _{dec})
1809:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 10.	OCTET-STRING[30]	RO	08 1A 00

Index 180A ENC TxPDO-Par Period Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
180A:0	ENC TxPDO-Par Period Ch.1	PDO Parameter TxPDO 11	UINT8	RO	0x06 (6 _{dec})
180A:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 11.	OCTET-STRING[30]	RO	0B 1A 00

Index 180B ENC TxPDO-Par Period Compact Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
180B:0	ENC TxPDO-Par Period Compact Ch.1	PDO Parameter TxPDO 12	UINT8	RO	0x06 (6 _{dec})
180B:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 12.	OCTET-STRING[30]	RO	0A 1A 00

Index 180D ENC TxPDO-Par Timestamp Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
180D:0	ENC TxPDO-Par Timestamp Ch.1	PDO Parameter TxPDO 13	UINT8	RO	0x06 (6 _{dec})
180D:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 13.	OCTET-STRING[30]	RO	0E 1A 00

Index 180E ENC TxPDO-Par Timestamp Compact Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
180E:0	ENC TxPDO-Par Timestamp Compact Ch.1	PDO Parameter TxPDO 14	UINT8	RO	0x06 (6 _{dec})
180E:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 14.	OCTET-STRING[30]	RO	0D 1A 00

Index 1811 ENC TxPDO-Par Status Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1811:0	ENC TxPDO-Par Status Ch.2	PDO Parameter TxPDO 15	UINT8	RO	0x06 (6 _{dec})
1811:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 15.	OCTET-STRING[30]	RO	00 1A 01 1A 06 1A 07 1A 12 1A 13 1A 14 1A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Index 1812 ENC TxPDO-Par Status Compact Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1812:0	ENC TxPDO-Par Status Compact Ch.2	PDO Parameter TxPDO 16	UINT8	RO	0x06 (6 _{dec})
1812:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 16.	OCTET-STRING[30]	RO	00 1A 01 1A 06 1A 07 1A 11 1A 13 1A 14 1A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Index 1813 ENC TxPDO-Par Status Counter Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1813:0	ENC TxPDO-Par Status Counter Ch.2	PDO Parameter TxPDO 17	UINT8	RO	0x06 (6 _{dec})
1813:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 17.	OCTET-STRING[30]	RO	00 1A 01 1A 06 1A 07 1A 11 1A 12 1A 14 1A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Index 1814 ENC TxPDO-Par Status Compact Counter Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1814:0	ENC TxPDO-Par Status Compact Counter Ch.2	PDO Parameter TxPDO 19	UINT8	RO	0x06 (6 _{dec})
1814:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 19.	OCTET-STRING[30]	RO	00 1A 01 1A 06 1A 07 1A 11 1A 12 1A 13 1A 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Index 1817 ENC TxPDO-Par Frequency Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1817:0	ENC TxPDO-Par Frequency Ch.2	PDO Parameter TxPDO 20	UINT8	RO	0x06 (6 _{dec})
1817:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 20.	OCTET-STRING[30]	RO	18 1A 00

Index 1818 ENC TxPDO-Par Frequency Compact Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1818:0	ENC TxPDO-Par Frequency Compact Ch.2	PDO Parameter TxPDO 21	UINT8	RO	0x06 (6 _{dec})
1818:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 21.	OCTET-STRING[30]	RO	17 1A 00

Index 1819 ENC TxPDO-Par Period Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1819:0	ENC TxPDO-Par Period Ch.2	PDO Parameter TxPDO 22	UINT8	RO	0x06 (6 _{dec})
1819:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 22.	OCTET-STRING[30]	RO	1A 1A 00

Index 181A ENC TxPDO-Par Period Compact Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
181A:0	ENC TxPDO-Par Period Compact Ch.2	PDO Parameter TxPDO 22	UINT8	RO	0x06 (6 _{dec})
181A:06	Exclude TxPDOs	Specifies the TxPDOs (index of TxPDO mapping objects) that must not be transferred together with TxPDO 22.	OCTET-STRING[30]	RO	19 1A 00

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Index 1A00 ENC TxPDO-Map Status Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A00:0	ENC TxPDO-Map Status Ch.1	PDO Mapping TxPDO 1	UINT8	RO	0x18 (24 _{dec})
1A00:01	SubIndex 001	1. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x01 (Latch C valid))	UINT32	RO	0x6000:01, 1
1A00:02	SubIndex 002	2. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x02 (Latch extern valid))	UINT32	RO	0x6000:02, 1
1A00:03	SubIndex 003	3. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x03 (Set counter done))	UINT32	RO	0x6000:03, 1
1A00:04	SubIndex 004	4. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x04 (Counter underflow))	UINT32	RO	0x6000:04, 1
1A00:05	SubIndex 005	5. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x05 (Counter overflow))	UINT32	RO	0x6000:05, 1
1A00:06	SubIndex 006	6. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x06 (Status of input status))	UINT32	RO	0x6000:06, 1
1A00:07	SubIndex 007	7. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x07 (Open circuit))	UINT32	RO	0x6000:07, 1
1A00:08	SubIndex 008	8. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x08 (Extrapolation stall))	UINT32	RO	0x6000:08, 1
1A00:09	SubIndex 009	9. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x09 (Status of input A))	UINT32	RO	0x6000:09, 1
1A00:0A	SubIndex 010	10. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0A (Status of input B))	UINT32	RO	0x6000:0A, 1
1A00:0B	SubIndex 011	11. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0B (Status of input C))	UINT32	RO	0x6000:0B, 1
1A00:0C	SubIndex 012	12. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0C (Status of input gate))	UINT32	RO	0x6000:0C, 1
1A00:0D	SubIndex 013	13. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1) entry 0x0D (Diag))	UINT32	RO	0x6002:0D, 1
1A00:0E	SubIndex 014	14. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0E (TxPDO State))	UINT32	RO	0x6002:0E, 1
1A00:0F	SubIndex 015	15. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0F (Input cycle counter))	UINT32	RO	0x6002:0F, 2
1A00:10	SubIndex 016	16. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x10 (Software gate valid))	UINT32	RO	0x6002:10, 1
1A00:11	SubIndex 017	17. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x11 (Latch extern 2 valid))	UINT32	RO	0x6002:11, 1
1A00:12	SubIndex 018	18. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x12 (Direction inversion detected))	UINT32	RO	0x6002:12, 1
1A00:13	SubIndex 019	19. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x13 (Status of extern latch))	UINT32	RO	0x6002:13, 1
1A00:14	SubIndex 020	20. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x14 (Counter value out of range))	UINT32	RO	0x6002:14, 1
1A00:15	SubIndex 021	21. PDO Mapping entry (11 bit align)	UINT32	RO	0x0000:00, 11
1A00:16	SubIndex 022	22. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x11 (Counter value))	UINT32	RO	0x6000:11, 32
1A00:17	SubIndex 023	23. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x12 (Latch value))	UINT32	RO	0x6000:12, 32
1A00:18	SubIndex 024	24. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x22 (Latch value 2))	UINT32	RO	0x6000:22, 32

Index 1A01 ENC TxPDO-Map Status Compact Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A01:0	ENC TxPDO-Map Status Ch.1	PDO Mapping TxPDO 2	UINT8	RO	0x18 (24 _{dec})
1A01:01	SubIndex 001	1. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x01 (Latch C valid))	UINT32	RO	0x6000:01, 1
1A01:02	SubIndex 002	2. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x02 (Latch extern valid))	UINT32	RO	0x6000:02, 1
1A01:03	SubIndex 003	3. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x03 (Set counter done))	UINT32	RO	0x6000:03, 1
1A01:04	SubIndex 004	4. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x04 (Counter underflow))	UINT32	RO	0x6000:04, 1
1A01:05	SubIndex 005	5. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x05 (Counter overflow))	UINT32	RO	0x6000:05, 1
1A01:06	SubIndex 006	6. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x06 (Status of input status))	UINT32	RO	0x6000:06, 1
1A01:07	SubIndex 007	7. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x07 (Open circuit))	UINT32	RO	0x6000:07, 1
1A01:08	SubIndex 008	8. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x08 (Extrapolation stall))	UINT32	RO	0x6000:08, 1
1A01:09	SubIndex 009	9. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x09 (Status of input A))	UINT32	RO	0x6000:09, 1
1A01:0A	SubIndex 010	10. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0A (Status of input B))	UINT32	RO	0x6000:0A, 1
1A01:0B	SubIndex 011	11. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0B (Status of input C))	UINT32	RO	0x6000:0B, 1
1A01:0C	SubIndex 012	12. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0C (Status of input gate))	UINT32	RO	0x6000:0C, 1
1A01:0D	SubIndex 013	13. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0D (Diag))	UINT32	RO	0x6002:0D, 1
1A01:0E	SubIndex 014	14. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0E (TxPDO State))	UINT32	RO	0x6002:0E, 1
1A01:0F	SubIndex 015	15. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0F (Input cycle counter))	UINT32	RO	0x6002:0F, 2
1A01:10	SubIndex 016	16. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x11 (Software gate valid))	UINT32	RO	0x6002:11, 1
1A01:11	SubIndex 017	17. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x12 (Latch extern 2 valid))	UINT32	RO	0x6002:12, 1
1A01:12	SubIndex 018	18. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x13 (Direction inversion detected))	UINT32	RO	0x6002:13, 1
1A01:13	SubIndex 019	19. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x14 (Status of extern latch))	UINT32	RO	0x6002:14, 1
1A01:14	SubIndex 020	20. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x15 (Counter value out of range))	UINT32	RO	0x6002:15, 1
1A01:15	SubIndex 021	21. PDO Mapping entry (11 bit align)	UINT32	RO	0x0000:00, 11
1A01:16	SubIndex 022	22. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x11 (Counter value))	UINT32	RO	0x6000:11, 16
1A01:17	SubIndex 023	23. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x12 (Latch value))	UINT32	RO	0x6000:12, 16
1A01:18	SubIndex 024	24. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x22 (Latch value 2))	UINT32	RO	0x6000:22, 16

Index 1A02 ENC TxPDO-Map Status Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A02:0	ENC TxPDO-Map Status Ch.1	PDO Mapping TxPDO 3	UINT8	RO	0x17 (23 _{dec})
1A02:01	SubIndex 001	1. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A02:02	SubIndex 002	2. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x02 (Latch extern valid))	UINT32	RO	0x6000:02, 1
1A02:03	SubIndex 003	3. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x03 (Set counter done))	UINT32	RO	0x6000:03, 1
1A02:04	SubIndex 004	4. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x04 (Counter underflow))	UINT32	RO	0x6000:04, 1
1A02:05	SubIndex 005	5. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x05 (Counter overflow))	UINT32	RO	0x6000:05, 1
1A02:06	SubIndex 006	6. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A02:07	SubIndex 007	7. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x07 (Open circuit))	UINT32	RO	0x6000:07, 1
1A02:08	SubIndex 008	8. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A02:09	SubIndex 009	9. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x09 (Status of input A))	UINT32	RO	0x6000:09, 1
1A02:0A	SubIndex 010	10. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0A (Status of input B))	UINT32	RO	0x6000:0A, 1
1A02:0B	SubIndex 011	11. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A02:0C	SubIndex 012	12. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0C (Status of input gate))	UINT32	RO	0x6000:0C, 1
1A02:0D	SubIndex 013	13. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0D (Diag))	UINT32	RO	0x6002:0D, 1
1A02:0E	SubIndex 014	14. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0E (TxPDO State))	UINT32	RO	0x6002:0E, 1
1A02:0F	SubIndex 015	15. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0F (Input cycle counter))	UINT32	RO	0x6002:0F, 2
1A02:10	SubIndex 016	16. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x11 (Software gate valid))	UINT32	RO	0x6002:11, 1
1A02:11	SubIndex 017	17. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A02:12	SubIndex 018	18. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A02:13	SubIndex 019	19. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A02:14	SubIndex 020	20. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x15 (Counter value out of range))	UINT32	RO	0x6002:15, 1
1A02:15	SubIndex 021	21. PDO Mapping entry (11 bit align)	UINT32	RO	0x0000:00, 11
1A02:16	SubIndex 022	22. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x11 (Counter value))	UINT32	RO	0x6000:11, 32
1A02:17	SubIndex 023	23. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x12 (Latch value))	UINT32	RO	0x6000:12, 32

Index 1A03 ENC TxPDO-Map Status Compact Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A03:0	ENC TxPDO-Map Status Compact Ch.1	PDO Mapping TxPDO 4	UINT8	RO	0x17 (23 _{dec})
1A03:01	SubIndex 001	1. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A03:02	SubIndex 002	2. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x02 (Latch extern valid))	UINT32	RO	0x6000:02, 1
1A03:03	SubIndex 003	3. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x03 (Set counter done))	UINT32	RO	0x6000:03, 1
1A03:04	SubIndex 004	4. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x04 (Counter underflow))	UINT32	RO	0x6000:04, 1
1A03:05	SubIndex 005	5. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x05 (Counter overflow))	UINT32	RO	0x6000:05, 1
1A03:06	SubIndex 006	6. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A03:07	SubIndex 007	7. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x07 (Open circuit))	UINT32	RO	0x6000:07, 1
1A03:08	SubIndex 008	8. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A03:09	SubIndex 009	9. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x09 (Status of input A))	UINT32	RO	0x6000:09, 1
1A03:0A	SubIndex 010	10. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0A (Status of input B))	UINT32	RO	0x6000:0A, 1
1A03:0B	SubIndex 011	11. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A03:0C	SubIndex 012	12. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0C (Status of input gate))	UINT32	RO	0x6000:0C, 1
1A03:0D	SubIndex 013	13. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0D (Diag))	UINT32	RO	0x6002:0D, 1
1A03:0E	SubIndex 014	14. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0E (TxPDO State))	UINT32	RO	0x6002:0E, 1
1A03:0F	SubIndex 015	15. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0F (Input cycle counter))	UINT32	RO	0x6002:0F, 2
1A03:10	SubIndex 016	16. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x11 (Software gate valid))	UINT32	RO	0x6002:11, 1
1A03:11	SubIndex 017	17. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A03:12	SubIndex 018	18. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A03:13	SubIndex 019	19. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A03:14	SubIndex 020	20. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x15 (Counter value out of range))	UINT32	RO	0x6002:15, 1
1A03:15	SubIndex 021	21. PDO Mapping entry (11 bit align)	UINT32	RO	0x0000:00, 11
1A03:16	SubIndex 022	22. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x11 (Counter value))	UINT32	RO	0x6000:11, 16
1A03:17	SubIndex 023	23. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x12 (Latch value))	UINT32	RO	0x6000:12, 16

Index 1A04 ENC TxPDO-Map Status Counter Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A04:0	ENC TxPDO-Map Status Counter Ch.1	PDO Mapping TxPDO 5	UINT8	RO	0x09 (9 _{dec})
1A04:01	SubIndex 001	1. PDO Mapping entry (2 bits align)	UINT32	RO	0x0000:00, 2
1A04:02	SubIndex 002	2. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x03 (Set counter done))	UINT32	RO	0x6000:03, 1
1A04:03	SubIndex 003	3. PDO Mapping entry (9 bits align)	UINT32	RO	0x0000:00, 9
1A04:04	SubIndex 004	4. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0D (Diag))	UINT32	RO	0x6002:0D, 1
1A04:05	SubIndex 005	5. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0E (TxPDO State))	UINT32	RO	0x6002:0E, 1
1A04:06	SubIndex 006	6. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0F (Input cycle counter))	UINT32	RO	0x6002:0F, 2
1A04:07	SubIndex 007	7. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x11 (Software gate valid))	UINT32	RO	0x6002:11, 1
1A04:08	SubIndex 008	8. PDO Mapping entry (15 bits align)	UINT32	RO	0x0000:00, 15
1A04:09	SubIndex 009	9. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x11 (Counter value))	UINT32	RO	0x6000:11, 32

Index 1A05 ENC TxPDO-Map Status Compact Counter Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A05:0	ENC TxPDO-Map Status Compact Counter Ch.1	PDO Mapping TxPDO 6	UINT8	RO	0x09 (9 _{dec})
1A05:01	SubIndex 001	1. PDO Mapping entry (2 bits align)	UINT32	RO	0x0000:00, 2
1A05:02	SubIndex 002	2. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x03 (Set counter done))	UINT32	RO	0x6000:03, 1
1A05:03	SubIndex 003	3. PDO Mapping entry (9 bits align)	UINT32	RO	0x0000:00, 9
1A05:04	SubIndex 004	4. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0D (Diag))	UINT32	RO	0x6002:0D, 1
1A05:05	SubIndex 005	5. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0E (TxPDO State))	UINT32	RO	0x6002:0E, 1
1A05:06	SubIndex 006	6. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x0F (Input cycle counter))	UINT32	RO	0x6002:0F, 2
1A05:07	SubIndex 007	7. PDO Mapping entry (object 0x6002 (ENC Inputs status Ch. 1), entry 0x11 (Software gate valid))	UINT32	RO	0x6002:11, 1
1A05:08	SubIndex 008	8. PDO Mapping entry (15 bits align)	UINT32	RO	0x0000:00, 15
1A05:09	SubIndex 009	9. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x11 (Counter value))	UINT32	RO	0x6000:11, 16

Index 1A06 ENC TxPDO-Map Status Legacy Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A06:0	ENC TxPDO-Map Status Legacy Ch.1	PDO Mapping TxPDO 7	UINT8	RO	0x12 (18 _{dec})
1A06:01	SubIndex 001	1. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x01 (Latch C valid))	UINT32	RO	0x6000:01, 1
1A06:02	SubIndex 002	2. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x02 (Latch extern valid))	UINT32	RO	0x6000:02, 1
1A06:03	SubIndex 003	3. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x03 (Set counter done))	UINT32	RO	0x6000:03, 1
1A06:04	SubIndex 004	4. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x04 (Counter underflow))	UINT32	RO	0x6000:04, 1
1A06:05	SubIndex 005	5. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x05 (Counter overflow))	UINT32	RO	0x6000:05, 1
1A06:06	SubIndex 006	6. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x06 (Status of input status))	UINT32	RO	0x6000:06, 1
1A06:07	SubIndex 007	7. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x07 (Open circuit))	UINT32	RO	0x6000:07, 1
1A06:08	SubIndex 008	8. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 11), entry 0x08 (Extrapolation stall))	UINT32	RO	0x6000:08, 1
1A06:09	SubIndex 009	9. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x09 (Status of input A))	UINT32	RO	0x6000:09, 1
1A06:0A	SubIndex 010	10. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0A (Status of input B))	UINT32	RO	0x6000:0A, 1
1A06:0B	SubIndex 011	11. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0B (Status of input C))	UINT32	RO	0x6000:0B, 1
1A06:0C	SubIndex 012	12. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0C (Status of input gate))	UINT32	RO	0x6000:0C, 1
1A06:0D	SubIndex 013	13. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0D (Status of extern latch))	UINT32	RO	0x6000:0D, 1
1A06:0E	SubIndex 014	14. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0E (Sync error))	UINT32	RO	0x6000:0E, 1
1A06:0F	SubIndex 015	15. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0F (TxPDO State))	UINT32	RO	0x6000:0F, 1
1A06:10	SubIndex 016	16. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x10 (TxPDO Toggle))	UINT32	RO	0x6000:10, 1
1A06:11	SubIndex 017	17. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x11 (Counter value))	UINT32	RO	0x6000:11, 32
1A06:12	SubIndex 018	18. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x12 (Latch value))	UINT32	RO	0x6000:12, 32

Index 1A07 ENC TxPDO-Map Status Compact Legacy Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A07:0	ENC TxPDO-Map Status Compact Legacy Ch.1	PDO Mapping TxPDO 8	UINT8	RO	0x12 (1 _{dec})
1A07:01	SubIndex 001	1. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x01 (Latch C valid))	UINT32	RO	0x6000:01, 1
1A07:02	SubIndex 002	2. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x02 (Latch extern valid))	UINT32	RO	0x6000:02, 1
1A07:03	SubIndex 003	3. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x03 (Set counter done))	UINT32	RO	0x6000:03, 1
1A07:04	SubIndex 004	4. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x04 (Counter underflow))	UINT32	RO	0x6000:04, 1
1A07:05	SubIndex 005	5. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x05 (Counter overflow))	UINT32	RO	0x6000:05, 1
1A07:06	SubIndex 006	6. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x06 (Status of input status))	UINT32	RO	0x6000:06, 1
1A07:07	SubIndex 007	7. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x07 (Open circuit))	UINT32	RO	0x6000:07, 1
1A07:08	SubIndex 008	8. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x08 (Extrapolation stall))	UINT32	RO	0x6000:08, 1
1A07:09	SubIndex 009	9. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x09 (Status of input A))	UINT32	RO	0x6000:09, 1
1A07:0A	SubIndex 010	10. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0A (Status of input B))	UINT32	RO	0x6000:0A, 1
1A07:0B	SubIndex 011	11. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0B (Status of input C))	UINT32	RO	0x6000:0B, 1
1A07:0C	SubIndex 012	12. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0C (Status of input gate))	UINT32	RO	0x6000:0C, 1
1A07:0D	SubIndex 013	13. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0D (Status of extern latch))	UINT32	RO	0x6000:0D, 1
1A07:0E	SubIndex 014	14. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0E (Sync error))	UINT32	RO	0x6000:0E, 1
1A07:0F	SubIndex 015	15. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x0F (TxPDO State))	UINT32	RO	0x6000:0F, 1
1A07:10	SubIndex 016	16. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x10 (TxPDO Toggle))	UINT32	RO	0x6000:10, 1
1A07:11	SubIndex 017	17. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x11 (Counter value))	UINT32	RO	0x6000:11, 16
1A07:12	SubIndex 018	18. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x12 (Latch value))	UINT32	RO	0x6000:12, 16

Index 1A08 ENC TxPDO-Map Frequency Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A08:0	ENC TxPDO-Map Frequency Ch.1	PDO Mapping TxPDO 9	UINT8	RO	0x01 (1 _{dec})
1A08:01	SubIndex 001	1. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x13 (Frequency value))	UINT32	RO	0x6000:13, 32

Index 1A09 ENC TxPDO-Map Frequency Compact Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A09:0	ENC TxPDO-Map Frequency Compact Ch.1	PDO Mapping TxPDO 10	UINT8	RO	0x01 (1 _{dec})
1A09:01	SubIndex 001	1. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x13 (Frequency value))	UINT32	RO	0x6000:13, 16

Index 1A0A ENC TxPDO-Map Period Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A0A:0	ENC TxPDO-Map Period Ch.1	PDO Mapping TxPDO 11	UINT8	RO	0x01 (1 _{dec})
1A0A:01	SubIndex 001	1. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x14 (Period value))	UINT32	RO	0x6000:14, 32

Index 1A0B ENC TxPDO-Map Period Compact Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A0B:0	ENC TxPDO-Map Period Compact Ch.1	PDO Mapping TxPDO 12	UINT8	RO	0x01 (1 _{dec})
1A0B:01	SubIndex 001	1. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x14 (Period value))	UINT32	RO	0x6000:14, 16

Index 1A0C ENC TxPDO-Map Duty cycle Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A0C:0	ENC TxPDO-Map Duty Cycle Ch.1	PDO Mapping TxPDO 13	UINT8	RO	0x03 (3 _{dec})
1A0C:01	SubIndex 001	1. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x23 (Duty cycle))	UINT32	RO	0x6000:23, 16
1A0C:02	SubIndex 002	2. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x24 (Duty cycle min))	UINT32	RO	0x6000:24, 16
1A0C:03	SubIndex 003	3. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x25 (Duty cycle max))	UINT32	RO	0x6000:25, 16

Index 1A0D ENC TxPDO-Map Timestamp Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A0D:0	ENC TxPDO-Map Timestamp Ch.1	PDO Mapping TxPDO 14	UINT8	RO	0x04 (4 _{dec})
1A0D:01	SubIndex 001	1. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x16 (Timestamp))	UINT32	RO	0x6000:16, 64
1A0D:02	SubIndex 002	2. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x1F (Timestamp C))	UINT32	RO	0x6000:1F, 64
1A0D:03	SubIndex 003	3. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x20 (Timestamp latch))	UINT32	RO	0x6000:20, 64
1A0D:04	SubIndex 004	4. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x20 (Timestamp latch 2))	UINT32	RO	0x6000:21, 64

Index 1A0E ENC TxPDO-Map Timestamp Compact Ch.1

Index (hex)	Name	Meaning	Data type	Flags	Default
1A0E:0	ENC TxPDO-Map Timestamp Compact Ch.1	PDO Mapping TxPDO 15	UINT8	RO	0x04 (4 _{dec})
1A0E:01	SubIndex 001	1. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x16 (Timestamp))	UINT32	RO	0x6000:16, 32
1A0E:02	SubIndex 002	2. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x1F (Timestamp C))	UINT32	RO	0x6000:1F, 32
1A0E:03	SubIndex 003	3. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x20 (Timestamp latch))	UINT32	RO	0x6000:20, 32
1A0E:04	SubIndex 004	4. PDO Mapping entry (object 0x6000 (ENC Inputs Ch. 1), entry 0x20 (Timestamp latch 2))	UINT32	RO	0x6000:21, 32

Index 1A11 ENC TxPDO-Map Status Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1A11:0	ENC TxPDO-Map Status Ch.2	PDO Mapping TxPDO 16	UINT8	RO	0x17 (23 _{dec})
1A11:01	SubIndex 001	1. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A11:02	SubIndex 002	2. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x02 (Latch extern valid))	UINT32	RO	0x6010:02, 1
1A11:03	SubIndex 003	3. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x03 (Set counter done))	UINT32	RO	0x6010:03, 1
1A11:04	SubIndex 004	4. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x04 (Counter underflow))	UINT32	RO	0x6010:04, 1
1A11:05	SubIndex 005	5. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x05 (Counter overflow))	UINT32	RO	0x6010:05, 1
1A11:06	SubIndex 006	6. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A11:07	SubIndex 007	7. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x07 (Open circuit))	UINT32	RO	0x6010:07, 1
1A11:08	SubIndex 008	8. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A11:09	SubIndex 009	9. PDO Mapping entry (object object 0x6010 (ENC Inputs Ch.2), entry 0x09 (Status of input A))	UINT32	RO	0x6010:09, 1
1A11:0A	SubIndex 010	10. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x0A (Status of input B))	UINT32	RO	0x6010:0A, 1
1A11:0B	SubIndex 011	11. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A11:0C	SubIndex 012	12. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x0C (Status of input gate))	UINT32	RO	0x6010:0C, 1
1A11:0D	SubIndex 013	13. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x0D (Diag))	UINT32	RO	0x6012:0D, 1
1A11:0E	SubIndex 014	14. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x0E (TxPDO State))	UINT32	RO	0x6012:0E, 1
1A11:0F	SubIndex 015	15. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x0F (Input cycle counter))	UINT32	RO	0x6012:0F, 2
1A11:10	SubIndex 016	16. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x11 (Software gate valid))	UINT32	RO	0x6012:11, 1
1A11:11	SubIndex 017	17. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A11:12	SubIndex 018	18. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A11:13	SubIndex 019	19. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A11:14	SubIndex 020	20. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x15 (Counter value out of range))	UINT32	RO	0x6012:15, 1
1A11:15	SubIndex 021	21. PDO Mapping entry (11 bit align)	UINT32	RO	0x0000:00, 11
1A11:16	SubIndex 022	22. PDO Mapping entry (object object 0x6010 (ENC Inputs Ch.2), entry 0x11 (Counter value))	UINT32	RO	0x6010:11, 32
1A11:17	SubIndex 023	23. PDO Mapping entry (object object 0x6010 (ENC Inputs Ch.2), entry 0x12 (Latch value))	UINT32	RO	0x6010:12, 32

Index 1A12 ENC TxPDO-Map Status Compact Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1A12:0	ENC TxPDO-Map Status Compact Ch.2	PDO Mapping TxPDO 17	UINT8	RO	0x17 (23 _{dec})
1A12:01	SubIndex 001	1. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A12:02	SubIndex 002	2. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x02 (Latch extern valid))	UINT32	RO	0x6010:02, 1
1A12:03	SubIndex 003	3. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x03 (Set counter done))	UINT32	RO	0x6010:03, 1
1A12:04	SubIndex 004	4. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x04 (Counter underflow))	UINT32	RO	0x6010:04, 1
1A12:05	SubIndex 005	5. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x05 (Counter overflow))	UINT32	RO	0x6010:05, 1
1A12:06	SubIndex 006	6. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A12:07	SubIndex 007	7. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x07 (Open circuit))	UINT32	RO	0x6010:07, 1
1A12:08	SubIndex 008	8. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A12:09	SubIndex 009	9. PDO Mapping entry (object object 0x6010 (ENC Inputs Ch.2), entry 0x09 (Status of input A))	UINT32	RO	0x6010:09, 1
1A12:0A	SubIndex 010	10. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.22), entry 0x0A (Status of input B))	UINT32	RO	0x6010:0A, 1
1A12:0B	SubIndex 011	11. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A12:0C	SubIndex 012	12. PDO Mapping entry (object 0x6010 (ENC Inputs Ch. 2), entry 0x0C (Status of input gate))	UINT32	RO	0x6010:0C, 1
1A12:0D	SubIndex 013	13. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x0D (Diag))	UINT32	RO	0x6012:0D, 1
1A12:0E	SubIndex 014	14. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x0E (TxPDO State))	UINT32	RO	0x6012:0E, 1
1A12:0F	SubIndex 015	15. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x0F (Input cycle counter))	UINT32	RO	0x6012:0F, 2
1A12:10	SubIndex 016	16. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x11 (Software gate valid))	UINT32	RO	0x6012:11, 1
1A12:11	SubIndex 017	17. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A12:12	SubIndex 018	18. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A12:13	SubIndex 019	19. PDO Mapping entry (1 bit align)	UINT32	RO	0x0000:00, 1
1A12:14	SubIndex 020	20. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x15 (Counter value out of range))	UINT32	RO	0x6012:15, 1
1A12:15	SubIndex 021	21. PDO Mapping entry (11 bit align)	UINT32	RO	0x0000:00, 11
1A12:16	SubIndex 022	22. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x11 (Counter value))	UINT32	RO	0x6010:11, 16
1A12:17	SubIndex 023	23. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x12 (Latch value))	UINT32	RO	0x6010:12, 16

Index 1A13 ENC TxPDO-Map Status Counter Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1A13:0	ENC TxPDO-Map Status Counter Ch.2	PDO Mapping TxPDO 18	UINT8	RO	0x09 (9 _{dec})
1A13:01	SubIndex 001	1. PDO Mapping entry (2 bits align)	UINT32	RO	0x0000:00, 2
1A13:02	SubIndex 002	2. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x03 (Set counter done))	UINT32	RO	0x6010:03, 1
1A13:03	SubIndex 003	3. PDO Mapping entry (9 bits align)	UINT32	RO	0x0000:00, 9
1A13:04	SubIndex 004	4. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x0D (Diag))	UINT32	RO	0x6012:0D, 1
1A13:05	SubIndex 005	5. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x0E (TxPDO State))	UINT32	RO	0x6012:0E, 1
1A13:06	SubIndex 006	6. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x0F (Input cycle counter))	UINT32	RO	0x6012:0F, 2
1A13:07	SubIndex 007	7. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x11 (Software gate valid))	UINT32	RO	0x6012:11, 1
1A13:08	SubIndex 008	8. PDO Mapping entry (15 bits align)	UINT32	RO	0x0000:00, 15
1A13:09	SubIndex 009	9. PDO Mapping entry (object object 0x6010 (ENC Inputs Ch.2), entry 0x12 (Latch value))	UINT32	RO	0x6010:11, 32

Index 1A14 ENC TxPDO-Map Status Compact Counter Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1A14:0	ENC TxPDO-Map Status Compact Counter Ch.2	PDO Mapping TxPDO 19	UINT8	RO	0x09 (9 _{dec})
1A14:01	SubIndex 001	1. PDO Mapping entry (2 bits align)	UINT32	RO	0x0000:00, 2
1A14:02	SubIndex 002	2. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x03 (Set counter done))	UINT32	RO	0x6010:03, 1
1A14:03	SubIndex 003	3. PDO Mapping entry (9 bits align)	UINT32	RO	0x0000:00, 9
1A14:04	SubIndex 004	4. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x0D (Diag))	UINT32	RO	0x6012:0D, 1
1A14:05	SubIndex 005	5. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x0E (TxPDO State))	UINT32	RO	0x6012:0E, 1
1A14:06	SubIndex 006	6. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x0F (Input cycle counter))	UINT32	RO	0x6012:0F, 2
1A14:07	SubIndex 007	7. PDO Mapping entry (object 0x6012 (ENC Inputs status Ch.2), entry 0x11 (Software gate valid))	UINT32	RO	0x6012:11, 1
1A14:08	SubIndex 008	8. PDO Mapping entry (15 bits align)	UINT32	RO	0x0000:00, 15
1A14:09	SubIndex 009	9. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x12 (Latch value))	UINT32	RO	0x6010:11, 16

Index 1A17 ENC TxPDO-Map Frequency Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1A17:0	ENC TxPDO-Map Frequency Ch.2	PDO Mapping TxPDO 20	UINT8	RO	0x01 (1 _{dec})
1A17:01	SubIndex 001	1. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x13 (Frequency value))	UINT32	RO	0x6010:13, 32

Index 1A18 ENC TxPDO-Map Frequency Compact Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1A18:0	ENC TxPDO-Map Timestamp Ch.2	PDO Mapping TxPDO 21	UINT8	RO	0x04 (4 _{dec})
1A18:01	SubIndex 001	1. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x13 (Frequency value))	UINT32	RO	0x6010:13, 16

Index 1A19 ENC TxPDO-Map Period Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1A19:0	ENC TxPDO-Map Period Ch.2	PDO Mapping TxPDO 22	UINT8	RO	0x01 (1 _{dec})
1A19:01	SubIndex 001	1. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x14 (Period value))	UINT32	RO	0x6010:14, 32

Index 1A1A ENC TxPDO-Map Period Compact Ch.2

Index (hex)	Name	Meaning	Data type	Flags	Default
1A1A:0	ENC TxPDO-Map Period Ch.2	PDO Mapping TxPDO 23	UINT8	RO	0x01 (1 _{dec})
1A1A:01	SubIndex 001	1. PDO Mapping entry (object 0x6010 (ENC Inputs Ch.2), entry 0x14 (Period value))	UINT32	RO	0x6010:14, 16

4.4.8.6 1C00...1C33 | Device - System Manager**Index 1C00 Sync manager type**

Index (hex)	Name	Meaning	Data type	Flags	Default
1C00:0	Sync manager type	Using the Sync Managers	UINT8	RO	0x04 (4 _{dec})
1C00:01	SubIndex 001	Sync-Manager Type Channel 1: Mailbox Write	UINT8	RO	0x01 (1 _{dec})
1C00:02	SubIndex 002	Sync-Manager Type Channel 2: Mailbox Read	UINT8	RO	0x02 (2 _{dec})
1C00:03	SubIndex 003	Sync-Manager Type Channel 3: Process Data Write (Outputs)	UINT8	RO	0x03 (3 _{dec})
1C00:04	SubIndex 004	Sync-Manager Type Channel 4: Process Data Read (Inputs)	UINT8	RO	0x04 (4 _{dec})

Index 1C12 RxPDO assign

Index (hex)	Name	Meaning	Data type	Flags	Default
1C12:0	RxPDO assign	PDO Assign Outputs	UINT8	RW	0x01 (1 _{dec})
1C12:01	SubIndex 001	1. allocated RxPDO (contains the index of the associated RxPDO mapping object)	UINT16	RW	0x1600 (5632 _{dec})

Index 1C13 TxPDO assign

Index (hex)	Name	Meaning	Data type	Flags	Default
1C13:0	TxPDO assign	PDO Assign Inputs	UINT8	RW	0x01 (1 _{dec})
1C13:01	SubIndex 001	1. allocated TxPDO (contains the index of the associated TxPDO mapping object)	UINT16	RW	0x1A00 (6656 _{dec})

Index 1C32 SM output parameter

Index (hex)	Name	Meaning	Data type	Flags	Default
1C32:0	SM output parameter	Synchronization parameters for the outputs	UINT8	RO	0x20 (32 _{dec})
1C32:01	Sync mode	Current synchronization mode: 0: Free Run 1: Synchronous with SM 2 event 2: DC mode – synchronous with SYNC0 event 3: DC mode – synchronous with SYNC1 event	UINT16	RW	0x0001 (1 _{dec})
1C32:02	Cycle time	Cycle time (in ns): - Free Run: Cycle time of the local timer - Synchronous with SM 2 event: cycle time of the master - DC mode: SYNC0/SYNC1 cycle time	UINT32	RW	0x000F4240 (1000000 _{dec})
1C32:03	Shift time	Time between SYNC0 event and output of the outputs (in ns, DC mode only)	UINT32	RO	0x00000000 (0 _{dec})
1C32:04	Sync modes supported	Supported synchronization modes: - Bit 0 = 1: Free Run is supported - Bit 1 = 1: Synchronous with SM 2 event is supported - Bit 2–3 = 01: DC mode is supported - Bit 4–5 = 10: Output shift with SYNC1 event (DC mode only) - Bit 14 = 1: Dynamic times (measurement through writing of 0x1C32:08)	UINT16	RO	0x4807 (18439 _{dec})
1C32:05	Minimum cycle time	Minimum cycle time (in ns)	UINT32	RO	0x000101D0 (66000 _{dec})
1C32:06	Calc and copy time	Minimum time between SYNC0 and SYNC1 event (in ns, DC Mode only)	UINT32	RO	0x00000000 (0 _{dec})
1C32:07	Minimum delay time	Min. time between SYNC1 event and output of the outputs (in ns, DC mode only)	UINT32	RO	0x00000000 (000000 _{dec})
1C32:08	Command	This entry allows to measure the real required process data provision time. 0: Measurement of the local cycle time is stopped 1: Measurement of the local cycle time is started The entries 0x1C32:03, 0x1C32:05, 0x1C32:06, 0x1C32:09, 0x1C33:03 [► 181], 0x1C33:06 [► 180], 0x1C33:09 [► 181] are updated with the maximum measured values. For a subsequent measurement, the measured values are reset.	UINT16	RW	0x0000 (0 _{dec})
1C32:09	Maximum delay time	Time between SYNC1 event and output of the outputs (in ns, DC mode only)	UINT32	RO	0x00000000 (0 _{dec})
1C32:0B	SM event missed counter	Number of missed SM events in OPERATIONAL (DC mode only)	UINT16	RO	0x0000 (0 _{dec})
1C32:0C	Cycle exceeded counter	Number of occasions the cycle time was exceeded in OPERATIONAL (cycle was not completed in time or the next cycle began too early)	UINT16	RO	0x0000 (0 _{dec})
1C32:0D	Shift too short counter	Number of times that the interval between SYNC0 and SYNC1 event was too short (DC mode only)	UINT16	RO	0x0000 (0 _{dec})
1C32:20	Sync error	The synchronization was not correct in the last cycle (outputs were output too late; DC mode only)	BOOLEAN	RO	0x00 (0 _{dec})

Index 1C33 SM input parameter

Index (hex)	Name	Meaning	Data type	Flags	Default
1C33:0	SM input parameter	Synchronization parameters for the inputs	UINT8	RO	0x20 (32 _{dec})
1C33:01	Sync mode	Current synchronization mode: 0: Free Run 1: Synchronous with SM 3 event (no outputs available) 2: DC – synchronous with SYNC0 event 3: DC – synchronous with SYNC1 event 34: Synchronous with SM 2 event (outputs available)	UINT16	RW	0x0022 (34 _{dec})
1C33:02	Cycle time	Cycle time (in ns): - Free Run: Cycle time of the local timer - Synchronous with SM 2 event: cycle time of the master DC mode: SYNC0/SYNC1 cycle time	UINT32	RW	0x000F4240 (1000000 _{dec})
1C33:03	Shift time	Time between SYNC0 event and reading of the inputs (in ns, DC mode only)	UINT32	RO	0x00000000 (0 _{dec})
1C33:04	Sync modes supported	Supported synchronization modes: - Bit 0: Free Run is supported - Bit 1: Synchronous with SM 2 event is supported (outputs available) - Bit 1: Synchronous with SM 3 event is supported (no outputs available) - Bit 2–3 = 01: DC mode is supported - Bit 4–5 = 01: Input shift through local event (outputs available) - Bit 4–5 = 10: Input shift with SYNC1 event (no outputs available) - Bit 14 = 1: Dynamic times (measurement through writing of 0x1C32:08 [► 180] or 0x1C33:08)	UINT16	RO	0x4007 (16391 _{dec})
1C33:05	Minimum cycle time	Minimum cycle time (in ns)	UINT32	RO	0x000101D0 (66000 _{dec})
1C33:06	Calc and copy time	Time between reading of the inputs and the inputs being available for the master (in ns, DC mode only)	UINT32	RO	0x000101D0 (66000 _{dec})
1C33:07	Minimum delay time	Min. time between SYNC1 event and reading of the inputs (in ns, DC mode only)	UINT32	RO	0x00000000 (000000 _{dec})
1C33:08	Command	This entry allows to measure the real required process data provision time. 0: Measurement of the local cycle time is stopped 1: Measurement of the local cycle time is started The entries 0x1C32:03, 0x1C32:05, 0x1C32:06, 0x1C32:09 [► 180], 0x1C33:03, 0x1C33:06, 0x1C33:09 are updated with the maximum measured values. For a subsequent measurement, the measured values are reset.	UINT16	RW	0x0000 (0 _{dec})
1C33:09	Maximum delay time	Time between SYNC1 event and reading of the inputs (in ns, DC mode only)	UINT32	RO	0x00000000 (0 _{dec})
1C33:0B	SM event missed counter	Number of missed SM events in OPERATIONAL (DC mode only)	UINT16	RO	0x0000 (0 _{dec})
1C33:0C	Cycle exceeded counter	Number of occasions the cycle time was exceeded in OPERATIONAL (cycle was not completed in time or the next cycle began too early)	UINT16	RO	0x0000 (0 _{dec})
1C33:0D	Shift too short counter	Number of intervals between SYNC0 and SYNC1 events that are too short (DC mode only)	UINT16	RO	0x0000 (0 _{dec})
1C33:20	Sync error	The synchronization was not correct in the last cycle (outputs were output too late; DC mode only)	BOOLEAN	RO	0x00 (0 _{dec})

4.4.8.7 F000, F008, F010, F081 | Modular device profile, code word, module list, download revision

Index F000 Modular device profile

Index (hex)	Name	Meaning	Data type	Flags	Default
F000:0	Modular device profile	General information for the modular device profile	UINT8	RO	0x02 (2 _{dec})
F000:01	Module index distance	Index distance of the objects of the individual channels	UINT16	RO	0x0010 (16 _{dec})
F000:02	Maximum number of modules	Number of channels	UINT16	RO	0x0002 (2 _{dec})

Index F008 Code word

Index (hex)	Name	Meaning	Data type	Flags	Default
F008:0	Code word	reserved	UINT32	RW	0x00000000 (0 _{dec})

Index F010 Module list

Index (hex)	Name	Meaning	Data type	Flags	Default
F010:0	Module list	Maximum subindex	UINT8	RW	0x02 (2 _{dec})
F010:01	SubIndex 001	reserved	UINT32	RW	0x000001FF (511 _{dec})
F010:02	SubIndex 002	reserved	UINT32	RW	0x000001FF (511 _{dec})

Index F081 Download revision

Index (hex)	Name	Meaning	Data type	Flags	Default
F081:0	Download revision	Download revision	UINT8	RO	0x01 (1 _{dec})
F081:01	Revision number	Revision number of the EtherCAT device Relevant as a startup list entry for compatibility	UINT32	RW	0x00000000 (0 _{dec})

5 Appendix

5.1 Firmware compatibility

Beckhoff EtherCAT devices are delivered with the latest available firmware version. Firmware and hardware must be compatible; not every combination ensures compatibility. The overview below shows the hardware versions on which a firmware can be operated.

Note

- The newest possible firmware for the respective hardware should be implemented
- Beckhoff is not under any obligation to provide customers with free firmware updates for delivered products.

NOTICE

Risk of damage to the device!

Observe the notes on the firmware update in the EtherCAT System Manual in chapter “[Firmware Update](#)”. If a device is set to BOOTSTRAP mode for firmware update, it may not check whether the new firmware is suitable during download.

This may result in damage to the device! Therefore, always make sure that the firmware is suitable for the hardware version!

ED5112			
Hardware (HW)	Firmware (FW)	Revision no.	Release date
01*	01*	ED5112-0000-0016	2026/04

*) This is the current compatible firmware/hardware version at the time of the preparing this documentation. Check on the Beckhoff website whether more up-to-date [documentation](#) is available.

5.2 Documentation issue status

Version	Comment
1.1.0	• Update chapter "Support and Service" • Update structure
1.0.0	• First release for ED5112
0.1	• Preliminary documentation for ED5112

5.3 Support and Service

Beckhoff Support and Service provides assistance with questions regarding Beckhoff products and system solutions, as well as with their planning, commissioning, and operation.

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