Hardware Data Sheet Section III Addendum

ET1810 / ET1811 / ET1812 and ET1815 / ET1816

EtherCAT® Slave Controller
IP Core for Altera® and Xilinx® FPGAs

Section I – Technology
(Online at http://www.beckhoff.com)

Section II – Register Description
(Online at http://www.beckhoff.com)

Section III – Hardware Description
(Online at http://www.beckhoff.com)

Section III – Addendum
Design Flow Compatibility, FPGA Device Support, Known issues
The Beckhoff EtherCAT Slave Controller (ESC) documentation covers the following Beckhoff ESCs:

- ET1100
- ET1200
- EtherCAT IP Core for Altera® FPGAs
- EtherCAT IP Core for Xilinx® FPGAs
- ESC20

The documentation is organized in three sections. Section I and section II are common for all Beckhoff ESCs. Section III is specific for each ESC variant.

The latest documentation is available at the Beckhoff homepage (http://www.beckhoff.com).

Section I – Technology (All ESCs)

Section I deals with the basic EtherCAT technology. Starting with the EtherCAT protocol itself, the frame processing inside EtherCAT slaves is described. The features and interfaces of the physical layer with its two alternatives Ethernet and EBUS are explained afterwards. Finally, the details of the functional units of an ESC like FMMU, SyncManager, Distributed Clocks, Slave Information Interface, Interrupts, Watchdogs, and so on, are described.

Since Section I is common for all Beckhoff ESCs, it might describe features which are not available in a specific ESC. Refer to the feature details overview in Section III of a specific ESC to find out which features are available.

Section II – Register Description (All ESCs)

Section II contains detailed information about all ESC registers. This section is also common for all Beckhoff ESCs, thus registers, register bits, or features are described which might not be available in a specific ESC. Refer to the register overview and to the feature details overview in Section III of a specific ESC to find out which registers and features are available.

Section III – Hardware Description (Specific ESC)

Section III is ESC specific and contains detailed information about the ESC features, implemented registers, configuration, interfaces, pinout, usage, electrical and mechanical specification, and so on. Especially the Process Data Interfaces (PDI) supported by the ESC are part of this section.

Additional Documentation

Application notes and utilities can also be found at the Beckhoff homepage. Pinout configuration tools for ET1100/ET1200 are available. Additional information on EtherCAT IP Cores with latest updates regarding design flow compatibility, FPGA device support and known issues are also available.

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Patent Pending

The EtherCAT Technology is covered, including but not limited to the following German patent applications and patents:
- DE10304637
- DE102004044764
- DE102005009224
- DE102007017835 with corresponding applications or registrations in various other countries.

Disclaimer

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CONTENTS

1 Overview 1

2 EtherCAT IP Core for Altera FPGAs 2
  2.1 FPGA design tool compatibility 2
  2.2 FPGA device compatibility 3
  2.3 FPGA device license support 4
  2.4 Known Designflow Issues 5
    2.4.1 Active (at least until Quartus 16.0.1) 5
    2.4.1.1 Quartus Prime Standard 16.0 – today: DE2-115 MII/RGMII
           example designs: synthesis fails because of an additional
           ALTPLL signal 5
    2.4.1.2 Quartus Prime Pro 16.0 – today: Assertions and report
           messages are not evaluated 5
    2.4.1.3 Quartus 14.0 – today: Cyclone IV DBC4CE55 with NIOS
           example design PLL cannot be upgraded or edited 5
    2.4.1.4 Quartus 14.0 – today: Cyclone III example designs are not
           synthesizable 5
    2.4.1.5 TimeQuest with EtherCAT IP Core V3.0.x: Recovery timing
           violation inside the EtherCAT IP Core from 25 MHz rising edge
           to 100 MHz falling edge (5 ns) 5
    2.4.1.6 Qsys with EtherCAT IP Core V2.x.x: Avalon read error 6

2.4.2 Solved 7
  2.4.2.1 Quartus Prime Standard 16.0.0: DE2-115 MII/RGMII
           example designs: ALTPLL cannot be generated 7
  2.4.2.2 Quartus 14.0: EtherCAT IP Core V3.0.0–V3.0.6: DE2-115
           example designs are not working 7

3 EtherCAT IP Core for Xilinx FPGAs 8
  3.1 Vivado design tool compatibility 8
  3.2 ISE design tool compatibility 9
  3.3 FPGA device compatibility 10
  3.4 Known Vivado Designflow Issues 11
    3.4.1 Active (at least until Vivado 2016.2) 11
    3.4.1.1 Vivado 2016.1 – today: Synthesis fails with an RTL assertion
           error 11
    3.4.1.2 Vivado 2015.1 – today: Resource consumption too high 11
    3.4.1.3 Vivado 2015.1 – today: Synthesis results are too high 12
    3.4.1.4 Vivado 2015.1 – today: Synthesis time is too high 12
    3.4.1.5 Vivado 2015.1 – today: Assertions and report messages are not
           evaluated 12
    3.4.1.6 Vivado 2015.1 – today: ZC702_AXI_VIVADO example design
           constraints fail 13
    3.4.1.7 Vivado 2015.1 – today: ZC702_AXI_VIVADO example design
           has timing failures 13

3.4.2 Solved 14
  3.4.2.1 Vivado 2015.3 – 2015.4: EXCEPTION_ACCESS_VIOLATION
           during synthesis because of tristate drivers (crash) 14
  3.4.2.2 Vivado 2015.1: EtherCAT IP cores outside the Zynq block
           design fails in SDK (ZC702_AXI_VIVADO example design also
           affected) 14
  3.4.2.3 Vivado 2014.4: EtherCAT IP cores outside the Zynq block
           design fails in SDK (ZC702_AXI_VIVADO example design also
           affected) 15
  3.4.2.4 Vivado 2014.3: EXCEPTION_ACCESS_VIOLATION during
           synthesis (crash) 15
  3.4.2.5 Vivado 2014.1 – 2014.3: Tri-state drivers inside EtherCAT IP
           Core 15
  3.4.2.6 Vivado 2014.1 – 2014.2: The resource consumption of the
           EtherCAT IP Core is too high 16
  3.4.2.7 Vivado 2013.2 – 2014.1: The ZC702 AXI Vivado example
           design is not synthesizable 16
  3.4.2.8 Vivado 2013.1 – 2013.2 with EtherCAT IP Core until V3.00f: IP
           License issue 16

3.5 Known ISE/EDK/PlanAhead 14.7 Designflow Issues 17
  3.5.1 ISE: Crash in libSecurity_FNP.dll 17
  3.5.2 ISE/EDK/PlanAhead: Additional BUFG inserted 17
  3.5.3 ISE/EDK/PlanAhead: CLOCKDEDICATED_ROUTE=FALSE constraint
           required 17

4 Appendix 18
  4.1 Support and Service 18
    4.1.1 Beckhoff’s branch offices and representatives 18
  4.2 Beckhoff Headquarters 18
1 Overview

This document provides latest release notes, documentation addendum, supported IP Core design flows, and supported IP Core FPGA types for the following Beckhoff EtherCAT Slave Controllers:

- EtherCAT IP Core for Altera® FPGAs (up to V2.4.3 / V3.0.10)
- EtherCAT IP Core for Xilinx® FPGAs (up to V2.04d Patch 1 / V3.00k)

Refer to the ESC data sheets for further information. The ESC data sheets are available from the Beckhoff homepage (http://www.beckhoff.com).
2 EtherCAT IP Core for Altera FPGAs

2.1 FPGA design tool compatibility

Starting with V2.4.0, Qsys is supported (the example designs of V2.4.0 are SoPC builder based).

<table>
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<tr>
<th>IP Core version</th>
<th>Release date</th>
<th>Tool compatibility</th>
<th>Quartus II / Quartus Prime Standard / NIOS EDS version compatibility</th>
<th>Quartus Prime Pro version compatibility</th>
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<td></td>
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<td>SoPC Builder Qsys</td>
<td>5.1 SP2 6.1 7.0 7.1 SP1 7.2 SP2 8.0 9.0 SP1 10.0 10.1 11.0 11.1 SP2 12.0 SP1 12.1 SP1 13.0 SP1 13.1.4 14.0 14.1 14.1 15.0 15.1 16.0</td>
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<td>11/2006</td>
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<td>2.4.0 Patch 5</td>
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<td>3.0.9</td>
<td>9/2014</td>
<td>● ● - - - - - -</td>
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Table 2: Tool compatibility legend

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<td>Compatible (maybe solved issues with example designs)</td>
</tr>
<tr>
<td>○</td>
<td>Compatible, issues with some example designs</td>
</tr>
<tr>
<td>-</td>
<td>Incompatible</td>
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<tr>
<td></td>
<td>Not tested</td>
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</tbody>
</table>

1 Cyclone III devices are not supported anymore by Quartus, corresponding example designs cannot be synthesized. Refer to known issues for more details.
### 2.2 FPGA device compatibility

Starting with V2.4.0 Patch 5, the family support check of the MegaWizard plugin has been turned off (a license update is now sufficient for new FPGA families).

#### Table 3: EtherCAT IP Core for Altera FPGAs compatibility with Altera FPGAs

<table>
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<th>IP Core version</th>
<th>Cyclone II</th>
<th>Cyclone III</th>
<th>Cyclone III LS</th>
<th>Cyclone IV E</th>
<th>Cyclone IV GX</th>
<th>Cyclone V / Cyclone V SoC</th>
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<th>Arria II GX</th>
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<th>Arria V GZ</th>
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#### Table 4: FPGA compatibility legend

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</table>
2.3 FPGA device license support

Every license for the EtherCAT IP Core contains restrictions on supported FPGA devices. All FPGA device families which have license support at the date when the license is generated are unlocked. The following table shows the dates of introduction of the FPGA license support. All EtherCAT IP Core licenses which are generated past the date will include the marked FPGA devices.

<table>
<thead>
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<th>First date of license support</th>
<th>Cyclone/ Cyclone III</th>
<th>Cyclone IV E</th>
<th>Cyclone IV GX</th>
<th>Cyclone V/ Cyclone V SoC</th>
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<th>Arria II GZ</th>
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<th>Arria V GZ</th>
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<th>Stratix GX/ Stratix II GX</th>
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Table 6: License support legend

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2.4 Known Designflow Issues

2.4.1 Active (at least until Quartus 16.0.1)

2.4.1.1 Quartus Prime Standard 16.0 – today: DE2-115 MII/RGMII example designs: synthesis fails because of an additional ALTPLL signal

Synthesis fails because Qsys does no longer generate the ALTPLL phasedone signal, when this feature is not used. Previous versions of Quartus generated that signal, so it was referenced by the example designs.

Solution
Delete the signal altpll_0_phasedone_conduit_export from the component declaration and instantiation in the top level file.

2.4.1.2 Quartus Prime Pro 16.0 – today: Assertions and report messages are not evaluated

Quartus Prime Pro 16.0 does not evaluate assertions and report messages anymore, even if they are based on constants or generics. As a result, the messages shown by the EtherCAT IP core source code (text configuration box) are no longer visible. Additionally, assertions resulting in errors or failures are no longer causing the synthesis to fail, thus, illegal configurations might become synthesized to dysfunctional logic. This is unlikely to happen since the configuration interface prevents illegal configurations, but manual changes might cause them.

This issue has already been reported to Altera for Quartus Prime Pro 15.1 (beta)

Solution
Use Quartus Prime Standard.

2.4.1.3 Quartus 14.0 – today: Cyclone IV DBC4CE55 with NIOS example design PLL cannot be upgraded or edited

The PLL IP cannot be upgraded/edited because it contains a Cyclone III device as the target device family, although a Cyclone IV device is actually used:

Error (14921): Error upgrading IP component "pll.vhd".

Solution
Please change the device family in the file pll.vhd from

"Cyclone III" to "Cyclone IV E"

There are three occurrences of “Cyclone III”, just replace all of them by “Cyclone IV E”, and upgrade or edit the pll.vhd IP afterwards.

2.4.1.4 Quartus 14.0 – today: Cyclone III example designs are not synthesizable

Cyclone III devices are not supported anymore by Quartus 14, corresponding example designs cannot be synthesized.

Solution
None. Use previous Quartus versions.

2.4.1.5 TimeQuest with EtherCAT IP Core V3.0.x: Recovery timing violation inside the EtherCAT IP Core from 25 MHz rising edge to 100 MHz falling edge (5 ns)

In rare cases, a recovery timing violation occurs inside the EtherCAT IP Core between two flip-flops. The start flip-flop is called HNR3530 (using the 25 MHz clock at the rising edge), and the end flip-flop is called BNR3543.ACL2024 (using the 100 MHz clock at the falling edge). Quartus infers a CLKCTRL instance on the path, which sometimes causes the recovery timing violation.

Solution
Quartus can be forced to connect both flip-flops individually, without using the CLKCTRL instance. All other targets of the CLKCTRL will remain untouched. Please use the Assignment Editor to add this assignment:

From: *ETHERCAT_IPCORE_V2:ethercat_0|ETHERCAT_CORE:|CORE_INST:|CORE_INST|OCL3344:OCL3344|HNR3530*
To: *ETHERCAT_IPCORE_V2:ethercat_0|ETHERCAT_CORE:|CORE_INST:|CORE_INST|OCL3344:OCL3344|BNR3543.ACL2024*
Assignment Name: Global Signal
Value: Off
Enabled: Yes
2.4.1.6 Qsys with EtherCAT IP Core V2.x.x: Avalon read error

With Qsys, a 32 bit read access to the EtherCAT IP Core might have gaps between the bytes. The prefetch feature (Data width of smallest Avalon Master is set to 2 or 4 byte), which is available in EtherCAT IP Core versions before V3.0.0, does not support these gaps, read errors occur as a consequence.

Solution
Set the configuration option Data width of smallest Avalon Master to 1 byte, prefetch is disabled then.
2.4.2 Solved

2.4.2.1 Quartus Prime Standard 16.0.0: DE2-115 MII/RGMII example designs: ALTPLL cannot be generated

Generating the Qsys fails with an error caused by the ALTPLL:

Error (12252): Altpll_0: Port phasecounterselect has width 4 in TCL, but 3 in the design file

This issue is caused by Quartus, which incorrectly expects a signal width of 4 for the unused port phasecounterselect. This issue has already been reported to Altera.

Solution

Update to Quartus Prime Standard 16.0.1 (partially solves the issue). An intermediate solution is to extend the ALTPLL TCL file located in

<Quartus installation folder>/16.0/ip/altera/sopc_builder_ip/altera_avalon_altpll/altera_avalon_altpll_hw.tcl

with an additional condition for the device family (row 339 ff.):  

```tcl
set device_family [get_parameter_value INTENDED_DEVICE_FAMILY]
if { $device_family == "MAX10" || $device_family == "MAX 10" || $device_family == "Cyclone IV E" } {
    set phasectrsel_width 3
} else {
    set phasectrsel_width 4
}
```

2.4.2.2 Quartus 14.0: EtherCAT IP Core V3.0.0-V3.0.6: DE2-115 example designs are not working

The DE2-115 example designs are not working when synthesized using Quartus 14.0 (no communication, no display). The reason is that the PLL remains in reset state, because the areset input pin is not connected. Quartus 14.0 seems to use a different input value for this signal, causing the reset to be active all the time.

Solution

Open Qsys, export the altpll_0 module’s areset_conduit signal, and connect it to GND. The warning regarding this conduit disappears.
3 EtherCAT IP Core for Xilinx FPGAs

3.1 Vivado design tool compatibility

Table 7: EtherCAT IP Core for Xilinx FPGAs compatibility with Xilinx Vivado designflow tools

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Table 8: Tool compatibility legend

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### 3.2 ISE design tool compatibility

Table 9: EtherCAT IP Core for Xilinx FPGAs compatibility with Xilinx ISE designflow tools

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Table 10: Tool compatibility legend

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3.3 FPGA device compatibility

Table 11: EtherCAT Core for Xilinx FPGAs compatibility with Xilinx FPGAs

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Table 12: FPGA compatibility legend

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3.4 Known Vivado Designflow Issues

3.4.1 Active (at least until Vivado 2016.2)

3.4.1.1 Vivado 2016.1 – today: Synthesis fails with an RTL assertion error
Since Vivado 2016.1, assertions can be enabled again – this feature was removed in Vivado 2015.1. Nevertheless, Vivado 2016.1 does not handle assertions like it did before 2015.1, which results in synthesis failing for the EtherCAT IP Core, which intentionally uses assertions. The problem is that Vivado 2016.1 evaluates assertions without taking care of the context in which they are used in the source code – e.g., surrounding conditional expressions. This causes assertion errors which are actually not applicable; the Vivado versions before 2015.1 calculated them correctly. Please refer to chapter 3.4.1.5 for more details.

Message:

[Synth 8-63] RTL assertion: “DIGITAL IO PDI CONFIGURED WITHOUT ENABLING DIGITAL IO SOURCE FEATURE.”

Solution

Disable the -assert switch in synth_design since Vivado 2016.1, or disable assertion messages since Vivado 2015.3:

set_param synth.elaboration.rodinMoreOptions {rt::set_parameter ignoreVhdlAssertStmts true}

Alternatively, use a Vivado version before 2015.1.

3.4.1.2 Vivado 2015.1 – today: Resource consumption too high
The EtherCAT IP Core has a higher resource consumption then before, when used with Vivado 2015.1 and later (about 30%); it also has a higher resource consumption compared with ISE results. The higher resource consumption is highly related to how Vivado handles protected IP.

Solution

Use Vivado 2016.1 and later with the following TCL command. It should be issued before synthesis to reduce the resource consumption and compile times:

set_param synth.elaboration.rodinMoreOptions "set rt::extractNetlistGenomes false; rt::set_parameter advancedConstPropAcrossHier true"

An answer record on this topic will be available soon on the Xilinx website. The TCL command is planned to become obsolete with Vivado 2016.3.

Additionally, the following settings have been found advantageous:

- Always use the latest synthesis and implementation strategies.
- Use the synthesis strategy AreaOptimized_High
- Use the implementation strategy Area_exploreSequential

Using the TCL command and the above strategies with Vivado 2016.1 led to the best results amongst all tested Vivado versions so far. The results are similar to ISE results as well. Nevertheless, the protected IP still has a higher resource consumption than the unprotected IP (up to 10%). Xilinx is aware of this issue, and working on it.

Settings for Vivado until 2015.1

The following synthesis settings have been suggested by Xilinx, and we found them useful until Vivado 2015.1:

- Option -control_set_opt_threshold 0
- Option -fsm_extraction sequential
- Use this TCL command:

set_param synth.elaboration.rodinMoreOptions "set rt::extractNetlistGenomes false"
3.4.1.3  Vivado 2015.1 – today: Synthesis results are too high

The resource consumption reported after synthesis is by factors too high, because Vivado synthesizes every possible functionality of the EtherCAT IP core, although typically many functions are disabled by the configuration. This increases the resource consumption unnecessarily. After implementation, the resource consumption is fairly reasonable.

**Solution**

Please refer to chapter 3.4.1.1 for a solution.

3.4.1.4  Vivado 2015.1 – today: Synthesis time is too high

The synthesis time is too high because Vivado synthesizes every possible functionality of the EtherCAT IP core, although typically many functions are disabled by the configuration. This increases synthesis times unnecessarily.

**Solution**

Please refer to chapter 3.4.1.1 for a solution.

3.4.1.5  Vivado 2015.1 – today: Assertions and report messages are not evaluated

Vivado 2015.1 and later do not evaluate assertions and report messages anymore, even if they are based on constants or generics. As a result, the messages shown by the EtherCAT IP core source code (text configuration box) are no longer visible. Additionally, assertions resulting in errors or failures are no longer causing the synthesis to fail, thus, illegal configurations might become synthesized to dysfunctional logic. This is unlikely to happen since the IP core configuration tool prevents illegal configurations, but manual changes might cause them.

**Message:**

[Synth 8-312] ignoring unsynthesizable construct: assertion statement ["<...>/EtherCAT_IPCore.vhd":44812]

**Solution**

Use a previous Vivado version.

Although it is possible to re-enable assertions and report messages by issuing TCL commands since Vivado 2015.3, the EtherCAT IP Core until V3.00k cannot be synthesized with messages enabled. This is caused by the newer Vivado versions, which use a different kind of evaluation compared with Vivado 2014.4 and before. This results in assertion errors, which are not intended by the EtherCAT IP Core. Please refer to chapter 3.4.1.1 for more details.

Enable assertion messages since Vivado 2015.3:

```tcl
set_param synth.elaboration.rodinMoreOptions {rt::set_parameter ignoreVhdlAssertStmts false}
```

Since Vivado 2016.1, the `-assert` switch in `synth_design` can be used instead. Vivado 2016.2 ignores the `-assert` switch when an XDC file is used for synthesis, you can use the above setting instead, which is still working (or disable the XDC for synthesis only).

The EtherCAT IP core uses only few report messages, you can enable report messages since Vivado 2015.3:

```tcl
set_param synth.elaboration.rodinMoreOptions {rt::set_parameter ignoreVhdlReportStmts false}
```
3.4.1.6 Vivado 2015.1 – today: ZC702_AXI_VIVADO example design constraints fail
Since Vivado 2015, clock signals are renamed inside the Zynq block design. This causes some constraints to fail with such an error message:
[Vivado 12-1387] No valid object(s) found for set_false_path constraint with option '-to [get_clocks CLKOUT1]'.

Solution
In the ZC702.xdc constraint file, rename all clock references using
CLKOUT1
to the new name
clk_out2_ZYNC_BLOCK_clk_wiz_0_0

3.4.1.7 Vivado 2015.1 – today: ZC702_AXI_VIVADO example design has timing failures
Vivado introduces BUFGs on the MII_TX_CLK wires, which causes timing failures for paths from ISMNET1_PHY1_MII_TX_CLK and ISMNET1_PHY2_MII_TX_CLK. In addition, it causes suboptimal placement of other signals in the IP core, which may cause additional timing violations.

Solution
Prevent inferring a BUFG by adding this line to the ZC702.xdc constraints file:
set_property CLOCK_BUFFER_TYPE NONE [get_ports ISMNET1_PHY*_MII_TX_CLK]
If Vivado infers a BUFG anyway (experienced with Vivado 2015.3), try relaxing the constraints (3 ns instead of 5 ns):
set_input_delay -clock ISMNET1_CARRIER_25MHZ_S 3.000 [get_ports ISMNET1_PHY1_MII_TX_CLK]
set_input_delay -clock ISMNET1_CARRIER_25MHZ_S 3.000 [get_ports ISMNET1_PHY2_MII_TX_CLK]

3.4.1.8 Vivado 2014.1 – today: Upgrading ZC702_AXI_VIVADO example results in warning on port differences
When upgrading the ZC702_AXI_VIVADO example design to a newer Vivado version, a warning may be issued regarding port differences:
[IP_Flow 19-3298] Detected external port differences while upgrading IP 'ZYNC_BLOCK_processing_system7_0_0'. These changes may impact your design.
These warnings can be ignored since the different port signals are not used by the example design.

3.4.1.9 Vivado 2013.1 – today: EtherCAT IP Core is not part of the IP Catalog
The EtherCAT IP Core is not part of the IP Catalog, because the configuration options required by the EtherCAT IP Core are currently not supported by the IP Packager/IP Catalog. Additionally, Vivado does not support Spartan-6 FPGA devices, so ISE support is still required. Maintaining two types of configuration (IPCore_Config tool for ISE and IP Catalog for Vivado) is currently not planned.

Solution
Use The IPCore_Config tool to configure the EtherCAT IP Core, then add it to your project. You can either instantiate the EtherCAT IP Core wrapper directly, or you can use the IP Packager to add it to the IP Catalog (without any configuration options). The last solution allows for automatically connecting the AXI interface.
3.4.2 Solved

3.4.2.1 Vivado 2015.3 – 2015.4: EXCEPTION_ACCESS_VIOLATION during synthesis because of tristate drivers (crash)

Vivado 2015.3/2015.4 crashes during synthesis with an EXCEPTION_ACCESS_VIOLATION, if the EtherCAT IP Core is not part of a block design. This issue is related to the tristate drivers, which are optionally available inside the EtherCAT IP Core. The crash occurs because of the pure existence of the drivers in the source code, regardless of them being enabled or disabled.

Solution

This issue is fixed in Vivado 2016.1. There are two possible workarounds for 2015.x:

Set a “DONT_TOUCH” attribute on the EtherCAT IP Core instance (e.g. `axi_ethercat_user_i` in the ZC702 example design). Vivado does this automatically for IP integrated in a block design, so the issue does not appear in this case.

```tcl
attribute DONT_TOUCH : string;
attribute DONT_TOUCH of axi_ethercat_user_i: label is "TRUE";
```

Alternatively, execute the following TCL command in the Vivado GUI TCL Console and disable all internal tristate drivers inside the IP core:

```
set_param synth.elaboration.rodinMoreOptions "rt::set_parameter enableTristateBubbleUp false"
```

Caution: Using internal tristate drivers with this option causes Vivado to implement tristate drivers wrong (refer to chapter 3.4.2.5 for more information on this older issue).

3.4.2.2 Vivado 2015.1: EtherCAT IP cores outside the Zynq block design fails in SDK (ZC702_AXI_VIVADO example design also affected)

Vivado 2015.1 generates an `xparameters.h` file without base address defines if the EtherCAT IP core (and probably any other AXI slave) is connected externally to the Zynq block design. This causes a compile error for the example software in the SDK:

```
../src/EtherCAT_TestApp.c:18:28: error: ' XPAR_ETHERCAT_AXI_BASEADDR' undeclared [first use in this function]
```

Solution

Please use Vivado 2015.2 (and newer) or change the base address reference in `EtherCAT_TestApp.c` (line 18) to refer to the actual base address instead of the ` XPAR_ETHERCAT_AXI_BASEADDR ` define:

```
#define ETHERCAT_BASEADDR 0x43C00000
```
3.4.2.3  Vivado 2014.4: EtherCAT IP cores outside the Zynq block design fails in SDK (ZC702_AXI_VIVADO example design also affected)

Vivado 2014.4 generates a wrong hardware description file if the EtherCAT IP core (and probably any other AXI slave) is connected externally to the Zynq block design. This causes the SDK to fail in generating the example software with such an error message:

```
[Hsi 55-1464] Hardware instance __EMPTY__ not found in the design
```

This issue is partially fixed in Vivado 2015.1. A similar answer record (AR63036) can be found on the Xilinx website.

Solution
Please use Vivado 2015.1 (and newer) or 2014.3 to implement this example design and other designs which have the EtherCAT IP Core connected externally to the Zynq block design.

3.4.2.4  Vivado 2014.3: EXCEPTION_ACCESS_VIOLATION during synthesis (crash)

Vivado 2014.3 may stop during Technology Mapping with an access violation occasionally. Just repeat the synthesis run again and again until it succeeds (1-6 iterations until success have been seen). This issue is already approved by Xilinx and should be fixed in 2014.3 Update 1.

The Vivado console stops with these messages:

```
[...]                                                                                      
Start Technology Mapping                                                                      
Abnormal program termination (EXCEPTION_ACCESS_VIOLATION)                                      
Please check '<project name>.runs/synth_1/hs_err_pid6336.log' for details
```

The mentioned log file contains no further details except for the dump file:

```
# An unexpected error has occurred (EXCEPTION_ACCESS_VIOLATION)                             
# Stack:                                                                                     
# no stack trace available, please use hs_err_<pid>.dmp instead.
```

Solution
Run the synthesis again several times until it succeeds or update Vivado.

3.4.2.5  Vivado 2014.1 – 2014.3: Tri-state drivers inside EtherCAT IP Core

If the EtherCAT IP Core is configured to have internal tri-state buffers (e.g. for EEPROM/MI), Vivado 2014.2 (and maybe others) does not correctly implement the tristate drivers. Instead of a tristate output, a push-pull output is implemented, which might not even toggle. This issue is approved by Xilinx, it should be solved in 2014.3.

Solution
Execute the following Tcl command in the Vivado GUI Tcl Console:

```
set_param synth.elaboration.rodinMoreOptions "rt::set_parameter enableTristateBubbleUp 1"
```
3.4.2.6  
**Vivado 2014.1 – 2014.2: The resource consumption of the EtherCAT IP Core is too high**
The resource consumption of the EtherCAT IP Core is about 30% higher when it is synthesized with Vivado instead of ISE. This issue is approved by Xilinx, it is targeted to be solved in 2014.3.

**Solution**
Refer to Answer Record 61518 for a Vivado 2014.2 patch (this is not publicly available on the website). After applying the patch, the resource consumption is still higher, but much more acceptable.

3.4.2.7  
**Vivado 2013.2 – 2014.1: The ZC702 AXI Vivado example design is not synthesizable**
The ZC702 AXI Vivado example design was developed for Vivado 2014.2 and later, and it is incompatible with previous Vivado versions.

**Solution**
Use Vivado 2014.2 with the patch or a later Vivado version.

3.4.2.8  
**Vivado 2013.1 – 2013.2 with EtherCAT IP Core until V3.00f: IP License issue**
The license string used by the EtherCAT IP Core before V3.00g is not accepted by Vivado 2013.2. Note that the license key style change was not communicated to Beckhoff.

**Solution**
- use Vivado 2013.3 or later, or
- use EtherCAT IP Core V3.00g or later, or
- refer to Answer Record 56630 for a Vivado 2013.2 patch required to use the EtherCAT IP Core before V3.00g
3.5 Known ISE/EDK/PlanAhead 14.7 Designflow Issues

3.5.1 ISE: Crash in libSecurity_FNP.dll
After installing both ISE 14.7 and Vivado 2014.1 on a Microsoft Windows 7 64 bit operating system, a crash occurred while synthesizing the EtherCAT IP Core using ISE 14.7. The crash was caused by libSecurity_FNP.dll. This issue is approved by Xilinx, but there will not be any future version of ISE.

Solution
Refer to Answer Record 59851 for an ISE 14.7 patch.

3.5.2 ISE/EDK/PlanAhead: Additional BUFG inserted
Under certain circumstances, the tools insert additional BUFGs into the clock signals to the EtherCAT IP Core (CLK25, CLK100), or the BUFGs are not placed at optimal sites. This results in an error message suggesting to add a CLOCK_DEDICATED_ROUTE=FALSE constraint to the clocks. This issue occurs especially when the MAP option “Global optimization” is different from OFF. This issue is reported to Xilinx and present at least until ISE 14.5.

Solution
Either set Global optimization to OFF or add the CLOCK_DEDICATED_ROUTE=FALSE constraint.

3.5.3 ISE/EDK/PlanAhead: CLOCK_DEDICATED_ROUTE=FALSE constraint required
The PDI_SPI_SEL, PDI_SPI_DI and MII_RX_CLK0/1/2 signals are used as clock inputs for a few registers at low speed. Since these signals are not placed on dedicated clock inputs – which is not required –, Xilinx ISE sometimes issues an error, which needs to be suppressed.

Solution
Add an additional constraint for the signals causing the error message (or uncomment the appropriate lines in the example UCF files):

    CLOCK_DEDICATED_ROUTE = FALSE
4 Appendix

4.1 Support and Service
Beckhoff and our partners around the world offer comprehensive support and service, making available fast and competent assistance with all questions related to Beckhoff products and system solutions.

4.1.1 Beckhoff’s branch offices and representatives
Please contact your Beckhoff branch office or representative for local support and service on Beckhoff products!
The addresses of Beckhoff's branch offices and representatives round the world can be found on her internet pages: http://www.beckhoff.com
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4.2 Beckhoff Headquarters
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